Product Change Notification - SYST-21DDQK199

Date:

22 Apr 2020

Product Category:

32-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - PIC32MX320/340/360/440/460 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-21DDQK199

Microchip has released a new Product Documents for the PIC32MX320/340/360/440/460 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC32MX320/340/360/440/460 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Added silicon issue 77. Module: “USB Low-Speed Mode”. 2) Removal of obsolete Data Sheet Clarifications for Comparator Specifications, Flash Program Memory and Pin Diagrams.
Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 22 Apr 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

PIC32MX320/340/360/440/460 Family Silicon Errata and Data Sheet Clarification

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PIC32MX534/564/664/764

PIC32MX534/564/664/764 Family
Silicon Errata and Data Sheet Clarification

The PIC32MX534/564/664/764 family devices that you have received conform functionally to the current Device Data Sheet (DS60001156**K**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX534/564/664/764 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX534/564/664/764 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A0	A1	A2
PIC32MX534F064H	0x4400053	0x0	0x1	0x2
PIC32MX564F064H	0x4401053			
PIC32MX564F128H	0x4403053			
PIC32MX664F064H	0x4405053			
PIC32MX664F128H	0x4407053			
PIC32MX764F128H	0x440B053			
PIC32MX534F064L	0x440C053			
PIC32MX564F064L	0x440D053			
PIC32MX564F128L	0x440F053			
PIC32MX664F064L	0x4411053			
PIC32MX664F128L	0x4413053			
PIC32MX764F128L	0x4417053			

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
JTAG	—	1.	On 64-pin devices the TMS pin requires an external pull-up.	X	X	X
CAN	—	2.	The TXBAT bit status may be incorrect after an abort.	X	X	X
SPI	Slave Mode	3.	The SPIBUSY status is incorrect after an aborted transfer.	X	X	X
SPI	Slave Mode	4.	A wake-up interrupt may not be clearable.	X	X	X
SPI	Frame Mode	5.	Recovery from an underrun requires multiple SPI clock periods.	X	X	X
SPI	—	6.	Byte writes to the SPISTAT register are not decoded correctly.	X	X	X
UART	—	7.	The TRMT bit is asserted before the transmission is complete.	X	X	X
UART	IrDA® with BCLK	8.	TX data is corrupted when BRG values greater than 0x200 are used.	X	X	X
UART	IrDA	9.	The IrDA minimum bit time is not detected at all baud rates.	X	X	X
UART	UART Receive Buffer Overrun Error Status	10.	OERR bit does not get cleared on a module Reset.	X	X	X
ADC	Conversion Trigger from INT0 Interrupt	11.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	X	X	X
JTAG	Boundary Scan	12.	Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.	X	X	X
Oscillator	Clock Switch	13.	Clock switch may not work if Cache is disabled and Prefetch is enabled.	X	X	X
DMA	Suspend Status	14.	The DMABUSY status bit may not reflect the correct status if the DMA module is suspended.	X	X	X
Voltage Regulator	BOR	15.	Device may not exit BOR state if BOR event occurs.	X	X	
USB	OTG Mode	16.	When the USB model is configured for OTG operation, it may not properly recognize all required OTG voltage levels on VBUS pin.	X	X	X
Oscillator	Clock Switch	17.	If a Fail-Safe Clock Monitor (FSCM) event occurs when Primary Oscillator (POSC) mode is used, firmware clock switch requests to switch from FRC mode will fail.	X	X	X
I^2C	Slave Mode	18.	The I^2C module does not respond to address 0x78 when the STRICT and A10M bits are cleared in the I2CxCON register.	X	X	X
USB	UIDLE Interrupt	19.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	X	X	X
CPU	Constant Data Access from Flash	20.	A Data Bus Exception (DBE) may occur if an interrupt is encountered by the CPU while it is accessing constant data from Flash memory.	X	X	X
CPU	Data Write to a Peripheral	21.	A data write operation by the CPU to a peripheral may be repeated if an interrupt occurs during initial write operation.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
Oscillator	Clock Out	22.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	X	X	X
Input Capture	Idle Mode and Sleep Mode	23.	All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle mode or Sleep mode.	X	X	X
USB	Host	24.	The USB bus might not be returned to the J-state following an acknowledgment packet when running low-speed through a hub.	X	X	X
Non-5V Tolerant Pins	Pull-ups	25.	Internal pull-up resistors may not guarantee a logical '1' on non-5V tolerant pins when they are configured as digital inputs.	X	X	X
5V Tolerant Pins	Pull-ups	26.	Internal pull-up resistors may not guarantee a logical '1' on 5V tolerant pins when they are configured as digital inputs.	X	X	X
I^2C	Slave Addresses	27.	When the I^2C module is operating as a Slave, some reserved bus addresses may be Acknowledged (ACKed) when they should be not Acknowledged (NAKed).	X	X	X
UART	Synchronization	28.	On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.	X	X	X
USB Low-Speed Mode	Low-Speed Mode	29.	USB Low-Speed Device and Host modes are not supported.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: JTAG

On 64-pin devices, an external pull-up resistor is required on the TMS pin for proper JTAG.

Work around

Connect a 100k-200k pull-up to the TMS pin.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

2. Module: CAN

When an abort request occurs concurrently with a successful message transmission, and additional messages remain in the FIFO, these remaining messages are not transmitted and the TXBAT bit does not reflect the abort.

Work around

The actual FIFO status can be determined by the FIFO pointers CFIFOCI and CFIFOUA.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

3. Module: SPI

In Slave mode with Chip Select (CS) enabled, if the Master deasserts CS before the SPI clock has returned to the Idle state, the SPIBUSY bit will remain set until the next SPI data transfer is completed. The other SPI status bits will reflect the actual status.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

4. Module: SPI

In Slave mode when entering Sleep mode after a SPI transfer with SPI interrupts enabled, a false interrupt may be generated waking the device. This interrupt can be cleared; however, entering Sleep may cause the condition to occur again.

Work around

Do not use SPI in Slave mode as a wake-up source from Sleep mode.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

5. Module: SPI

In Frame mode the module is not immediately ready for further transfers after clearing the SPITUR bit. The SPITUR bit will be cleared by hardware before the SPI state machine is prepared for the next operation.

Work around

Firmware must wait at least four bit times before writing to the SPI registers after clearing the SPITUR bit.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

6. Module: SPI

Byte writes to the SPISTAT register are not decoded correctly. A byte write to byte zero of SPISTAT is actually performed on both byte zero and byte one. A byte write to byte one of SPISTAT is ignored.

Work around

Only perform word operations on the SPISTAT register.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

7. Module: UART

The TRMT bit is asserted during the STOP bit generation not after the STOP bit has been sent.

Work around

If firmware needs to be aware when the transmission is complete, firmware should add a half bit time delay after the TRMT bit is asserted.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

8. Module: UART

In IrDA mode with baud clock output enabled, the UART TX data is corrupted when the BRG value is greater than 0x200.

Work around

Use the Peripheral Bus (PB) divisor to lower the PB frequency such that the required UART BRG value is less than 0x201.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

9. Module: UART

The UART module is not fully IrDA compliant. The module does not detect the 1.6 µs minimum bit width at all baud rates as defined in the IrDA specification. The module does detect the 3/16 bit width at all baud rates.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

10. Module: UART

The OERR bit does not get cleared on a module reset. If the OERR bit is set and the module is disabled, the OERR bit retains its status even after the UART module is reinitialized.

Work around

The user software must check this bit in the UART module initialization routine and clear it if it is set.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

11. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternatively, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

12. Module: JTAG

Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

13. Module: Oscillator

Clock switch may not work if Cache is disabled (DCSZ<1:0> = 00 in the CHECON register) and Prefetch is enabled (PREFEN<1:0> not equal '00' in the CHECON register).

Work around

Set wait states to a value of 7 (PFMWS<2:0> = 111 in the CHECON register), perform a clock switch, and then set waits states to the desired value.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

14. Module: DMA

If the DMA module is suspended by setting the DMA Suspend bit (SUSPEND) in the DMA Controller Control register (DMACON), the DMA Module Busy Bit (DMABUSY) in the DMACON register may continue to show a Busy status, when the DMA module completes transaction.

Work around

Use the Channel Busy bit (CHBUSY) in the DMA Channel Control Register (DCHxCON) to check the status of the DMA channel.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

15. Module: Voltage Regulator

Device may not exit BOR state if BOR event occurs.

Work arounds

Work around 1:

VDD must remain within published specification (see Parameter DC10 of the device data sheet).

Work around 2:

Reset device by providing POR condition.

Affected Silicon Revisions

A0	A1	A2					
X	X						

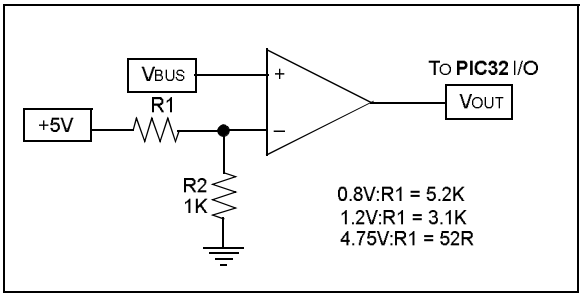
16. Module: USB

When the USB model is configured for OTG operation, it may not recognize all required OTG voltage levels on VBUS pin.

Work around

Use external comparator circuit to detect OTG specific voltage levels on VBUS pin.

FIGURE 1: EXTERNAL COMPARATOR SCHEMATIC EXAMPLE



Affected Silicon Revisions

A0	A1	A2					
X	X	X					

17. Module: Oscillator

If the Primary Oscillator (POSC) mode is implemented and a Fail-Safe Clock Monitor (FSCM) event occurs (failure of the external primary clock), the internal clock source will switch to the FRC oscillator. Subsequent firmware clock switch requests from the FRC oscillator to other clock sources will fail and the device will continue to execute on the FRC oscillator. Upon repair of the external clock source and a power-on state, the device will resume operation with the primary oscillator clock source.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

18. Module: I²C

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I²C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but it does not.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

19. Module: USB

If the bus has been idle for more than 3 ms, the UIDLE interrupt flag is set. If software clears the interrupt flag, and the bus remains idle, the UIDLE interrupt flag will not be set again.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption. (Resume, Reset, SOF, or Error).

Note: Resume and Reset are the only interrupts that should be following UIDLE assertion. If the UIDLE bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the UIDLE interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

20. Module: CPU

When both prefetch and instruction cache are enabled, a Data Bus Exception (DBE) may occur if an interrupt is encountered by the CPU while it is accessing constant data (not instructions) from Flash memory.

Work around

To avoid a DBE, use one of the following two solutions:

1. Structure application code, such that interrupts are not used while the CPU is accessing data from Flash memory.
2. Disable either the Prefetch module or CPU cache functionality as follows (by default both are disabled on a Power-on Reset (POR)):
   a) To disable the Prefetch module, set the Predictive Prefetch Enable bits, PREFEN<1:0>, in the Cache Control Register, CHECON<6:5>, to '00'.
   b) To disable CPU cache, set the Kseg0 bits, K0<2:0>, in the CP0 Configuration Register, Config<2:0>, to '010'.

Note: Disabling either the cache or Prefetch module will have minimum performance degradation, with a typical application realizing 10 percent or less performance impact.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

21. Module: CPU

During normal operation, if a CPU write operation is interrupted by an incoming interrupt, it should be aborted (not completed) and resumed after the interrupt is serviced. However, some of these write operations may not be aborted, resulting in a double write to peripherals by the CPU (the first write during the interrupt and the second write after the interrupt is serviced).

Work around

Most peripherals are not affected by this issue, as a double write will not have a negative impact. However, the following communication peripherals will double-send data if their respective transmit buffers are written twice: SPI, I²C, UART and PMP. To avoid double transmission of data, utilize DMA to transfer data to these peripherals or disable interrupts while writing to these peripherals.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

22. Module: Oscillator

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

23. Module: Input Capture

All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle or Sleep mode.

Work around

Configure the Input Capture module for Interrupt-only mode (ICM<2:0> = 111) when the CPU is in Sleep or Idle mode.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

24. Module: USB

While operating in Host mode and attached to a low-speed device through a full-speed USB hub, the host may persistently drive the bus to an SE0 state (both D+/D- as '0'), which would be interpreted as a bus Reset condition by the hub; or the host may persistently drive the bus to a J state, which would make the hub detach condition undetectable by the host.

Work around

Connect low-speed devices directly to the Host USB port and not through a USB hub.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

25. Module: Non-5V Tolerant Pins

When internal pull-ups are enabled on non-5V tolerant pins, the level as measured on the pin and available to external device inputs, may not exceed the minimum value of V_{IH}, and therefore, qualify as a logic "high". However, with respect to PIC32 devices, as long as the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic "high" for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

26. Module: 5V Tolerant Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs, may not exceed the minimum value of V_{IH}, and therefore, qualify as a logic "high". However, with respect to PIC32 devices, as long as the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic "high" for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

27. Module: I²C

When the I²C module is operating as a Slave, some reserved bus addresses may be *Acknowledged* (ACKed) when they should be *not Acknowledged* (NAKed).

As a result, there will be multiple data NAK interrupts until the Stop condition is asserted.

Work around

When the address interrupt arrives, check the address to determine if it is actually a reserved address. If the address is a reserved address, set a flag and use the flag to ignore subsequent data interrupts. When the Stop condition occurs, clear the flag.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

28. Module: UART

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement a ACK/NAK software handshake protocol to repeat lost packet transfers after restoring UART synchronization.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

29. Module: USB Low-Speed Mode

The USB Low-Speed mode is not functional in both Device and Host modes due to signal integrity compliance issues.

Work around

Use USB Full-Speed mode.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001156**K**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are currently no Data Sheet Clarifications to report.

APPENDIX A: REVISION HISTORY

Rev A Document (7/2010)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (JTAG), 2 (CAN), 3-6 (SPI) and 7-9 (UART).

Rev B Document (12/2010)

Added silicon issues 10 (UART), 11 (ADC), 12 (JTAG), 13 (Oscillator), 14 (DMA), 15 (Voltage Regulator) and 16 (USB).

Rev C Document (3/2011)

Updated the data sheet revision from "E" to "F" and updated the current silicon revision to A1 throughout the document.

Added data sheet clarification 1 (Pin Diagrams).

Rev D Document (5/2011)

Updated the data sheet revision from "F" to "G" throughout the document.

Removed data sheet clarification 1.

Rev E Document (10/2011)

Added silicon issues 17 (Oscillator), 18 (I^2C), and 19 (USB).

Added data sheet clarification 1 (Revision History).

Rev F Document (2/2012)

Updated the current silicon revision to A2 throughout the document.

Added silicon issues 20 (CPU), 21 (CPU), and 22 (Oscillator).

Rev G Document (4/2012)

Updated silicon issues 20 (CPU) and 21 (CPU).

Added silicon issue 23 (Input Capture).

Added silicon issue 24 (USB).

Rev H Document (5/2013)

Added silicon issues 25 (Non-5V Tolerant Pins) and 26 (5V Tolerant Pins).

Removed data sheet clarification 1.

Added data sheet clarifications 1 (DC Characteristics: I/O Pin Input Specifications), 2 (DC Characteristics: Program Memory), 3 (DC Characteristics: Operating Current (Idd)), 4 (DC Characteristics: Operating Current (Iidle)), 5 (DC Characteristics: Operating Current (Ipd)) and 6 (Product Identification System).

Rev J Document (4/2016)

Added silicon issues 27 (I^2C) and 28 (UART).

Rev K Document (08/2019)

Added Data Sheet Clarifications,: "There are currently no Data Sheet Clarifications to report.".

Removed previous Data Sheet Clarifications 1 through 6.

Rev L Document (04/2020)

Added silicon issue 29. Module: "USB Low-Speed Mode".
Removed "Features List" Data Sheet Clarifications.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

Affected Catalog Part Numbers (CPN)

PIC32MX534F064H-I/MR
PIC32MX534F064H-I/PT
PIC32MX534F064H-V/MR
PIC32MX534F064H-V/PT
PIC32MX534F064HT-I/MR
PIC32MX534F064HT-I/PT
PIC32MX534F064HT-V/MR
PIC32MX534F064HT-V/PT
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PIC32MX534F064L-I/PF
PIC32MX534F064L-I/PT
PIC32MX534F064L-V/BG
PIC32MX534F064L-V/PF
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PIC32MX534F064LT-I/PF
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