Product Change Notification - SYST-16NCFL501

Date:

17 Apr 2020

Product Category:

32-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - SAM G55 Series Family Silicon Errata and Data Sheet Clarifications

Notification text:

SYST-16NCFL501

Microchip has released a new Product Documents for the SAM G55 Series Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at SAM G55 Series Family Silicon Errata and Data Sheet Clarifications .

Notification Status: Final

Description of Change:

This revision includes the following updates to Data Sheet Clarifications:
1) Module: FLEXCOM in USART Mode Reference: M32DOC-1852.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 Apr 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

SAM G55 Series Family Silicon Errata and Data Sheet Clarifications

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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SAM G55 Series Family
Silicon Errata and Data Sheet Clarification

The SAM G55 Series family of devices that you have received conform functionally to the current Device Data Sheet (Atmel-11289F-ATARM-SAM-G55G-SAM-G55J-Datasheet_27-May-16), except for the anomalies described in this document.

New Silicon Errata Issues

Note:	This document provides information on new errata issues for the SAM G55 Series family of devices. Refer to the current device data sheet for all pre-existing silicon errata issues.

1. Module: FLEXCOM in USART Mode
Reference: M32DOC-1852

When the Peripheral DMA Controller (PDC) is enabled, the USART Receiver Time Out Register (RTOR) read value is incorrect.

Work around

To read correctly, the USART RTOR value for all PDC channels and buffers must be disabled (transmitter and receiver) by writing the PDC Peripheral Transfer Control Register (PTCR) with the value of 0x010A0202.

Affected Silicon Revisions

A	B						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (Atmel-11289F-ATARM-SAM-G55G-SAM-G55J-Datasheet_27-May-16).

Corrections in tables and paragraphs are shown in **bold.** Where possible, the original bold text formatting has been removed for the clarity.

1. Module: Bootloader

Chapter 7 “Bootloader” in the data sheet has a new verbiage for the NRST line. The newly added text is shown in bold.

The SAM G55 devices ship with a factory-programmed bootoader in Flash. The Flash loader downloads code either through the SPI or through the TWI0.

The Bootloader mode is entered automatically on power-up if no valid firmware is detected in the Flash. A valid firmware is detected by performing a CRC on the content of the Flash. If the CRC is correct, the application is started. Otherwise, the Bootloader mode is entered.

Alternatively, the Bootloader mode can be forced by applying 10 low pulses of 1 ms on the NRST line (with a period of 10 ms maximum). When the Bootloader detects this sequence, it asserts the pin PA01 (NCHG) low as an acknowledge.

The Bootloader mode initializes the TWI0 in Slave Mode with the I^2C address 0x26, and the SPI in Slave Mode, 8-bit data length, SPI Mode 1.

2. Module: System Configuration - CCFG_USBMR Register

In the current device data sheet section 15.9.7, the PLLFREQADJUST bit is missing from the register description. This bit occupies a bit offset of 4 as shown below.

PLLFREQADJUST: USB PLL Output Automatic Synchronization

0:USB PLL clock is not adjust

1:USB PLL output is automatically adjust at 48 MHz +/-0.25% whatever the internal 32 KHz accuracy.

3. Module: Clock Generator - CKGR_PLLAR Register

In the current device data sheet section 18.20.9, the MULA bit field for the CKGR_PLLAR register extends from bit 16 to bit 27. The corrected bit field extends from bit 16 to bit 28.

4. Module: Clock Generator - CKGR_PLLBR Register

In the current device data sheet, the MULB bit field for the CKGR_PLLBR register extends from bit field 16 to 26. The corrected bit field extended from 16 to 27.

5. Module: Clock Generator - PMC_PMMR Register

In the current device data sheet Section 18.20.32, the PLLA_MMAX bit field for the PMC_PMMR register extends from bit 0 to bit 10. The corrected bit field extends from bit 0 to bit 12.

6. Module: Clock Generator - PMC_PMMR Register

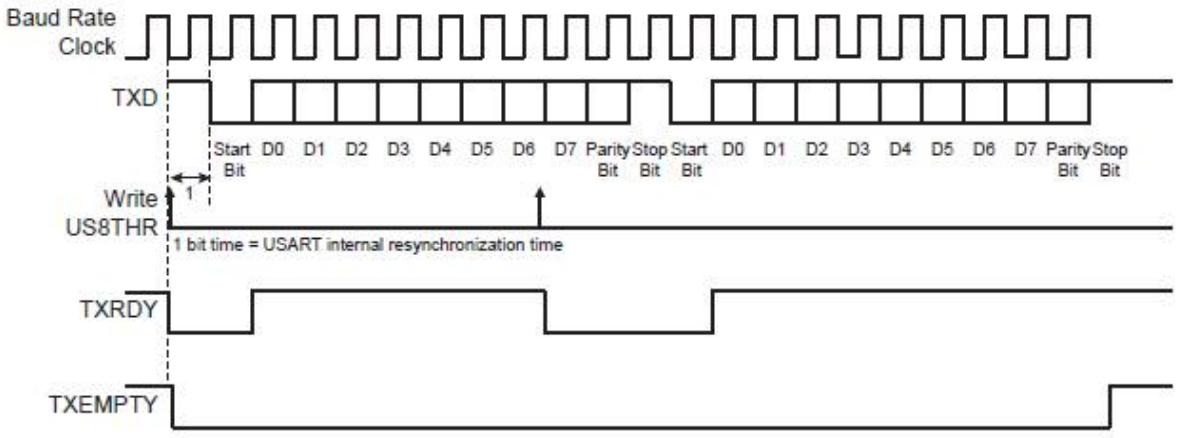
In the current device data sheet Section 18.20.32, the PLLB_MMAX bit field for the PMC_PMMR register extends from bit 16 to bit 26. The corrected bit field extends from bit 16 to bit 27.

7. Module: I^2S Controller - I2SC_MR Register

In the current device data sheet Section 33.8.2, the table for the FORMAT bit is incorrect and lists left-justified format. This format is not supported for this device.

8. Module: USART - Transmitter Operations

Figure 30-6 is incorrect. The corrected figure is as shown below:



9. Module: USART - Multi-drop Mode

In the current device data sheet Section 30.6.3.6, the bit name SENTA is incorrect. The corrected name is SENDA.

10. Module: USART - ISO7816 Mode Overview

The last paragraph of the current device data sheet Section 30.6.4.1 has erroneous text. The corrected text is given in bold.

When operating in ISO7816, either in T = 0 or T = 1 modes, the character format is fixed. The configuration is 8 data bits and 1 or 2 stop bits, regardless of the values programmed in the Mode register fields CHRL, MODE9 and CHMODE. MSBF can be used to transmit LSB or MSB first. The Parity (PAR) bit can be used to transmit in normal or inverse mode. Refer to Section 31.7.3 “USART Mode Register” and “PAR: Parity Type”.

11. Module: USART - US_RTOR Register

In the Section 30.7.20, the TimeOut (TO) bit information is incomplete, hence the following information has been added.

TimeOut (TO) value is 17 bits for USART, which supports all modes including LIN mode.

16 bits for USART, which supports all modes.

8 bits for USART, which does not support ISO7816.

12. Module: USART - US_LINMR Register

The following sentence in the current device data sheet Section 30.7.25 has an error and must be disregarded:

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

13. Module: Electrical Characteristics - Recommended Operating Conditions

Table 39-2 is updated to clarify the V_{DDIO_SLOPE} parameter. The new values are shown below.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDIO_SLOPE}	Slope on VDDIO	Single Supply, See Figure 5-2	**1.5**			V/ms
V_{DDIO_SLOPE}	Slope on VDDIO	Dual Supply, See Figure 5-3	**7**			V/ms

14. Module: USB Host Port (UHP): User Interface

The addresses listed for the UHP Registers are incorrect. The base address is **0x20400000**. All 23 register addresses must be read as 0x20400000 + the offset listed in Table 36.2.

15. Module: System I/O Lines -Table 9-6 "System I/O Configuration Pin List"

The default function after reset of PA21 and PA22 is I/O.

16. Module: Reset Controller (RSTC)

The SYSC_WPMR register is not present. References to that register must be ignored.

17. Module: Product Mapping

The offset listed for GPBR in Figure 6-1. SAM G55 Product Mapping must be 0x90.

18. Module: Supply Controller (SUPC)

In the device data sheet Section 25.5.2, the Supply Controller (SUPC) user interface erroneously lists offsets 0x20 through 0x2C as reserved. They are not part of the SUPC.

19. Module: General Purpose Backup Registers (GPBR)

The offset listed for SYS_GPBR7 in Table 28-1. Register Mapping must be 0x1C.

20. Module: ADC Channel Status Register bit descriptions

The CHx bits in the ADC_CHSR register description must be as follows:

CHx: Channel x Status

0: The corresponding channel (or part of sequence, see ADC_SEQR1.USCHx field) is disabled.

1: The corresponding channel (or part of sequence, see ADC_SEQR1.USCHx field) is enabled.

Note: For example, when ADC_MR.USEQ = 1 and a '1' is written to CH2, the channel defined in ADC_SEQR1.USCH2 is part of the sequence of conversions.

APPENDIX A: REVISION HISTORY

Revision A Document (07/2019)

This is the initial released version of this document.

Revision B Document (01/2020)

This revision includes the following updates to Data Sheet Clarifications:

- 13. Module: Electrical Characteristics - Recommended Operating Conditions
- 14. Module: USB Host Port (UHP): User Interface
- 15. Module: System I/O Lines -Table 9-6 “System I/O Configuration Pin List”
- 16. Module: Reset Controller (RSTC)
- 17. Module: Product Mapping
- 18. Module: Supply Controller (SUPC)
- 19. Module: General Purpose Backup Registers (GPBR)
- The offset listed for SYS_GPBR7 in Table 28-1. Register Mapping must be 0x1C.

Revision C Document (04/2020)

This revision includes the addition of silicon Issue 1. Module: FLEXCOM in USART Mode Reference: M32DOC-1852.

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SYST-16NCFL501 - ERRATA - SAM G55 Series Family Silicon Errata and Data Sheet Clarifications

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