Product Change Notification - SYST-14ISTP136

Date:

16 Apr 2020

Product Category:

Driver / Interface ICs

Affected CPNs:

Notification subject:

Data Sheet - HV7224 40-Channel Symmetric Row Driver Data Sheet Document Revision

Notification text:

SYST-14ISTP136

Microchip has released a new Product Documents for the HV7224 40-Channel Symmetric Row Driver Data Sheet of devices. If you are using one of these devices please read the document located at HV7224 40-Channel Symmetric Row Driver Data Sheet.

Notification Status: Final

Description of Change: 1) Converted Supertex Doc # DSFP-HV7224 to Microchip DS20005895A 2) Removed HVCMOS® Technology in the Features section 3) Changed the package marking format 4) Made minor changes throughout the document

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 16 April 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

HV7224 40-Channel Symmetric Row Driver Data Sheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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HV7224

40-Channel Symmetric Row Driver

Features

- Symmetric Row Drive
- Reduces Latent Imaging in AC Thin Film Electroluminescent (ACTFEL) Displays
- Up to +240V Output Voltage
- Low-Power Level Shifting
- 70 mA minimum Source and Sink Current
- 3 MHz Shift Register Speed
- Pin-Programmable Shift Direction (DIR, SHIFT)

Applications

- Display Driver

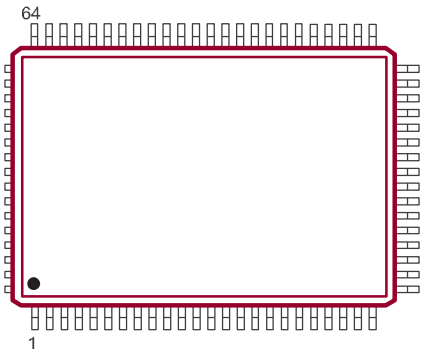
General Description

The HV7224 is a low-voltage to high-voltage serial-to-parallel converter with push-pull outputs. It is especially suitable for use as a symmetric row driver in ACTFEL displays.

When the data reset pin ($DR_{IO}A/DR_{IO}B$) is at logic high, it will reset all the outputs of the internal Shift register to zero. At the same time, the output of the Shift register will start shifting a logic high from the Least Significant bit to the Most Significant bit. The $DR_{IO}A/DR_{IO}B$ can be triggered at any time. The DIR and shift pins control the direction of data shift through the device. When DIR is at logic high, $DR_{IO}A$ is the input and $DR_{IO}B$ is the output. When DIR is grounded, $DR_{IO}B$ is the input and the $DR_{IO}A$ is the output. (See Table 3-3 for output sequence.) The Polarity ($\overline{POL}$) and Output Enable ($\overline{OE}$) pins perform the polarity select and output enable function respectively. Data is loaded on the low-to-high transition of the clock. A logic high will cause the output to swing to V_{PP} if $\overline{POL}$ is high, or to GND if $\overline{POL}$ is low. All outputs will be in High-Z state if $\overline{OE}$ is at logic high. Data output buffers are provided for cascading devices.

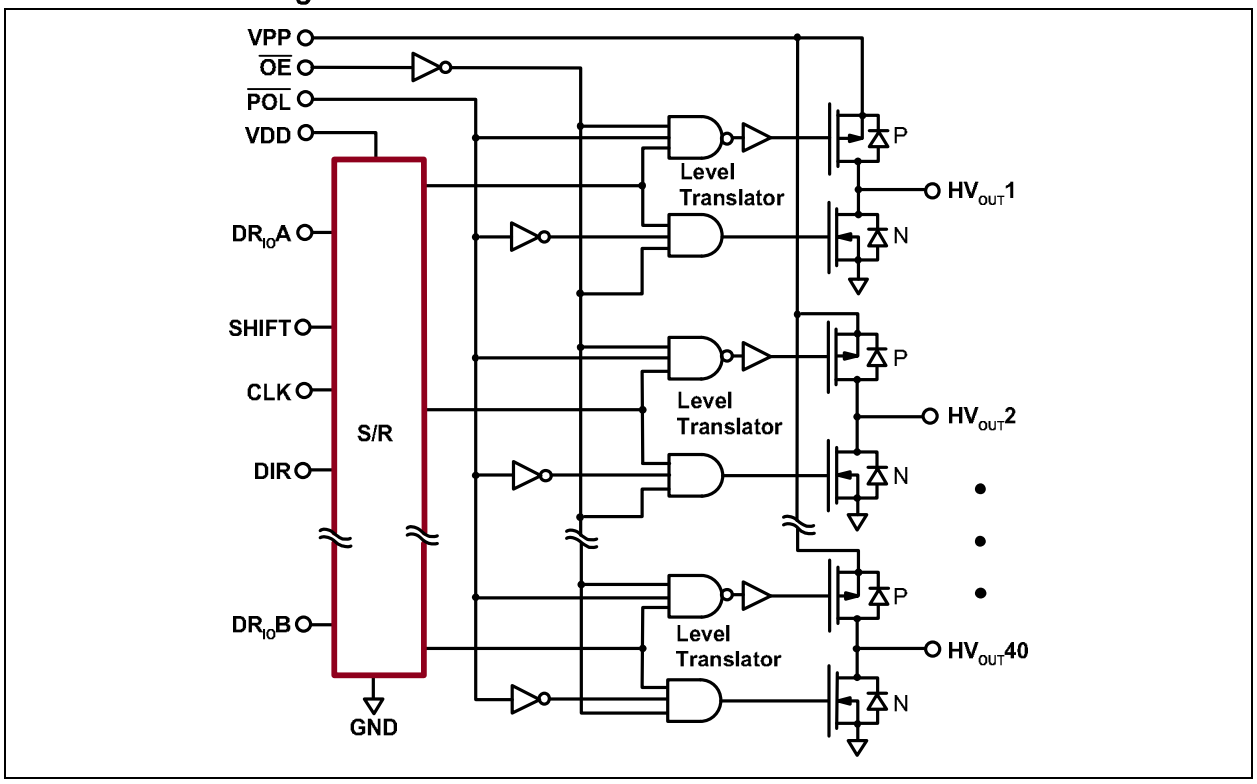
Package Type

64-lead PQFP
(Top view)

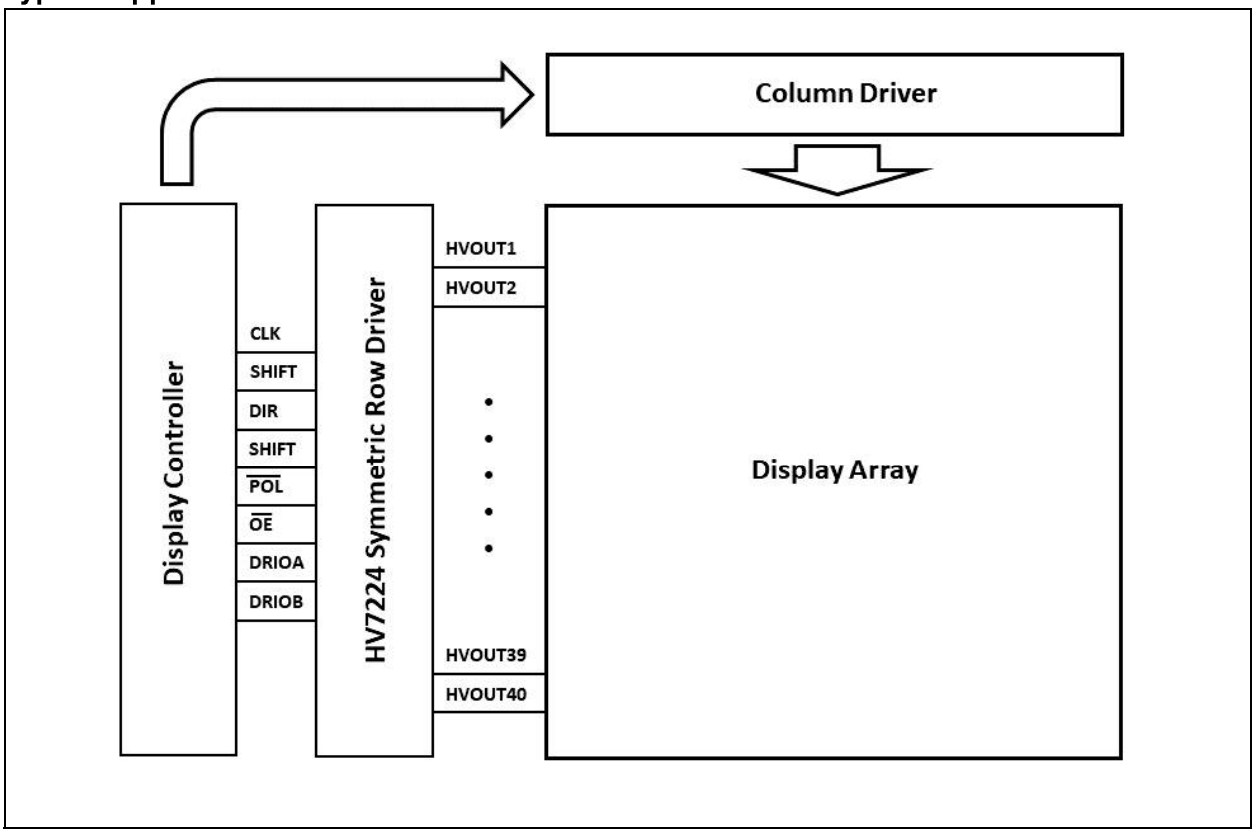


See Table 2-1 and Table 2-2 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} ..... –0.5V to +7V
High-Voltage Supply Voltage, V_{PP} ..... –0.5V to +260V
Logic Input Levels ..... –0.5V to V_{DD}+0.5V
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Total Power Dissipation:
64-lead PQFP (Note 1) ..... 1200 mW

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: For operations above 25°C ambient, derate linearly to maximum operating temperature at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	4.5	—	5.5	V	
High-Voltage Supply Voltage	V_{PP}	0	—	240	V	Note 1
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	—	V_{DD}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.2 V_{DD}	V	
Clock Frequency	f_{CLK}	—	—	3	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	
High-Voltage Output Current	I_O	—	—	±70	mA	
Allowable Current through Output Diodes	I_O	—	—	±300	mA	
Note 1: Output will not switch at V_{PP} = 0V.						

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated, V_{DD} = 5V, V_{PP} = 240V, T_A = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply Current		I_{DD}	—	—	10	mA	f_{CLK} = 3 MHz, V_{DD} = 5.5V
V_{PP} Supply Current		I_{PP}	—	—	2	mA	All outputs low or High-Z
			—	—	4	mA	One output high (**Note 1**)
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	100	µA	All V_{IN} = GND or V_{DD}
High-Level Logic Input Current		I_{IH}	—	—	1	µA	V_{IH} = V_{DD}
Low-Level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IL} = 0V
High-Level Output Voltage	HV_{OUT}	V_{OH}	190	—	—	V	I_O = –70 mA
	Data Out		4.5	—	—	V	I_O = –100 µA
Low-Level Output Voltage	HV_{OUT}	V_{OL}	—	—	50	V	I_O = 70 mA
	Data Out		—	—	0.5	V	I_O = 100 µA
HV_{OUT} Saturation Current	P-channel	I_{SAT}	–80	—	—	mA	
	N-channel		75	—	—	mA	

Note 1: Only one output can be turned on at a time.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 5V and T_A = 25°C.

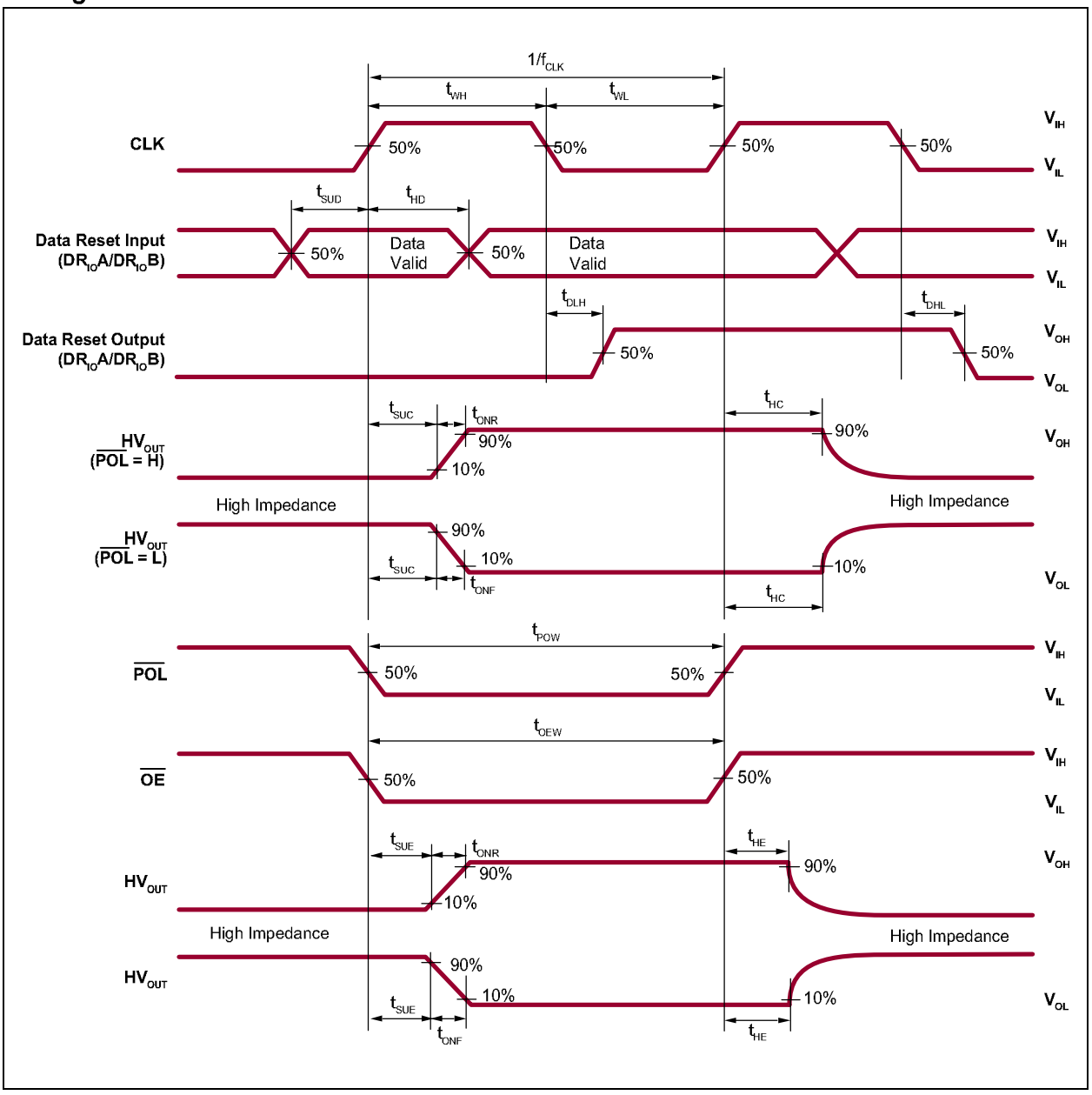
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	—	—	3	MHz	Per register, C_L = 15 pF
Clock Width, High or Low	t_{WL}, t_{WH}	150	—	—	ns	
Data Setup Time before Clock Rises	t_{SUD}	50	—	—	ns	
Data Hold Time after Clock Rises	t_{HD}	50	—	—	ns	
HV_{OUT} Delay from Clock Rises (High-Z to H or L)	t_{SUC}	—	—	1	µs	C_L = 330 pF // R_L = 10 kΩ
HV_{OUT} Delay from Output Enable $\overline{OE}$ Falls	t_{SUE}	—	—	600	ns	C_L = 330 pF // R_L = 10 kΩ
HV_{OUT} Delay from Clock Rises (H or L to High-Z)	t_{HC}	—	—	2	µs	C_L = 330 pF // R_L = 10 kΩ
HV_{OUT} Delay from Output Enable $\overline{OE}$ Falls	t_{HE}	—	—	600	ns	C_L = 330 pF // R_L = 10 kΩ
Delay Time Clock to Data Output Falls	t_{DHL}	—	—	250	ns	C_L = 15 pF (**Note 1**)
Delay Time Clock to Data Output Rises	t_{DLH}	—	—	250	ns	C_L = 15 pF (**Note 1**)
HV_{OUT} Fall Time	t_{ONF}	—	—	2	µs	C_L = 330 pF // R_L = 10 kΩ
HV_{OUT} Rise Time	t_{ONR}	—	—	2	µs	C_L = 330 pF // R_L = 10 kΩ
$\overline{POL}$ Pulse Width	t_{POW}	3	—	—	µs	
Output Enable $\overline{OE}$ Pulse Width	t_{OEW}	3	—	—	µs	
Slew Rate, V_{PP}	SR	—	—	45	V/µs	One active output driving 4.7 nF load

Note 1: The delay is measured from the trailing edge of the clock but the data is triggered by the rising edge of the clock. There is an internal delay for the data output which is equal to t_{WH}.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Storage Temperature	T_S	–65	—	+150	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
64-lead PQFP	θ_{JA}	—	41	—	°C/W	

Timing Waveforms



2.0 PIN DESCRIPTION

The two pin function options for the HV7224 64-lead PQFP are specified in Table 2-1 and Table 2-2. Refer to **Package Type** for the location of pins.

TABLE 2-1: OPTION A PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT1/40	High-voltage output
2	HVOUT2/39	High-voltage output
3	HVOUT3/38	High-voltage output
4	HVOUT4/37	High-voltage output
5	HVOUT5/36	High-voltage output
6	HVOUT6/35	High-voltage output
7	HVOUT7/34	High-voltage output
8	HVOUT8/33	High-voltage output
9	HVOUT9/32	High-voltage output
10	HVOUT10/31	High-voltage output
11	HVOUT11/30	High-voltage output
12	HVOUT12/29	High-voltage output
13	HVOUT13/28	High-voltage output
14	HVOUT14/27	High-voltage output
15	HVOUT15/26	High-voltage output
16	HVOUT16/25	High-voltage output
17	HVOUT17/24	High-voltage output
18	HVOUT18/23	High-voltage output
19	HVOUT19/22	High-voltage output
20	HVOUT20/21	High-voltage output
21	VPP	High-voltage power supply
22	NC	No connection
23	GND (Power)	High-voltage supply ground
24	GND (Logic)	Logic supply ground
25	DIR	Direction pin
26	VDD	Logic supply voltage
27	CLK	Clock pin
28	NC	No connection
29	SHIFT	Shift pin
30	NC	No connection
31	DRIOA	Data reset pin A
32	NC	No connection
33	NC	No connection
34	DRIOB	Data reset pin B

Note: Pin designation for DIR H/L, Shift = L.
Example: For DIR = H, Pin 1 is $HV_{OUT}1$
For DIR = L, Pin 1 is $HV_{OUT}40$

TABLE 2-1: OPTION A PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
35	$\overline{OE}$	Output Enable pin
36	NC	No connection
37	$\overline{POL}$	Polarity pin
38	NC	No connection
39	VDD	Logic supply voltage
40	NC	No connection
41	GND (Logic)	Logic supply ground
42	GND (Power)	High-voltage supply ground
43	NC	No connection
44	VPP	High-voltage power supply
45	HVOUT21/20	High-voltage output
46	HVOUT22/19	High-voltage output
47	HVOUT23/18	High-voltage output
48	HVOUT24/17	High-voltage output
49	HVOUT25/16	High-voltage output
50	HVOUT26/15	High-voltage output
51	HVOUT27/14	High-voltage output
52	HVOUT28/13	High-voltage output
53	HVOUT29/12	High-voltage output
54	HVOUT30/11	High-voltage output
55	HVOUT31/10	High-voltage output
56	HVOUT32/9	High-voltage output
57	HVOUT33/8	High-voltage output
58	HVOUT34/7	High-voltage output
59	HVOUT35/6	High-voltage output
60	HVOUT36/5	High-voltage output
61	HVOUT37/4	High-voltage output
62	HVOUT38/3	High-voltage output
63	HVOUT39/2	High-voltage output
64	HVOUT40/1	High-voltage output

Note: Pin designation for DIR H/L, Shift = L.
Example: For DIR = H, Pin 1 is $HV_{OUT}1$
For DIR = L, Pin 1 is $HV_{OUT}40$

TABLE 2-2: OPTION B PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT20/21	High-voltage output
2	HVOUT19/22	High-voltage output
3	HVOUT18/23	High-voltage output
4	HVOUT17/24	High-voltage output
5	HVOUT16/25	High-voltage output
6	HVOUT15/26	High-voltage output
7	HVOUT14/27	High-voltage output
8	HVOUT13/28	High-voltage output
9	HVOUT12/29	High-voltage output
10	HVOUT11/30	High-voltage output
11	HVOUT10/31	High-voltage output
12	HVOUT9/32	High-voltage output
13	HVOUT8/33	High-voltage output
14	HVOUT7/34	High-voltage output
15	HVOUT6/35	High-voltage output
16	HVOUT5/36	High-voltage output
17	HVOUT4/37	High-voltage output
18	HVOUT3/38	High-voltage output
19	HVOUT2/39	High-voltage output
20	HVOUT1/40	High-voltage output
21	VPP	High-voltage power supply
22	NC	No connection
23	GND (Power)	High-voltage supply ground
24	GND (Logic)	Logic supply ground
25	DIR	Direction pin
26	VDD	Logic supply voltage
27	CLK	Clock pin
28	NC	No connection
29	SHIFT	Shift pin
30	NC	No connection
31	DRIOA	Data reset pin A
32	NC	No connection
33	NC	No connection
34	DRIOB	Data reset pin B
35	$\overline{OE}$	Output enable pin
36	NC	No connection
37	$\overline{POL}$	Polarity pin
38	NC	No connection
39	VDD	Logic supply voltage

Note: Pin designation for DIR H/L, Shift = H.
Example: For DIR = H, Pin 1 is HVOUT20
For DIR = L, Pin 1 is HVOUT21

TABLE 2-2: OPTION B PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
40	NC	No connection
41	GND (Logic)	Logic supply ground
42	GND (Power)	Ground power
43	NC	No connection
44	VPP	High-voltage power supply
45	HVOUT40/1	High-voltage output
46	HVOUT39/2	High-voltage output
47	HVOUT38/3	High-voltage output
48	HVOUT37/4	High-voltage output
49	HVOUT36/5	High-voltage output
50	HVOUT35/6	High-voltage output
51	HVOUT34/7	High-voltage output
52	HVOUT33/8	High-voltage output
53	HVOUT32/9	High-voltage output
54	HVOUT31/10	High-voltage output
55	HVOUT30/11	High-voltage output
56	HVOUT29/12	High-voltage output
57	HVOUT28/13	High-voltage output
58	HVOUT27/14	High-voltage output
59	HVOUT26/15	High-voltage output
60	HVOUT25/16	High-voltage output
61	HVOUT24/17	High-voltage output
62	HVOUT23/18	High-voltage output
63	HVOUT22/19	High-voltage output
64	HVOUT21/20	High-voltage output

Note: Pin designation for DIR H/L, Shift = H.
Example: For DIR = H, Pin 1 is HVOUT20
For DIR = L, Pin 1 is HVOUT21

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV7224.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-Up		Power-Down	
Step	**Description**	**Step**	**Description**
1	Connect ground.	1	Remove $V_{PP.}$ (**Note 1**)
2	Apply $V_{DD.}$	2	Remove all inputs.
3	Set all inputs (Data, CLK, EN, etc.) to a known state.	3	Remove $V_{DD.}$
4	Apply $V_{PP.}$ (**Note 1**)	4	Disconnect ground.

Note 1: The V_{PP} should not drop below V_{DD} during operation.

TABLE 3-2: TRUTH FUNCTION TABLE

I/O Relations	Inputs					High-voltage Outputs
	CLK	DIR	S/R DATA	$\overline{POL}$	$\overline{OE}$	
O/P HIGH	X	X	H	H	L	H
O/P OFF	X	X	L	X	L	High-Z
O/P LOW	X	X	H	L	L	L
O/P OFF	X	X	X	X	H	All O/P High-Z

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
Data input (DR_{IO}) loaded on the low-to-high transition of the clock.
Only one active output can be set at a time.

TABLE 3-3: OUTPUT SEQUENCE OPERATION TABLE

DIR	SHIFT	Data Reset In	Data Reset Out	HV_{OUT} # Sequence	Direction (**Note 1**)
L	L	$DR_{IO}B$	$DR_{IO}A$ (**Note 2**)	40 → 1	
H	L	$DR_{IO}A$	$DR_{IO}B$ (**Note 3**)	1 → 40	
L	H	$DR_{IO}B$	$DR_{IO}A$ (**Note 2**)	20 → 1 → 40 → 21	
H	H	$DR_{IO}A$	$DR_{IO}B$ (**Note 3**)	21 → 40 → 1 → 20	

Note 1: Reference to package outline or chip layout drawing
2: $DR_{IO}A$ is $DR_{IO}B$ delayed by 40 clock pulses.
3: $DR_{IO}B$ is $DR_{IO}A$ delayed by 40 clock pulses.

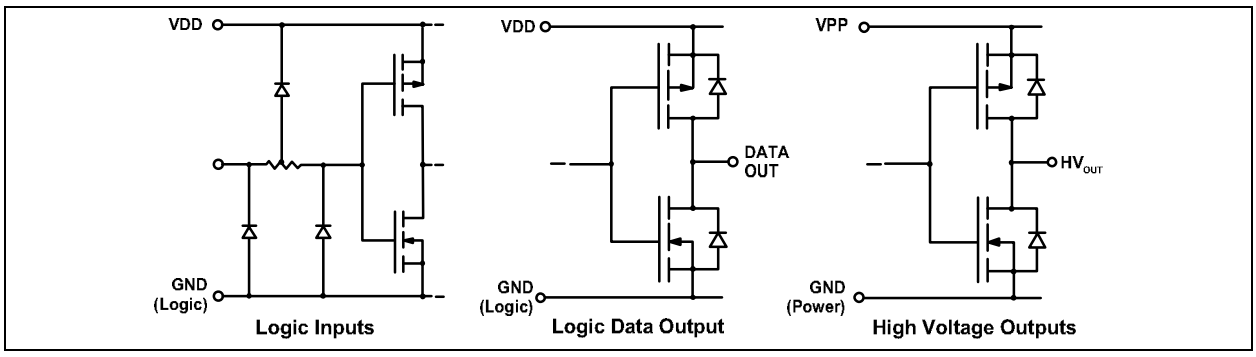


FIGURE 3-1: *Input and Output Equivalent Circuits.*

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

64-lead PQFP

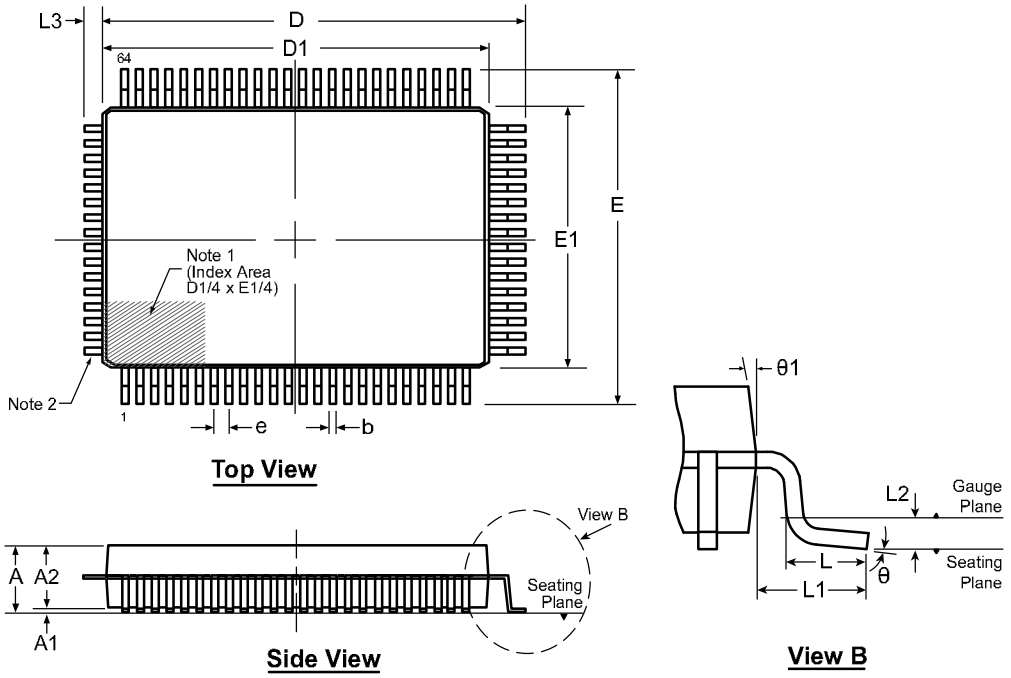
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The leads on this side are trimmed.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2020)

- Converted Supertex Doc # DSFP-HV7224 to Microchip DS20005895A
- Removed “HVCMOS® Technology” in the Features section
- Changed the package marking format
- Made minor changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV7224	=	40-Channel Symmetric Row Driver
Package:	PG	=	64-lead PQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for a PG Package

Example:

a) HV7224PG-G: 40-Channel Symmetric Row Driver, 64-lead PQFP, 66/Tray

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