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PRODUCT CHANGE NOTIFICATION

PCN: PCN201103

Date: March 16, 2020

Subject: Qualification of Fab 25 as an Additional Wafer Fab Site and Marketing Part Number Change for Select Automotive MCU Products

To: FUTURE ELECTRONICS
FUTURE ELE
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Change Type: Major

Description of Change:

Cypress announces the qualification of Fab 25 (5204 East Ben White Boulevard, Austin, TX 78741, USA) as an additional wafer fab site for select automotive MCU products. The current products are fabricated at ON Semiconductor Aizu Co., Ltd. Cypress also announces that the part number is changing from a MB prefix to a CY prefix, including a marking change of "F-logo" or "Spansion logo" removal. These changes include parts of Group 3 (GR3-C) in APCN173705C.

Changes	Current	New
Wafer Fab Site	ON Semiconductor Aizu Co., Ltd, Japan	Fab 25, USA
Part Number	MB***	CY***
Logo Marking	F-logo or Spansion logo	No logo

Benefit of Change:

Qualification of alternate manufacturing sites are part of the ongoing flexible manufacturing initiative announced by Cypress. The goal of the flexible manufacturing initiative is to provide the means for Cypress to continue to meet delivery commitments through dynamic, changing market conditions.

Part Numbers Affected: 12

See the attached 'Affected Parts List' file for a list of all part numbers affected by this change. Note that any new parts that are introduced after the publication of this PCN will include all changes outlined in this PCN.

Qualification Status:

These products have been qualified through a series of tests documented in the Qualification Test Plans summarized in the table below. These qualification reports can be found as attachments to

this PCN or by visiting www.cypress.com and typing the QTP number in the keyword search window.

QTP Number	Qualification
172504	Microcontrollers with Flash, 180nmTechnology (CU80F), Fab 25
184406	ATJ(former JD) Usuki Fab 25 Qual Report
002-29698	AECQ100 Qual Report - Fab25 180nm Technology (CU80F) Product, Grade-1 -40 to 125°C, Grade-2 -40 to 105°C

Sample Status:

Qualification samples may not be built ahead of time for all part numbers affected by this change. Please review the attached 'Affected Parts List' file for a list of affected part numbers with their associated Fab25 sample ordering part numbers. Sample ordering part numbers are subject to lead times. If you require qualification samples, please contact your local Cypress sales representative as soon as possible, preferably within 30 days of the date of this PCN, to place any sample orders.

Approximate Implementation Date:

The MB part numbers listed in attached file will be supported according to the Last Time Buy (LTB) and Last Time Ship (LTS) dates provided. The new Cypress marketing part number part will be open for order entry after the inventory on the MB part is depleted. Your Cypress Sales Representative will be in touch with you during the LTB phase to manage the backlog transition from MB marketing part number to CY marketing part number, depending on inventory depletion levels.

Anticipated Impact:

Products fabricated at the new site are completely compatible with existing products from form, fit, functional, parametric and quality performance perspectives.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:

Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:

No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration

Cypress Semiconductor Corporation

CUSTOMER CHARACTERIZATION REPORT
FOR CY96340 Series products Cypress FAB25

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CUSTOMER CHARACTERIZATION REPORT FOR CY96340 Series products Cypress FAB25

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2.0 Introduction

2.1 General Description

CY96340 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance).

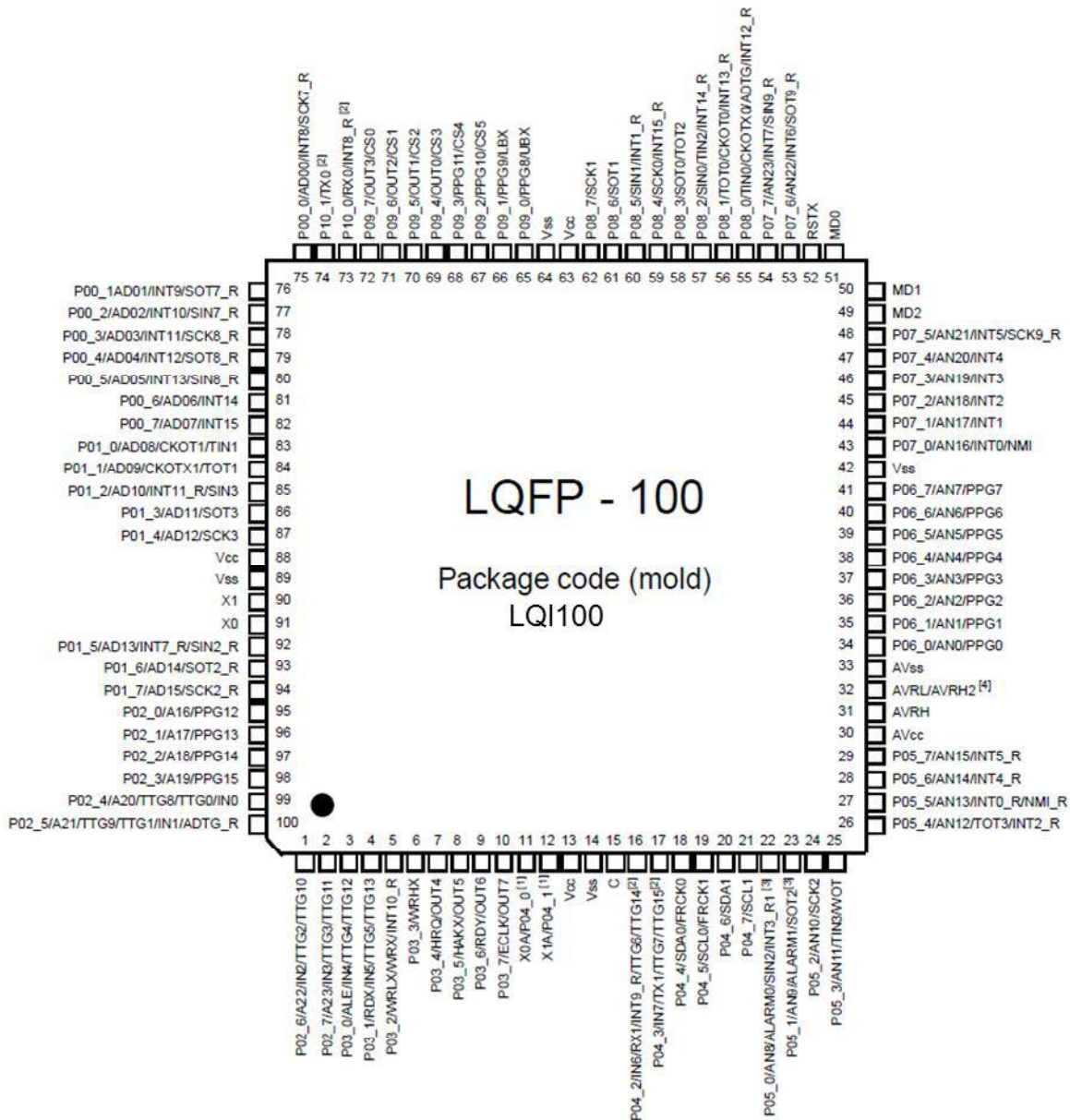
The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance – even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

2.2 Pin Assignment

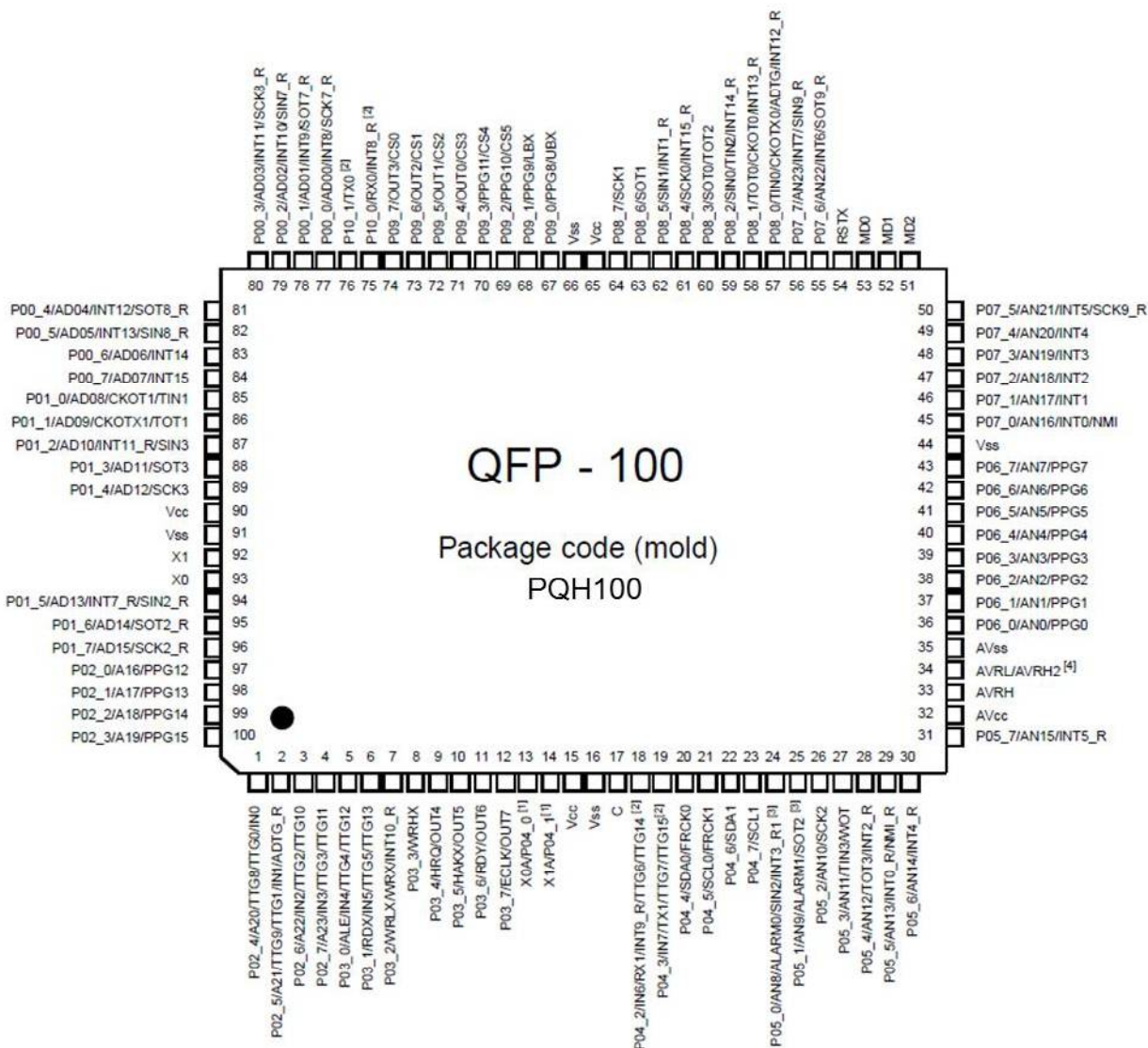
CY96340 Series (LQI100)

(Top view)



CY96340 Series (PQH100)

(Top view)



[1]: MB96(F)34xyWy: X0A, X1A
 MB96(F)34xySy: P04_0, P04_1

[2]: TX0, RX0, TX1, RX1 are not available on MB96(F)34xAyy or MB96(F)34xCyy
 TX1, RX1 are not available on MB96F345Dyy or MB96F345Fyy

[3]: ALARM0, ALARM1 are not available on MB96F345Dyy or MB96F345Fyy

[4]: AVRH2 is not available on MB96F345Dyy or MB96F345Fyy

(PQH100)

2.3 Datasheet

The datasheet is available from the Cypress Website: [CY96340 Series](#)

2.4 Application Notes

The application notes are available from the Cypress Website: [CY96340 Series](#)

2.5 White Papers

CY96340 Series products have no associated White Papers at this time.

2.6 Qualification Report

CY96340 Series products are qualified under QTP172504 and QTP173908. The qualification reports are available from the Cypress Website at:

QTP# 172504: Microcontrollers with Flash 180nm Technology (CU80F), Cypress FAB25

QTP# 173908: QTP of JD Usuki standard material LQFP package using Fab25 wafer

3.0 Characterization Hardware and Setup

3.1 DC Characterization Board

All critical DC parameters were measured on an engineering samples, with the performance board for specified ATE Tester.

3.2 DC Measurement System and Hardware

Temperature Forcing System

The Thermonics T-2500E Precision Temperature Forcing System was used to force ambient temperature.

ATE Tester

The Advantest T6573 was used to power the device and measure DC parameters.

3.3 AC Characterization Board

All critical AC parameters were measured on an engineering samples, with the performance board for specified ATE Tester.

3.4 AC Measurement System and Hardware

Temperature Forcing System

The Thermonics T-2500E Precision Temperature Forcing System was used to force ambient temperature.

ATE Tester

The Advantest T6573 was used to power the device and measure AC parameters.

3.5 Characterization Conditions and Parameters

Characterization was done on the following conditions as listed in [Table.1](#). Units were built using standard production manufacturing and chosen randomly unless specified.

Table 1. Characterization Conditions and Parameters

Parameter	Device	Fab Lot	Assy Lot	# of Devices	Voltage Range (V)	Temperature Range (°C)
DC/AC	CY96F346RWAPMC-GS-UJE2	J7423L0	1824N04	31	3.0V-6.0V	-40, 25, 125

(CY96F346 guarantee from T_A=-40 C to 125 C.)

4.0 DC Characterization

4.1 DC Characterization Summary

Parameter	Symbol	Pin Name	Conditions	Datasheet		Measured				Unit
						Current Fab		Fab25		
				Min	Max	Min	Max	Min	Max	
Output H voltage	V _{OH2}	Normal outputs	3.0V ≤ V _{CC} ≤ 4.5V I _{OH} = -1.6mA	V _{CC} - 0.5	-	V _{CC} -0.38	V _{CC} -0.27	V _{CC} -0.41	V _{CC} -0.28	V
	V _{OH5}	Normal outputs	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -5mA	V _{CC} - 0.5	-	V _{CC} -0.40	V _{CC} -0.28	V _{CC} -0.48	V _{CC} -0.31	V
	V _{OH3}	3mA outputs	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -3mA	V _{CC} - 0.5	-	V _{CC} -0.38	V _{CC} -0.27	V _{CC} -0.39	V _{CC} -0.27	V
Output L voltage	V _{OL2}	Normal outputs	3.0V ≤ V _{CC} ≤ 4.5V I _{OL} = +1.6mA	-	0.4	0.13	0.21	0.11	0.19	V
	V _{OL5}	Normal outputs	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = +5mA	-	0.4	0.16	0.26	0.16	0.29	V
	V _{OL3}	3mA outputs	3.0V ≤ V _{CC} ≤ 5.5V I _{OL} = +3mA	-	0.4	0.12	0.19	0.11	0.18	V
Input leak current	I _{IL}	Pnn_m	V _{SS} < V _I < V _{CC} AV _{SS} , AV _{RL} < V _I < AV _{CC} , AV _{RH}	-1	1	-0.02	0.02	-0.04	0.18	μA
Pull-up resistance	R _{UP}	Pnn_m, RSTX	V _{CC} = 5.5 V	25	100	33.1	52.4	31.4	51.9	kΩ

Parameter	Symbol	Pin Name	Conditions (at T _A)	Datasheet		Measured				Unit	
				Min	Max	Current Fab		Fab25			
						Min	Max	Min	Max		
Power supply current in Run modes	I _{CCPLL}	V _{CC}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	44	33.8	35.4	36.0	38.2	mA
			+125°C	-	47	35.6	36.8	38.6	40.8	mA	
			PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	57	43.2	45.6	45.4	48.6	mA
			+125°C	-	60	44.8	46.6	48.2	51.0	mA	
			PLL Run mode with CLKS1/2 = 72MHz, CLKB = CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	50	37.8	39.6	39.8	42.6	mA
			+125°C	-	53	39.4	41.0	42.8	45.4	mA	
	I _{CCMAIN}	V _{CC}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	-	5.5	4.2	4.4	4.4	4.7	mA
				+125°C	-	8.5	4.9	5.1	5.8	6.8	mA
	I _{CCRCH}	V _{CC}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	-	4	2.5	2.6	2.6	2.9	mA
				+125°C	-	6.5	3.2	3.4	4.0	4.8	mA
	I _{CCRCL}	V _{CC}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMs = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	-	0.25	0.13	0.14	0.15	0.18	mA
				+125°C	-	3.2	0.82	0.90	1.18	1.33	mA
Power supply current in Sleep modes	I _{CCSPLL}	V _{CC}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	10.5	6.6	6.9	7.0	7.4	mA
			+125°C	-	13	7.4	7.7	8.5	9.7	mA	
			PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	15.5	11.0	11.5	11.6	12.3	mA
			+125°C	-	18	12.0	12.4	13.4	14.6	mA	
			PLL Sleep mode with CLKS1/2 = 72MHz, CLKP1 = 36MHz, CLKP2 = 18MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	12	8.4	8.8	8.8	9.4	mA
			+125°C	-	14.5	9.3	9.6	10.5	11.7	mA	
	I _{CCsMAIN}	V _{CC}	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25°C	-	1.8	1.06	1.11	1.13	1.20	mA
				+125°C	-	4.5	2.16	2.24	2.28	2.66	mA
	I _{CCSRCH}	V _{CC}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25°C	-	1.4	0.73	0.77	0.78	0.83	mA
				+125°C	-	4	1.74	1.79	1.94	2.32	mA
	I _{CCSRCL}	V _{CC}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMss = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	-	0.15	0.03	0.04	0.05	0.07	mA
				+125°C	-	3	0.74	0.82	1.08	1.19	mA

Parameter	Symbol	Pin Name	Conditions (at T _A)	Datasheet		Measured				Unit	
				Min	Max	Current Fab		Fab25			
						Min	Max	Min	Max		
Power supply current in Timer modes	I _{CCTPLL}	V _{CC}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	-	2	1.37	1.44	1.50	1.65	mA
			+125°C	-	5	2.6	2.7	2.7	3.1	mA	
	I _{CCTMAIN}	V _{CC}	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	-	0.15	0.05	0.06	0.07	0.09	mA
			+125°C	-	2.9	0.79	0.86	1.14	1.28	mA	
	I _{CCTRCH}	V _{CC}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	-	0.15	0.06	0.07	0.08	0.09	mA
			+125°C	-	2.9	0.79	0.87	1.15	1.29	mA	
	I _{CCTRCL}	V _{CC}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	-	0.1	0.02	0.03	0.03	0.04	mA
			+125°C	-	2.85	0.73	0.81	1.09	1.24	mA	
Power supply current in Stop Mode	I _{CCH}	V _{CC}	VR _{CR} :LPMB[2:0] = 110B (Core voltage at 1.8V)	+25°C	-	0.08	0.01	0.02	0.02	0.03	mA
				+125°C	-	2.8	0.73	0.81	1.09	1.23	mA
			VR _{CR} :LPMB[2:0] = 000B (Core voltage at 1.2V)	+25°C	-	0.06	0.01	0.02	0.02	0.03	mA
				+125°C	-	2.3	0.64	0.70	0.92	1.02	mA
Analog input leakage current	I _{AIN}	Ann	AV _{CC} = 5.5 V, AV _{SS} , AV _{RL} < VI < AV _{CC} , AV _{RH}	+25°C	-1	+1	0.00	0.01	0.00	0.02	μA
				+125°C	-3	+3	0.17	0.23	0.30	0.38	μA
Power supply current	I _A	AV _{CC}	V _{CC} = AV _{CC} = AV _{RH} = 5.5 V A/D Converter active	-	5	1.94	2.64	2.02	2.88	mA	
	I _{AH}	AV _{CC}	V _{CC} = AV _{CC} = AV _{RH} = 5.5 V A/D Converter not operated	-	5	0.02	0.23	0.02	0.28	μA	
Reference voltage current	I _R	AV _{RH} / AV _{RL}	V _{CC} = AV _{CC} = AV _{RH} = 5.5 V A/D Converter active	-	1	0.66	0.72	0.58	0.73	mA	
	I _{RH}	AV _{RH} / AV _{RL}	V _{CC} = AV _{CC} = AV _{RH} = 5.5 V A/D Converter not operated	-	5	0.02	0.12	0.02	0.16	μA	

5.0 AC Characterization

5.1 AC Characterization Summary

A/D Converter

Parameter	Symbol	Pin Name	Conditions	Datasheet		Measured				Unit
				Min	Max	Current Fab		Fab25		
						Min	Max	Min	Max	
Nonlinearity error	-	ANn	$V_{CC} = AV_{CC} = AVR_H = 3.0\text{ V}$	-2.5	+2.5	-0.77	0.41	-0.86	0.50	LSB
Differential nonlinearity error	-	ANn	$V_{CC} = AV_{CC} = AVR_H = 3.0\text{ V}$	-1.9	+1.9	-0.55	0.62	-0.63	0.63	LSB
Zero reading voltage	V_{OT}	ANn	$V_{CC} = AV_{CC} = AVR_H = 3.0\text{ V}$	AVRL -1.5 LSB	AVRL +2.5 LSB	AVRL +0.25 LSB	AVRL +0.66 LSB	AVRL +0.37 LSB	AVRL +0.88 LSB	V
Full scale reading voltage	V_{FST}	ANn	$V_{CC} = AV_{CC} = AVR_H = 3.0\text{ V}$	AVRH -3.5 LSB	AVRH +0.5 LSB	AVRH -1.88 LSB	AVRH -1.00 LSB	AVRH -1.75 LSB	AVRH -1.38 LSB	V

Document History Page

Rev.	ECN No.	Orig. of Change	Description of Change
**	6269831	YAKU	New Characterization Report.

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F²MC-16FX, CY96340 Series, 16-bit Proprietary Microcontroller Datasheet

CY96340 series is based on Cypress advanced 16FX architecture (16-bit with instruction pipeline for RISC-like performance). The CPU uses the same instruction set as the established 16LX series - thus allowing for easy migration of 16LX Software to the new 16FX products. 16FX improvements compared to the previous generation include significantly improved performance - even at the same operation frequency, reduced power consumption and faster start-up time.

For highest processing speed at optimized power consumption an internal PLL can be selected to supply the CPU with up to 56MHz operation frequency from an external 4MHz resonator. The result is a minimum instruction cycle time of 17.8ns going together with excellent EMI behavior. An on-chip clock modulation circuit significantly reduces emission peaks in the frequency spectrum. The emitted power is minimized by the on-chip voltage regulator that reduces the internal CPU voltage. A flexible clock tree allows to select suitable operation frequencies for peripheral resources independent of the CPU speed.

Features

Technology

- 0.18µm CMOS

CPU

- F²MC-16FX CPU
- Up to 56 MHz internal, 17.8 ns instruction cycle time
- Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers)
- 8-byte instruction execution queue
- Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available

System clock

- On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop)
- 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor).
- Up to 56 MHz external clock for devices with fast clock input feature
- 32-100 kHz subsystem quartz clock
- 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog
- Clock source selectable from main- and subclock oscillator (part number suffix "W") and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals.
- Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode)
- Clock modulator

On-chip voltage regulator

- Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures

Low voltage reset

- Reset is generated when supply voltage is below minimum

Code Security

- Protects ROM content from unintended read-out

Memory Patch Function

- Replaces ROM content

- Can also be used to implement embedded debug support

DMA

- Automatic transfer function independent of CPU, can be assigned freely to resources

Interrupts

- Fast Interrupt processing
- 8 programmable priority levels
- Non-Maskable Interrupt (NMI)

Timers

- Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Watchdog Timer

CAN

- Supports CAN protocol version 2.0 part A and B
- ISO16845 certified
- Bit rates up to 1 Mbit/s
- 32 message objects
- Each message object has its own identifier mask
- Programmable FIFO mode (concatenation of message objects)
- Maskable interrupt
- Disabled Automatic Retransmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation

USART

- Full duplex USARTs (SCI/LIN)
- Wide range of baud rate settings using a dedicated reload timer
- Special synchronous options for adapting to different synchronous serial protocols
- LIN functionality working either as master or slave LIN device

I²C

- Up to 400 kbps
- Master and Slave functionality, 8-bit and 10-bit addressing

A/D converter

- SAR-type
- 10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer

A/D Converter Reference Voltage switch

- 2 independent positive A/D converter reference voltages available

Reload Timers

- 16-bit wide
- Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
- Event count function

Free Running Timers

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1 , $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency

Input Capture Units

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, falling edge or rising & falling edge sensitive

Output Compare Units

- 16-bit wide
- Signals an interrupt when a match with 16-bit I/O Timer occurs
- A pair of compare registers can be used to generate an output signal.

Programmable Pulse Generator

- 16-bit down counter, cycle and duty setting registers
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows 1 , $1/4$, $1/16$, $1/64$ of peripheral clock as counter clock and Reload timer overflow as clock input
- Can be triggered by software or reload timer

Real Time Clock

- Can be clocked either from sub oscillator (devices with part number suffix "W"), main oscillator or from the RC oscillator
- Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

External Interrupts

- Edge sensitive or level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

Non Maskable Interrupt

- Disabled after reset

- Once enabled, can not be disabled other than by reset.
- Level high or level low sensitive
- Pin shared with external interrupt 0.

External bus interface

- 8-bit or 16-bit bidirectional data
- Up to 24-bit addresses
- 6 chip select signals
- Multiplexed address/data lines
- Wait state request
- External bus master possible
- Timing programmable

Alarm comparator

- Monitors an external voltage and generates an interrupt in case of a voltage lower or higher than the defined thresholds
- Threshold voltages defined externally or generated internally
- Status is readable, interrupts can be masked separately

I/O Ports

- Virtually all external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL (TTL levels not supported by all devices)
- Bit-wise programmable pull-up resistor
- Bit-wise programmable output driving strength for EMI optimization

Packages

- 100-pin plastic QFP and LQFP

Flash Memory

- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Number of erase cycles: 10,000 times
- Data retention time: 20 years
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

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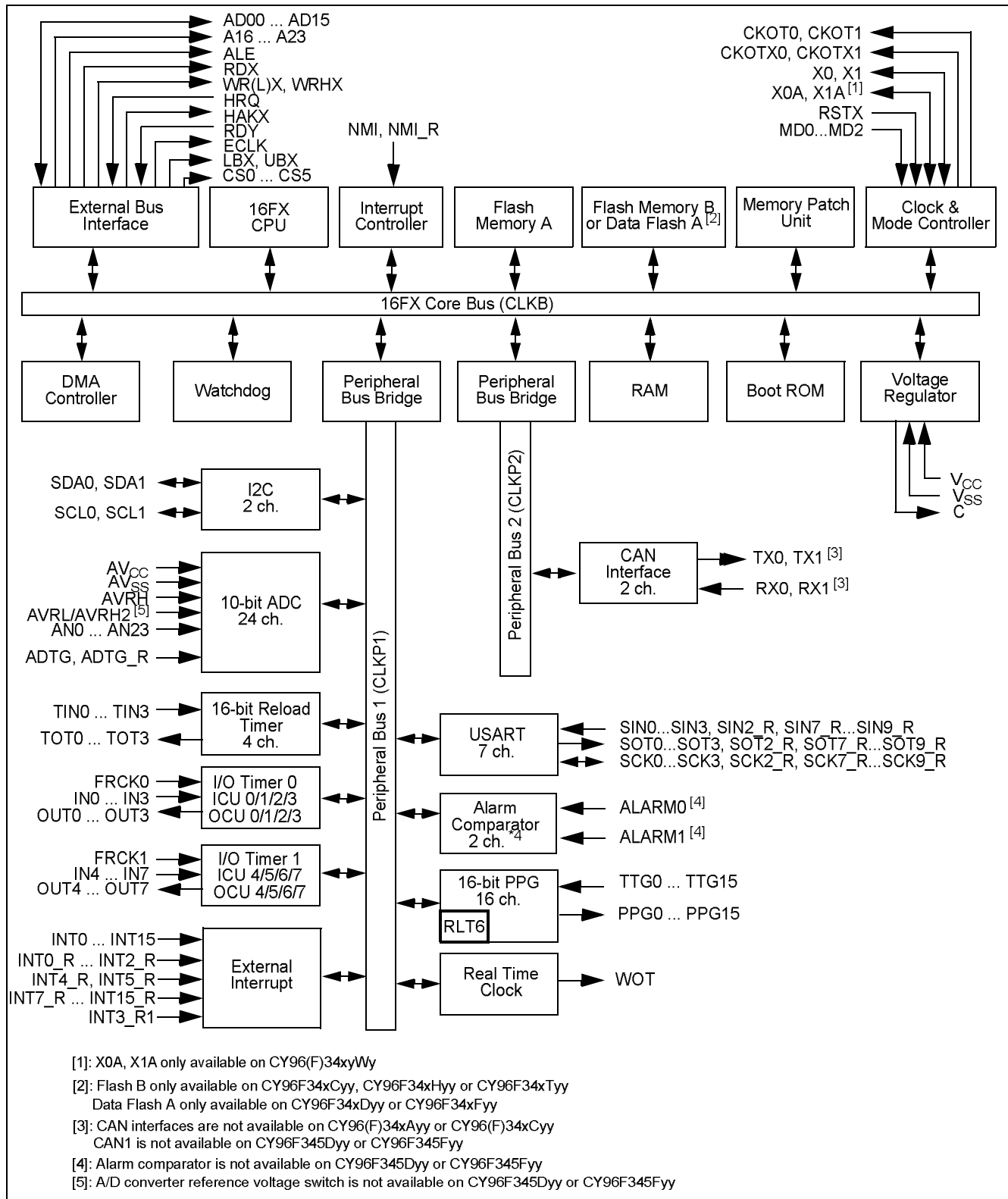
1. Product Lineup

Features		CY96V300B	CY96(F)34x
Product type		Evaluation sample	Flash product: CY96F34x Mask ROM product: CY9634x
Product options			
YS		NA	Low voltage reset persistently on / Single clock
RS			Low voltage reset can be disabled / Single clock
YW			Low voltage reset persistently on / Dual clock
RW			Low voltage reset can be disabled / Dual clock
TS			indep. 32KB Flash / Low voltage reset persistently on / Single clock
HS			indep. 32KB Flash / Low voltage reset can be disabled / Single clock
TW			indep. 32KB Flash / Low voltage reset persistently on / Dual clock
HW			indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
FS			64KB Data Flash / Low voltage reset persistently on / Single clock
DS			64KB Data Flash / Low voltage reset can be disabled / Single clock
FW			64KB Data Flash / Low voltage reset persistently on / Dual clock
DW			64KB Data Flash / Low voltage reset can be disabled / Dual clock
AS			No CAN / Low voltage reset can be disabled / Single clock devices
CS			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Single clock
AW			No CAN / Low voltage reset can be disabled / Dual clock
CW			No CAN / indep. 32KB Flash / Low voltage reset can be disabled / Dual clock
Flash/ROM	RAM		
160KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	CY96345Y, CY96345R
224KB [Flash A: 160KB, Data Flash A: 64KB]	8KB		CY96F345F, CY96F345D
288KB	16KB		CY96F346Y, CY96346Y, CY96F346R, CY96346R, CY96F346A
416KB	16KB		CY96F347Y, CY96F347R, CY96F347A
544KB	24KB		CY96F348Y, CY96F348R, CY96F348A
576KB [Flash A: 544KB, Flash B: 32KB]	24KB		CY96F348T, CY96F348H, CY96F348C
Package		BGA416	LQI100 PQH100
DMA		16 channels	6 channels
USART		10 channels	7 channels

Features	CY96V300B	CY96(F)34x
I ² C	2 channels	2 channels
A/D Converter	40 channels	24 channels
A/D Converter Reference Voltage switch	yes	yes (except CY96F345Dyy or CY96F345Fyy)
16-bit Reload Timer	6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer	4 channels	2 channels
16-bit Output Compare	12 channels	8 channels
16-bit Input Capture	12 channels	8 channels
16-bit Programmable Pulse Generator	20 channels	16 channels
CAN Interface	5 channels	CY96(F)34xAyy or CY96(F)34xCyy: no CY96F345Dyy or CY96F345Fyy: 1 channel others: 2 channels
External Interrupts	16 channels	
Non-Maskable Interrupt	1 channel	
Real Time Clock	1	
I/O Ports	136	80 for part number with suffix "W", 82 for part number with suffix "S"
Alarm comparator	2 channels	CY96F345Dyy or CY96F345Fyy: no others: 2 channels
External bus interface	Yes	Yes (multiplexed address/data)
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

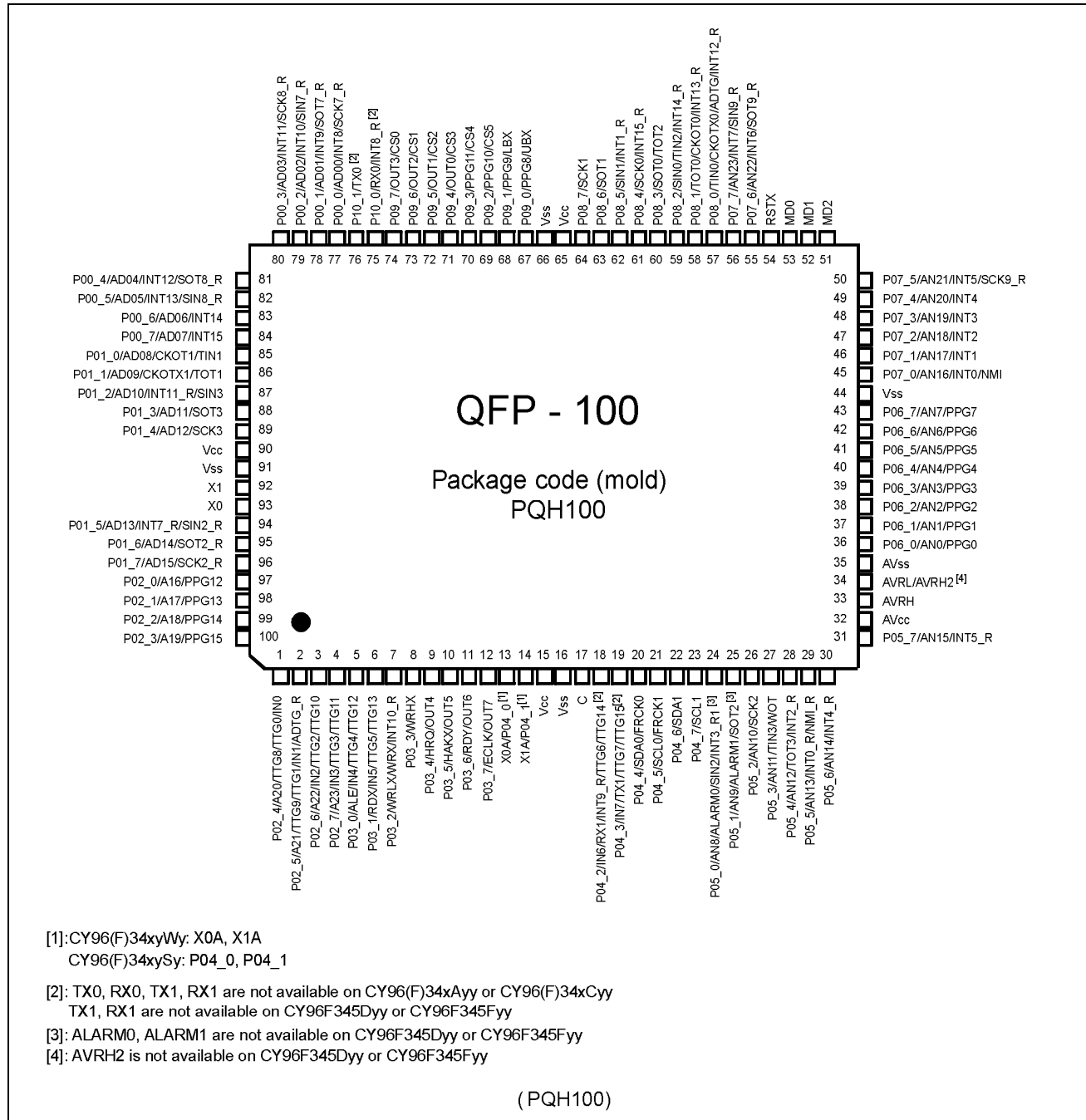
2. Block Diagram

Figure 1. Block diagram of CY96(F)34x



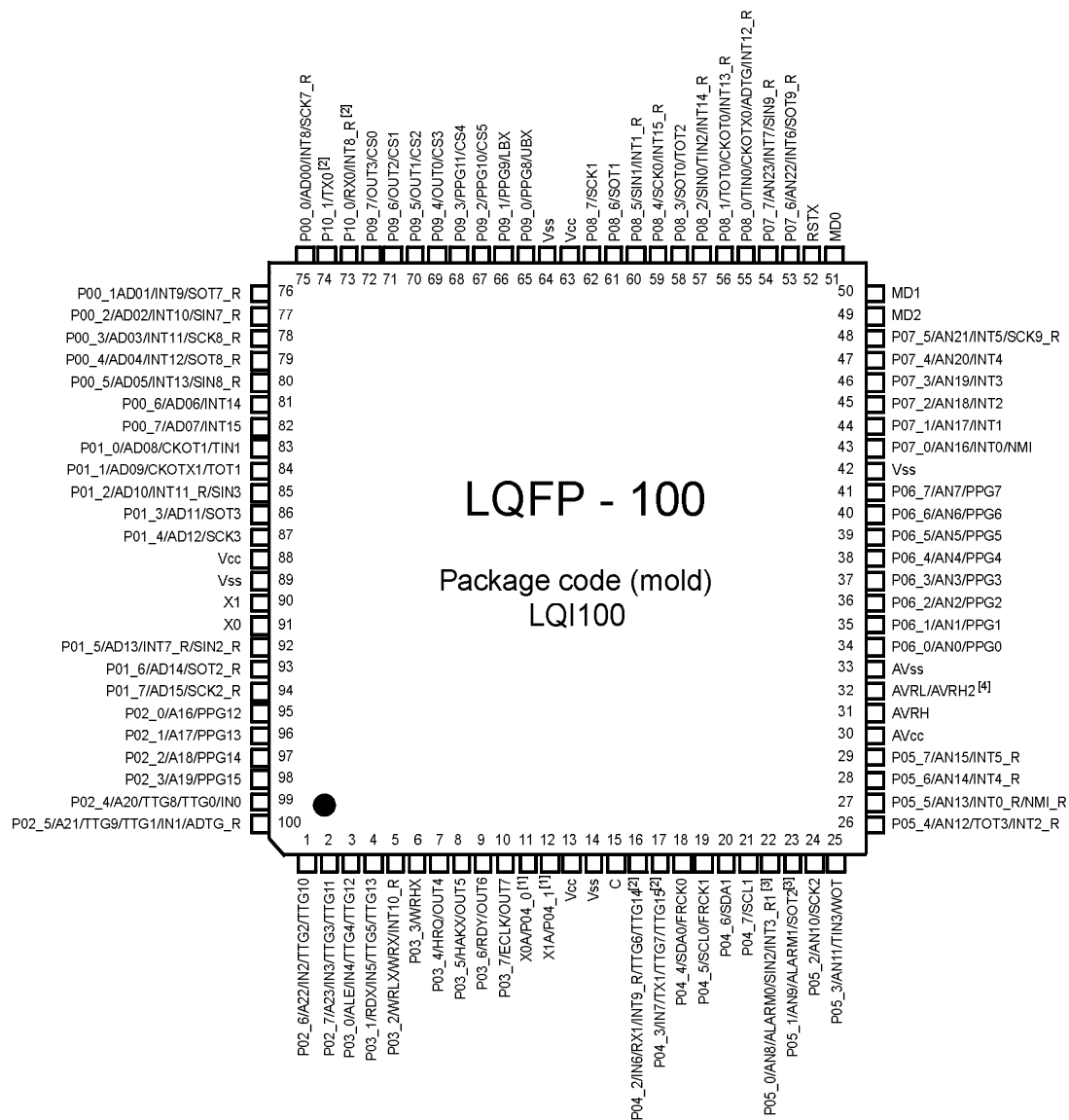
3. Pin Assignments

Figure 2. Pin assignment of CY96(F)34x (PQH100)



Remark:

CY96(F)34x products are pin-compatible to F²MC-16LX family CY90340 series.

Figure 3. Pin assignment of CY96(F)34x (LQ100)


4. Pin Function Description

Table 1: Pin Function description

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG	ADC	A/D converter trigger input
ADTG_R	ADC	Relocated A/D converter trigger input
ALARMn	Alarm comparator	Alarm Comparator n input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV _{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AVRH2	ADC	Alternative A/D converter high reference voltage input
AVRL	ADC	A/D converter low reference voltage input
AV _{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn	External bus	External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
LBX	External bus	External Bus Interface Lower Byte select strobe output
MDn	Core	Input pins for specifying the operating mode.
NMI	External Interrupt	Non-Maskable Interrupt input
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output

Table 1: Pin Function description

Pin name	Feature	Description
RDY	External bus	External bus interface external wait state request input
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I ² C interface n clock I/O input/output
SDAn	I2C	I ² C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
UBX	External bus	External Bus Interface Upper Byte select strobe output
V _{CC}	Supply	Power supply
V _{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

5. Pin Circuit Type

Table 2: Pin circuit types

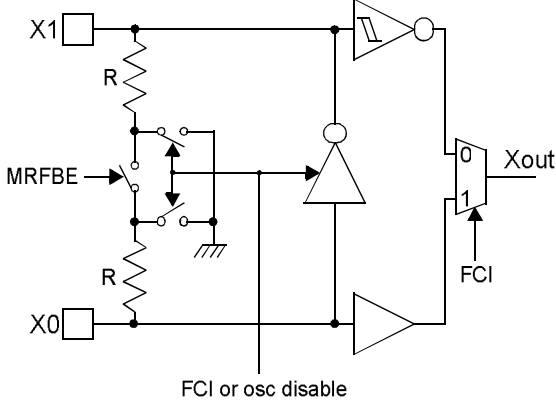
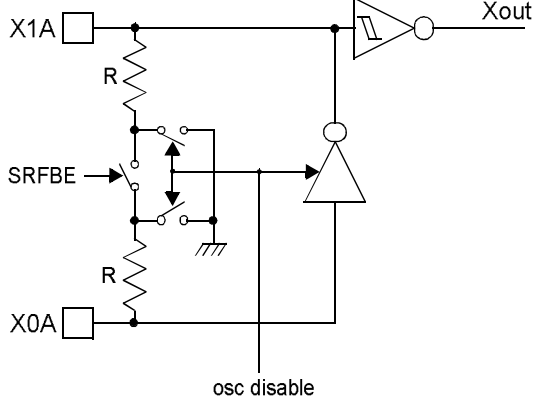
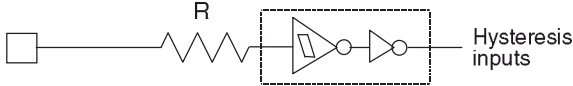
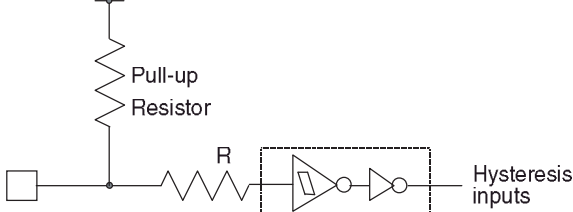
LQI100		PQH100	
Pin no.	Circuit type ^[1]	Pin no.	Circuit type ^[1]
1-10	H	1-12	H
11,12	B ^[2]	13, 14	B ^[2]
11,12	H ^[3]	13, 14	H ^[3]
13,14	Supply	15,16	Supply
15	F	17	F
16,17	H	18,19	H
18-21	N	20-23	N
22-29	I	24-31	I
30	Supply	32	Supply
31-32	G	33-34	G
33	Supply	35	Supply
34 to 41	I	36 to 43	I
42	Supply	44	Supply
43 to 48	I	45 to 50	I
49 to 51	C	51 to 53	C
52	E	54	E
53 to 54	I	55 to 56	I
55 to 62	H	57 to 64	H
63, 64	Supply	65, 66	Supply
65 to 87	H	67 to 89	H
88,89	Supply	90, 91	Supply
90, 91	A	92, 93	A
92-100	H	94 to 100	H

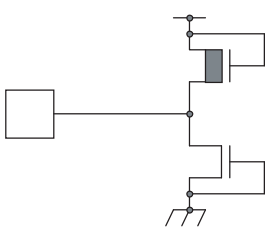
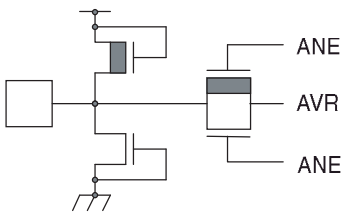
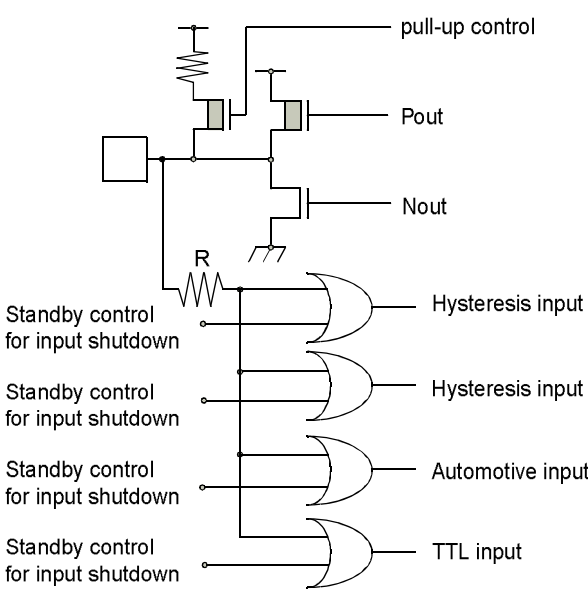
[1]: Please refer to “[I/O Circuit Type](#)” for details on the I/O circuit types

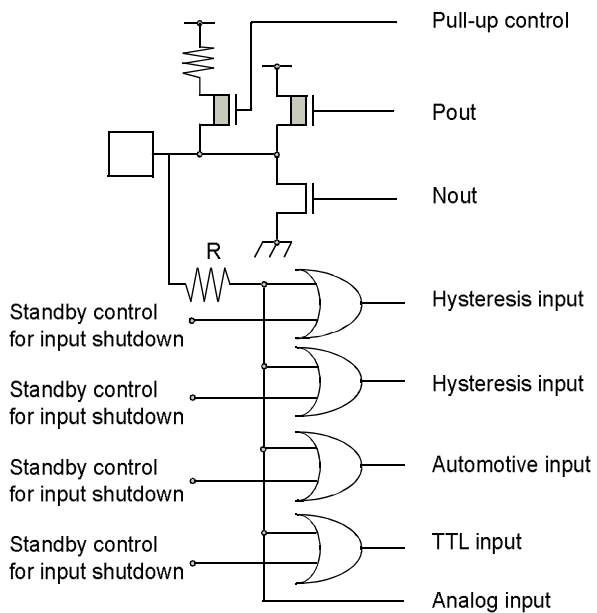
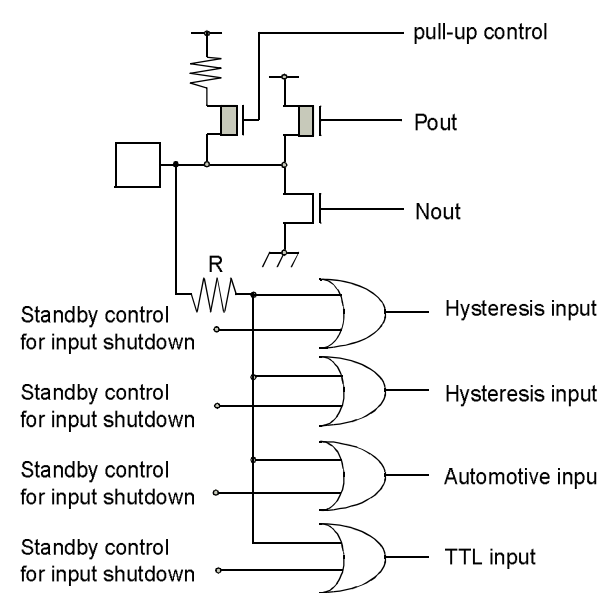
[2]: Devices with suffix “W”

[3]: Devices without suffix “W”

6. I/O Circuit Type

Type	Circuit	Remarks
A		<p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> ■ Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) ■ Programmable feedback resistor = approx. $2 * 0.5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		<p>Low-speed oscillation circuit:</p> <ul style="list-style-type: none"> ■ Programmable feedback resistor = approx. $2 * 5 \text{ M}\Omega$. Feedback resistor is grounded in the center when the oscillator is disabled
C		<ul style="list-style-type: none"> ■ Mask ROM and EVA device: CMOS Hysteresis input pin ■ Flash device: CMOS input pin
E		<ul style="list-style-type: none"> ■ CMOS Hysteresis input pin ■ Pull-up resistor value: approx. $50 \text{ k}\Omega$

Type	Circuit	Remarks
F		<ul style="list-style-type: none"> ■ Power supply input protection circuit
G		<ul style="list-style-type: none"> ■ A/D converter ref+ (AVRH/AVRH2) power supply input pin with protection circuit ■ Flash devices do not have a protection circuit against VCC for pins AVRH/AVRH2 ■ Devices without AVRH reference switch do not have an analog switch for the AVRL pin
H		<ul style="list-style-type: none"> ■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. <p>*CY96F345Dyy or CY96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported</p>

Type	Circuit	Remarks
I	 <p>Pull-up control</p> <p>Pout</p> <p>Nout</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Hysteresis input</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>TTL input</p> <p>Analog input</p>	<ul style="list-style-type: none"> ■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$ and $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. ■ Analog input <p>*CY96F345Dyy or CY96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported</p>
N	 <p>pull-up control</p> <p>Pout</p> <p>Nout</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Hysteresis input</p> <p>Hysteresis input</p> <p>Automotive input</p> <p>TTL input</p>	<ul style="list-style-type: none"> ■ CMOS level output ($I_{OL} = 3\text{mA}$, $I_{OH} = -3\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function * ■ Automotive input with input shutdown function ■ TTL input with input shutdown function * ■ Programmable pull-up resistor: 50kΩ approx. <p>*CY96F345Dyy or CY96F345Fyy: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported</p>

7. Memory Map

	CY96V300B		CY96(F)34x	
FF:FFF _H	Emulation ROM		USER ROM / External Bus ^[4]	
DE:000 _H				
	External Bus		External Bus	
10:000 _H				
0F:E00 _H	Boot-ROM		Boot-ROM	
	Reserved	0F:000 _H	Reserved	
0E:000 _H			DATA FLASH / Reserved ^[4]	
	External RAM	0C:000 _H		
02:000 _H			Reserved	
	Internal RAM bank 1	RAMEND ^[2] RAMSTART ^[2]	Internal RAM bank 1	RAM availability depending on the device
01:000 _H			Reserved	
	ROM/RAM MIRROR		ROM/RAM MIRROR	
00:800 _H				
	Internal RAM bank 0	RAMSTART ^[2]	Internal RAM bank 0	
			Reserved	
RAMSTART ^[3]			External Bus	External Bus end address ^[2]
00:0C0 _H	External Bus			
	Peripherals		Peripherals	
00:038 _H				
00:018 _H	GPR ^[1]		GPR ^[1]	
00:010 _H	DMA		DMA	
00:00F _H	External Bus		External Bus	
00:000 _H	Peripheral		Peripheral	

[1]: Unused GPR banks can be used as RAM area

[2]: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

[3]: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

[4]: For details about USER ROM area or DATA FLASH area, see the [User ROM Memory Map For Flash Devices](#) and [User ROM Memory Map for Mask ROM Devices](#) on the following pages.

The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ RAM Start/End and External Bus End Addresses

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
CY96(F)345	8KByte	-	00:21FF _H	00:6240 _H	-	-
CY96(F)346, CY96F347	16KByte	-	00:21FF _H	00:4240 _H	-	-
CY96F348	24KByte	-	00:21FF _H	00:2240 _H	-	-

8. User ROM Memory Map For Flash Devices

CY96F345D CY96F345F				
Alternative mode CPU address	Flash memory mode address	Flash size 160kByte +64KByte Data Flash		
FF:FFFF _H	3F:FFFF _H	S39 - 64K	Flash A	
FF:0000 _H	3F:0000 _H	S38 - 64K		
FE:FFFF _H	3E:FFFF _H	External bus		
FE:0000 _H	3E:0000 _H			
FD:FFFF _H	3D:FFFF _H			
FD:0000 _H	3D:0000 _H			
FC:FFFF _H	3C:FFFF _H			
FC:0000 _H	3C:0000 _H			
FB:FFFF _H	3B:FFFF _H			
FB:0000 _H	3B:0000 _H			
FA:FFFF _H	3A:FFFF _H			
FA:0000 _H	3A:0000 _H			
F9:FFFF _H	39:FFFF _H			
F9:0000 _H	39:0000 _H			
F8:FFFF _H	38:FFFF _H			
F8:0000 _H	38:0000 _H			
F7:FFFF _H	37:FFFF _H			
F7:0000 _H	37:0000 _H			
F6:FFFF _H	36:FFFF _H			
F6:0000 _H	36:0000 _H			
F5:FFFF _H	35:FFFF _H			
F5:0000 _H	35:0000 _H			
F4:FFFF _H	34:FFFF _H			
F4:0000 _H	34:0000 _H			
F3:FFFF _H	33:FFFF _H			
F3:0000 _H	33:0000 _H			
F2:FFFF _H	32:FFFF _H			
F2:0000 _H	32:0000 _H			
F1:FFFF _H	31:FFFF _H			
F1:0000 _H	31:0000 _H			
F0:FFFF _H	30:FFFF _H			
F0:0000 _H	30:0000 _H			
E0:FFFF _H		Reserved		
E0:0000 _H				
DF:FFFF _H		Reserved		
DF:8000 _H				
DF:7FFF _H	1F:7FFF _H	SA3 - 8K	Flash A	
DF:6000 _H	1F:6000 _H	SA2 - 8K		
DF:5FFF _H	1F:5FFF _H			
DF:4000 _H	1F:4000 _H	SA1 - 8K		
DF:3FFF _H	1F:3FFF _H			
DF:2000 _H	1F:2000 _H	SA0 - 8K ^[1]		
DF:1FFF _H	1F:1FFF _H			
DF:0000 _H	1F:0000 _H	Reserved		
DE:FFFF _H				
DE:0000 _H				
0E:FFFF _H	(0E:FFFF _H)	SDA0-256 ^[2]	Data Flash A	
0E:FF00 _H	(0E:FF00 _H)	Reserved		
0E:FEFF _H				
0E:0000 _H		Data Flash A		
0D:FFFF _H	(0F:FFFF _H)			SDA4-16K
0D:C000 _H	(0F:C000 _H)			SDA3-16K
0D:BFFF _H	(0F:BFFF _H)			
0D:8000 _H	(0F:8000 _H)			SDA2-16K
0D:7FFF _H	(0F:7FFF _H)			
0D:4000 _H	(0F:4000 _H)			SDA1-16K
0D:3FFF _H	(0F:3FFF _H)			
0D:0000 _H	(0F:0000 _H)	Reserved		
0C:FFFF _H				
0C:0000 _H				

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBA at CPU address DE:FF00_H - DE:FF2F_H

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SDA0 contains the ROM Configuration Block RCBDA at CPU address DE:FF00_H - DE:FF2F_H

		CY96F346Y CY96F346R CY96F346A		CY96F347Y CY96F347R CY96F347A	
Alternative mode CPU address	Flash memory mode address	Flash size 288kByte		Flash size 416kByte	
FF:FFF _H	3F:FFF _H	S39 - 64K		S39 - 64K	Flash A
FF:000 _H	3F:000 _H	S38 - 64K		S38 - 64K	
FE:FFF _H	3E:FFF _H			S37 - 64K	
FE:000 _H	3E:000 _H	S37 - 64K		S36 - 64K	
FD:FFF _H	3D:FFF _H			S35 - 64K	
FD:000 _H	3D:000 _H	S36 - 64K		S34 - 64K	
FC:FFF _H	3C:FFF _H				
FC:000 _H	3C:000 _H				
FB:FFF _H	3B:FFF _H				
FB:000 _H	3B:000 _H				
FA:FFF _H	3A:FFF _H	External bus			Flash A
FA:000 _H	3A:000 _H				
F9:FFF _H	39:FFF _H				
F9:000 _H	39:000 _H				
F8:FFF _H	38:FFF _H				
F8:000 _H	38:000 _H				
F7:FFF _H	37:FFF _H				
F7:000 _H	37:000 _H				
F6:FFF _H	36:FFF _H				
F6:000 _H	36:000 _H				
F5:FFF _H	35:FFF _H				
F5:000 _H	35:000 _H				
F4:FFF _H	34:FFF _H				
F4:000 _H	34:000 _H				
F3:FFF _H	33:FFF _H				
F3:000 _H	33:000 _H				
F2:FFF _H	32:FFF _H	External bus			
F2:000 _H	32:000 _H				
F1:FFF _H	31:FFF _H				
F1:000 _H	31:000 _H				
F0:FFF _H	30:FFF _H				
F0:000 _H	30:000 _H				
E0:FFF _H					
E0:000 _H					
DF:FFF _H		Reserved		Reserved	
DF:800 _H					
DF:7FF _H	1F:7FF _H	SA3 - 8K		SA3 - 8K	Flash A
DF:600 _H	1F:600 _H				
DF:5FF _H	1F:5FF _H	SA2 - 8K		SA2 - 8K	
DF:400 _H	1F:400 _H				
DF:3FF _H	1F:3FF _H	SA1 - 8K		SA1 - 8K	
DF:200 _H	1F:200 _H				
DF:1FF _H	1F:1FF _H	SA0 - 8K ^[1]		SA0 - 8K ^[1]	
DF:000 _H	1F:000 _H				
DE:FFF _H		Reserved		Reserved	
DE:000 _H					

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

		CY96F348Y CY96F348R CY96F348A		CY96F348T CY96F348H CY96F348C	
Alternative mode CPU address	Flash memory mode address	Flash size 544kByte		Flash size 576kByte	
FF:FFFF _H FF:0000 _H	3F:FFFF _H 3F:0000 _H	S39 - 64K		S39 - 64K	Flash A
FE:FFFF _H FE:0000 _H	3E:FFFF _H 3E:0000 _H	S38 - 64K		S38 - 64K	
FD:FFFF _H FD:0000 _H	3D:FFFF _H 3D:0000 _H	S37 - 64K		S37 - 64K	
FC:FFFF _H FC:0000 _H	3C:FFFF _H 3C:0000 _H	S36 - 64K		S36 - 64K	
FB:FFFF _H FB:0000 _H	3B:FFFF _H 3B:0000 _H	S35 - 64K		S35 - 64K	
FA:FFFF _H FA:0000 _H	3A:FFFF _H 3A:0000 _H	S34 - 64K		S34 - 64K	
F9:FFFF _H F9:0000 _H	39:FFFF _H 39:0000 _H	S33 - 64K		S33 - 64K	
F8:FFFF _H F8:0000 _H	38:FFFF _H 38:0000 _H	S32 - 64K		S32 - 64K	
F7:FFFF _H F7:0000 _H	37:FFFF _H 37:0000 _H	External bus		External bus	
F6:FFFF _H F6:0000 _H	36:FFFF _H 36:0000 _H				
F5:FFFF _H F5:0000 _H	35:FFFF _H 35:0000 _H				
F4:FFFF _H F4:0000 _H	34:FFFF _H 34:0000 _H				
F3:FFFF _H F3:0000 _H	33:FFFF _H 33:0000 _H				
F2:FFFF _H F2:0000 _H	32:FFFF _H 32:0000 _H				
F1:FFFF _H F1:0000 _H	31:FFFF _H 31:0000 _H				
F0:FFFF _H F0:0000 _H	30:FFFF _H 30:0000 _H				
E0:FFFF _H E0:0000 _H					
DF:FFFF _H DF:8000 _H		Reserved		Reserved	
DF:7FFF _H DF:6000 _H	1F:7FFF _H 1F:6000 _H	SA3 - 8K		SA3 - 8K	Flash A
DF:5FFF _H DF:4000 _H	1F:5FFF _H 1F:4000 _H	SA2 - 8K		SA2 - 8K	
DF:3FFF _H DF:2000 _H	1F:3FFF _H 1F:2000 _H	SA1 - 8K		SA1 - 8K	
DF:1FFF _H DF:0000 _H	1F:1FFF _H 1F:0000 _H	SA0 - 8K ^[1]		SA0 - 8K ^[1]	
DE:FFFF _H DE:8000 _H		Reserved		Reserved	Flash B
DE:7FFF _H DE:6000 _H	1E:7FFF _H 1E:6000 _H			SB3 - 8K	
DE:5FFF _H DE:4000 _H	1E:5FFF _H 1E:4000 _H			SB2 - 8K	
DE:3FFF _H DE:2000 _H	1E:3FFF _H 1E:2000 _H			SB1 - 8K	
DE:1FFF _H DE:0000 _H	1E:1FFF _H 1E:0000 _H			SB0 - 8K ^[2]	

[1]: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000_H - DF:007F_H

[2]: Sector SB0 contains the ROM Configuration Block RCBB at CPU address DE:0000_H - DE:002F_H

9. User ROM Memory Map for Mask ROM Devices

	CY96345	CY96346
CPU address	ROM size 160kByte	ROM size 288kByte
FF:FFF _H FF:000 _H	128K ROM	256K ROM
FE:FFF _H FE:000 _H		
FD:FFF _H FD:000 _H	Reserved	
FC:FFF _H FC:000 _H		
FB:FFF _H E0:000 _H	External bus	External bus
DF:FFF _H DF:800 _H	Reserved	Reserved
DF:7FF _H DF:008 _H	32K ROM	32K ROM
DF:007F _H DF:000 _H	ROM configuration block RCB	ROM configuration block RCB
DE:FFF _H DE:000 _H	Reserved	Reserved

10. Serial Programming Communication Interface

Table 3: USART pins for Flash serial programming (MD[2:0] = 010, Serial Communication mode)

CY96F34x			
Pin number	Pin number	USART Number	Normal function
LQFP-100	QFP-100		
57	59	USART0	SIN0
58	60		SOT0
59	61		SCK0
60	62	USART1	SIN1
61	63		SOT1
62	64		SCK1
22	24	USART2	SIN2
23	25		SOT2
24	26		SCK2
85	87	USART3	SIN3
86	88		SOT3
87	89		SCK3

Note: If a Flash programmer and its software needs to use a handshaking pin, Cypress suggests to the tool vendor to support at least port P00_1 on pin 76/78. If handshaking is used by the tool but P00_1 is not available in customer's application, Cypress suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

11. I/O Map

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000 _H	I/O Port P00 - Port Data Register	PDR00		R/W
000001 _H	I/O Port P01 - Port Data Register	PDR01		R/W
000002 _H	I/O Port P02 - Port Data Register	PDR02		R/W
000003 _H	I/O Port P03 - Port Data Register	PDR03		R/W
000004 _H	I/O Port P04 - Port Data Register	PDR04		R/W
000005 _H	I/O Port P05 - Port Data Register	PDR05		R/W
000006 _H	I/O Port P06 - Port Data Register	PDR06		R/W
000007 _H	I/O Port P07 - Port Data Register	PDR07		R/W
000008 _H	I/O Port P08 - Port Data Register	PDR08		R/W
000009 _H	I/O Port P09 - Port Data Register	PDR09		R/W
00000A _H	I/O Port P10 - Port Data Register	PDR10		R/W
00000B _H -000017 _H	Reserved			-
000018 _H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019 _H	ADC0 - Control Status register High	ADCSH		R/W
00001A _H	ADC0 - Data Register Low	ADCRL	ADCR	R
00001B _H	ADC0 - Data Register High	ADCRH		R
00001C _H	ADC0 - Setting Register		ADSR	R/W
00001D _H	ADC0 - Setting Register			R/W
00001E _H	ADC0 - Extended Configuration Register	ADECR		R/W
00001F _H	Reserved			-
000020 _H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021 _H	FRT0 - Data register of free-running timer			R/W
000022 _H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023 _H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024 _H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025 _H	FRT1 - Data register of free-running timer			R/W
000026 _H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027 _H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028 _H	OCU0 - Output Compare Control Status	OCS0		R/W
000029 _H	OCU1 - Output Compare Control Status	OCS1		R/W
00002A _H	OCU0 - Compare Register		OCCP0	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00002B _H	OCU0 - Compare Register			R/W
00002C _H	OCU1 - Compare Register		OCCP1	R/W
00002D _H	OCU1 - Compare Register			R/W
00002E _H	OCU2 - Output Compare Control Status	OCS2		R/W
00002F _H	OCU3 - Output Compare Control Status	OCS3		R/W
000030 _H	OCU2 - Compare Register		OCCP2	R/W
000031 _H	OCU2 - Compare Register			R/W
000032 _H	OCU3 - Compare Register		OCCP3	R/W
000033 _H	OCU3 - Compare Register			R/W
000034 _H	OCU4 - Output Compare Control Status	OCS4		R/W
000035 _H	OCU5 - Output Compare Control Status	OCS5		R/W
000036 _H	OCU4 - Compare Register		OCCP4	R/W
000037 _H	OCU4 - Compare Register			R/W
000038 _H	OCU5 - Compare Register		OCCP5	R/W
000039 _H	OCU5 - Compare Register			R/W
00003A _H	OCU6 - Output Compare Control Status	OCS6		R/W
00003B _H	OCU7 - Output Compare Control Status	OCS7		R/W
00003C _H	OCU6 - Compare Register		OCCP6	R/W
00003D _H	OCU6 - Compare Register			R/W
00003E _H	OCU7 - Compare Register		OCCP7	R/W
00003F _H	OCU7 - Compare Register			R/W
000040 _H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041 _H	ICU0/ICU1 - Edge register	ICE01		R/W
000042 _H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043 _H	ICU0 - Capture Register High	IPCPL0		R
000044 _H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045 _H	ICU1 - Capture Register High	IPCPL1		R
000046 _H	ICU2/ICU3 - Control Status Register	ICS23		R/W
000047 _H	ICU2/ICU3 - Edge register	ICE23		R/W
000048 _H	ICU2 - Capture Register Low	IPCPL2	IPCP2	R
000049 _H	ICU2 - Capture Register High	IPCPL2		R
00004A _H	ICU3 - Capture Register Low	IPCPL3	IPCP3	R
00004B _H	ICU3 - Capture Register High	IPCPL3		R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00004C _H	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004D _H	ICU4/ICU5 - Edge register	ICE45		R/W
00004E _H	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004F _H	ICU4 - Capture Register High	IPCPH4		R
000050 _H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051 _H	ICU5 - Capture Register High	IPCPH5		R
000052 _H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053 _H	ICU6/ICU7 - Edge register	ICE67		R/W
000054 _H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055 _H	ICU6 - Capture Register High	IPCPH6		R
000056 _H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057 _H	ICU7 - Capture Register High	IPCPH7		R
000058 _H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059 _H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
00005A _H	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005B _H	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
00005C _H	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
00005D _H	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
00005E _H	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
00005F _H	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060 _H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061 _H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062 _H	RLT0 - Reload Register - for writing		TMRLR0	W
000062 _H	RLT0 - Reload Register - for reading		TMR0	R
000063 _H	RLT0 - Reload Register - for writing			W
000063 _H	RLT0 - Reload Register - for reading			R
000064 _H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065 _H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066 _H	RLT1 - Reload Register - for writing		TMRLR1	W
000066 _H	RLT1 - Reload Register - for reading		TMR1	R
000067 _H	RLT1 - Reload Register - for writing			W
000067 _H	RLT1 - Reload Register - for reading			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000068 _H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069 _H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
00006A _H	RLT2 - Reload Register - for writing		TMRLR2	W
00006A _H	RLT2 - Reload Register - for reading		TMR2	R
00006B _H	RLT2 - Reload Register - for writing			W
00006B _H	RLT2 - Reload Register - for reading			R
00006C _H	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W
00006D _H	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E _H	RLT3 - Reload Register - for writing		TMRLR3	W
00006E _H	RLT3 - Reload Register - for reading		TMR3	R
00006F _H	RLT3 - Reload Register - for writing			W
00006F _H	RLT3 - Reload Register - for reading			R
000070 _H	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071 _H	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073 _H	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074 _H	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075 _H	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076 _H	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077 _H	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078 _H	PPG0 - Timer register		PTMR0	R
000079 _H	PPG0 - Timer register			R
00007A _H	PPG0 - Period setting register		PCSR0	W
00007B _H	PPG0 - Period setting register			W
00007C _H	PPG0 - Duty cycle register		PDUT0	W
00007D _H	PPG0 - Duty cycle register			W
00007E _H	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F _H	PPG0 - Control status register High	PCNH0		R/W
000080 _H	PPG1 - Timer register		PTMR1	R
000081 _H	PPG1 - Timer register			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000082 _H	PPG1 - Period setting register		PCSR1	W
000083 _H	PPG1 - Period setting register			W
000084 _H	PPG1 - Duty cycle register		PDUT1	W
000085 _H	PPG1 - Duty cycle register			W
000086 _H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087 _H	PPG1 - Control status register High	PCNH1		R/W
000088 _H	PPG2 - Timer register		PTMR2	R
000089 _H	PPG2 - Timer register			R
00008A _H	PPG2 - Period setting register		PCSR2	W
00008B _H	PPG2 - Period setting register			W
00008C _H	PPG2 - Duty cycle register		PDUT2	W
00008D _H	PPG2 - Duty cycle register			W
00008E _H	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008F _H	PPG2 - Control status register High	PCNH2		R/W
000090 _H	PPG3 - Timer register		PTMR3	R
000091 _H	PPG3 - Timer register			R
000092 _H	PPG3 - Period setting register		PCSR3	W
000093 _H	PPG3 - Period setting register			W
000094 _H	PPG3 - Duty cycle register		PDUT3	W
000095 _H	PPG3 - Duty cycle register			W
000096 _H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097 _H	PPG3 - Control status register High	PCNH3		R/W
000098 _H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099 _H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009A _H	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009B _H	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009C _H	PPG4 - Timer register		PTMR4	R
00009D _H	PPG4 - Timer register			R
00009E _H	PPG4 - Period setting register		PCSR4	W
00009F _H	PPG4 - Period setting register			W
0000A0 _H	PPG4 - Duty cycle register		PDUT4	W
0000A1 _H	PPG4 - Duty cycle register			W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000A2 _H	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3 _H	PPG4 - Control status register High	PCNH4		R/W
0000A4 _H	PPG5 - Timer register		PTMR5	R
0000A5 _H	PPG5 - Timer register			R
0000A6 _H	PPG5 - Period setting register		PCSR5	W
0000A7 _H	PPG5 - Period setting register			W
0000A8 _H	PPG5 - Duty cycle register		PDUT5	W
0000A9 _H	PPG5 - Duty cycle register			W
0000AA _H	PPG5 - Control status register Low	PCNL5	PCN5	R/W
0000AB _H	PPG5 - Control status register High	PCNH5		R/W
0000AC _H	I2C0 - Bus Status Register	IBSR0		R
0000AD _H	I2C0 - Bus Control Register	IBCR0		R/W
0000AE _H	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AF _H	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0 _H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1 _H	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2 _H	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3 _H	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4 _H	I2C0 - Data Register	IDAR0		R/W
0000B5 _H	I2C0 - Clock Control Register	ICCR0		R/W
0000B6 _H	I2C1 - Bus Status Register	IBSR1		R
0000B7 _H	I2C1 - Bus Control Register	IBCR1		R/W
0000B8 _H	I2C1 - Ten bit Slave address Register Low	ITBAL1	ITBA1	R/W
0000B9 _H	I2C1 - Ten bit Slave address Register High	ITBAH1		R/W
0000BA _H	I2C1 - Ten bit Address mask Register Low	ITMKL1	ITMK1	R/W
0000BB _H	I2C1 - Ten bit Address mask Register High	ITMKH1		R/W
0000BC _H	I2C1 - Seven bit Slave address Register	ISBA1		R/W
0000BD _H	I2C1 - Seven bit Address mask Register	ISMK1		R/W
0000BE _H	I2C1 - Data Register	IDAR1		R/W
0000BF _H	I2C1 - Clock Control Register	ICCR1		R/W
0000C0 _H	USART0 - Serial Mode Register	SMR0		R/W
0000C1 _H	USART0 - Serial Control Register	SCR0		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000C2 _H	USART0 - TX Register	TDR0		W
0000C2 _H	USART0 - RX Register	RDR0		R
0000C3 _H	USART0 - Serial Status	SSR0		R/W
0000C4 _H	USART0 - Control/Com. Register	ECCR0		R/W
0000C5 _H	USART0 - Ext. Status Register	ESCR0		R/W
0000C6 _H	USART0 - Baud Rate Generator Register Low	BGRL0	BGR0	R/W
0000C7 _H	USART0 - Baud Rate Generator Register High	BGRH0		R/W
0000C8 _H	USART0 - Extended Serial Interrupt Register	ESIR0		R/W
0000C9 _H	Reserved			-
0000CA _H	USART1 - Serial Mode Register	SMR1		R/W
0000CB _H	USART1 - Serial Control Register	SCR1		R/W
0000CC _H	USART1 - TX Register	TDR1		W
0000CC _H	USART1 - RX Register	RDR1		R
0000CD _H	USART1 - Serial Status	SSR1		R/W
0000CE _H	USART1 - Control/Com. Register	ECCR1		R/W
0000CF _H	USART1 - Ext. Status Register	ESCR1		R/W
0000D0 _H	USART1 - Baud Rate Generator Register Low	BGRL1	BGR1	R/W
0000D1 _H	USART1 - Baud Rate Generator Register High	BGRH1		R/W
0000D2 _H	USART1 - Extended Serial Interrupt Register	ESIR1		R/W
0000D3 _H	Reserved			-
0000D4 _H	USART2 - Serial Mode Register	SMR2		R/W
0000D5 _H	USART2 - Serial Control Register	SCR2		R/W
0000D6 _H	USART2 - TX Register	TDR2		W
0000D6 _H	USART2 - RX Register	RDR2		R
0000D7 _H	USART2 - Serial Status	SSR2		R/W
0000D8 _H	USART2 - Control/Com. Register	ECCR2		R/W
0000D9 _H	USART2 - Ext. Status Register	ESCR2		R/W
0000DA _H	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DB _H	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DC _H	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DD _H	Reserved			-
0000DE _H	USART3 - Serial Mode Register	SMR3		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000DF _H	USART3 - Serial Control Register	SCR3		R/W
0000E0 _H	USART3 - TX Register	TDR3		W
0000E0 _H	USART3 - RX Register	RDR3		R
0000E1 _H	USART3 - Serial Status	SSR3		R/W
0000E2 _H	USART3 - Control/Com. Register	ECCR3		R/W
0000E3 _H	USART3 - Ext. Status Register	ESCR3		R/W
0000E4 _H	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5 _H	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6 _H	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7 _H -0000EF _H	Reserved			-
0000F0 _H -0000FF _H	External Bus area	EXTBUS0		R/W
000100 _H	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101 _H	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102 _H	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103 _H	DMA0 - DMA control register	DMACS0		R/W
000104 _H	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105 _H	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106 _H	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107 _H	DMA0 - Data counter high byte	DCTH0		R/W
000108 _H	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109 _H	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010A _H	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010B _H	DMA1 - DMA control register	DMACS1		R/W
00010C _H	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W
00010D _H	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E _H	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F _H	DMA1 - Data counter high byte	DCTH1		R/W
000110 _H	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111 _H	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112 _H	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113 _H	DMA2 - DMA control register	DMACS2		R/W
000114 _H	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000115 _H	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116 _H	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117 _H	DMA2 - Data counter high byte	DCTH2		R/W
000118 _H	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119 _H	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A _H	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B _H	DMA3 - DMA control register	DMACS3		R/W
00011C _H	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D _H	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E _H	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F _H	DMA3 - Data counter high byte	DCTH3		R/W
000120 _H	DMA4 - Buffer address pointer low byte	BAPL4		R/W
000121 _H	DMA4 - Buffer address pointer middle byte	BAPM4		R/W
000122 _H	DMA4 - Buffer address pointer high byte	BAPH4		R/W
000123 _H	DMA4 - DMA control register	DMACS4		R/W
000124 _H	DMA4 - I/O register address pointer low byte	IOAL4	IOA4	R/W
000125 _H	DMA4 - I/O register address pointer high byte	IOAH4		R/W
000126 _H	DMA4 - Data counter low byte	DCTL4	DCT4	R/W
000127 _H	DMA4 - Data counter high byte	DCTH4		R/W
000128 _H	DMA5 - Buffer address pointer low byte	BAPL5		R/W
000129 _H	DMA5 - Buffer address pointer middle byte	BAPM5		R/W
00012A _H	DMA5 - Buffer address pointer high byte	BAPH5		R/W
00012B _H	DMA5 - DMA control register	DMACS5		R/W
00012C _H	DMA5 - I/O register address pointer low byte	IOAL5	IOA5	R/W
00012D _H	DMA5 - I/O register address pointer high byte	IOAH5		R/W
00012E _H	DMA5 - Data counter low byte	DCTL5	DCT5	R/W
00012F _H	DMA5 - Data counter high byte	DCTH5		R/W
000130 _H -00017F _H	Reserved			-
000180 _H -00037F _H	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380 _H	DMA0 - Interrupt select	DISEL0		R/W
000381 _H	DMA1 - Interrupt select	DISEL1		R/W
000382 _H	DMA2 - Interrupt select	DISEL2		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000383 _H	DMA3 - Interrupt select	DISSEL3		R/W
000384 _H	DMA4 - Interrupt select	DISSEL4		R/W
000385 _H	DMA5 - Interrupt select	DISSEL5		R/W
000386 _H -00038F _H	Reserved			-
000390 _H	DMA - Status register low byte	DSRL	DSR	R/W
000391 _H	DMA - Status register high byte	DSRH		R/W
000392 _H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393 _H	DMA - Stop status register high byte	DSSRH		R/W
000394 _H	DMA - Enable register low byte	DERL	DER	R/W
000395 _H	DMA - Enable register high byte	DERH		R/W
000396 _H -00039F _H	Reserved			-
0003A0 _H	Interrupt level register	ILR	ICR	R/W
0003A1 _H	Interrupt index register	IDX		R/W
0003A2 _H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3 _H	Interrupt vector table base register High	TBRH		R/W
0003A4 _H	Delayed Interrupt register	DIRR		R/W
0003A5 _H	Non Maskable Interrupt register	NMI		R/W
0003A6 _H -0003AB _H	Reserved			-
0003AC _H	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003AD _H	EDSU communication interrupt selection High	EDSU2H		R/W
0003AE _H	ROM mirror control register	ROMM		R/W
0003AF _H	EDSU configuration register	EDSU		R/W
0003B0 _H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1 _H	Memory patch control/status register ch 0/1			R/W
0003B2 _H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3 _H	Memory patch control/status register ch 2/3			R/W
0003B4 _H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5 _H	Memory patch control/status register ch 4/5			R/W
0003B6 _H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7 _H	Memory patch control/status register ch 6/7			R/W
0003B8 _H	Memory Patch function - Patch address 0 low	PFALO		R/W
0003B9 _H	Memory Patch function - Patch address 0 middle	PFAM0		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003BA _H	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BB _H	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BC _H	Memory Patch function - Patch address 1 middle	PFAM1		R/W
0003BD _H	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BE _H	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BF _H	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0 _H	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1 _H	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2 _H	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3 _H	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4 _H	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5 _H	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6 _H	Memory Patch function - Patch address 4 high	PFAH4		R/W
0003C7 _H	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8 _H	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9 _H	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CA _H	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CB _H	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CC _H	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CD _H	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CE _H	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CF _H	Memory Patch function - Patch address 7 high	PFAH7		R/W
0003D0 _H	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1 _H	Memory Patch function - Patch data 0 High	PFDH0		R/W
0003D2 _H	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
0003D3 _H	Memory Patch function - Patch data 1 High	PFDH1		R/W
0003D4 _H	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
0003D5 _H	Memory Patch function - Patch data 2 High	PFDH2		R/W
0003D6 _H	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
0003D7 _H	Memory Patch function - Patch data 3 High	PFDH3		R/W
0003D8 _H	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
0003D9 _H	Memory Patch function - Patch data 4 High	PFDH4		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003DA _H	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W
0003DB _H	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DC _H	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD _H	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DE _H	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF _H	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0 _H	Data Flash Control and Status register A	DFCSA		R/W
0003E1 _H	Data Flash Write command sequencer Control register A	DFWCA		R/W
0003E2 _H	Data Flash Write command sequencer Status register A	DFWSA		R/W
0003E3 _H -0003F0 _H	Reserved			-
0003F1 _H	Memory Control Status Register A	MCSRA		R/W
0003F2 _H	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3 _H	Memory Timing Configuration Register A High	MTCRAH		R/W
0003F4 _H	Reserved			-
0003F5 _H	Memory Control Status Register B	MCSR B		R/W
0003F6 _H	Memory Timing Configuration Register B Low	MTCRBL	MTCRB	R/W
0003F7 _H	Memory Timing Configuration Register B High	MTCRBH		R/W
0003F8 _H	Flash Memory Write Control register 0	FMWC0		R/W
0003F9 _H	Flash Memory Write Control register 1	FMWC1		R/W
0003FA _H	Flash Memory Write Control register 2	FMWC2		R/W
0003FB _H	Flash Memory Write Control register 3	FMWC3		R/W
0003FC _H	Flash Memory Write Control register 4	FMWC4		R/W
0003FD _H	Flash Memory Write Control register 5	FMWC5		R/W
0003FE _H -0003FF _H	Reserved			-
000400 _H	Standby Mode control register	SMCR		R/W
000401 _H	Clock select register	CKSR		R/W
000402 _H	Clock Stabilization select register	CKSSR		R/W
000403 _H	Clock monitor register	CKMR		R
000404 _H	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405 _H	Clock Frequency control register High	CKFCRH		R/W
000406 _H	PLL Control register Low	PLLCRL	PLLCR	R/W
000407 _H	PLL Control register High	PLLCRH		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000408 _H	RC clock timer control register	RCTCR		R/W
000409 _H	Main clock timer control register	MCTCR		R/W
00040A _H	Sub clock timer control register	SCTCR		R/W
00040B _H	Reset cause and clock status register with clear function	RCCSRC		R
00040C _H	Reset configuration register	RCR		R/W
00040D _H	Reset cause and clock status register	RCCSR		R
00040E _H	Watch dog timer configuration register	WDTC		R/W
00040F _H	Watch dog timer clear pattern register	WDTCP		W
000410 _H -000414 _H	Reserved			-
000415 _H	Clock output activation register	COAR		R/W
000416 _H	Clock output configuration register 0	COCR0		R/W
000417 _H	Clock output configuration register 1	COCR1		R/W
000418 _H	Clock Modulator control register	CMCR		R/W
000419 _H	Reserved			-
00041A _H	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B _H	Clock Modulator Parameter register High	CMPRH		R/W
00041C _H -00042B _H	Reserved			-
00042C _H	Voltage Regulator Control register	VRCR		R/W
00042D _H	Clock Input and LVD Control Register	CILCR		R/W
00042E _H -00042F _H	Reserved			-
000430 _H	I/O Port P00 - Data Direction Register	DDR00		R/W
000431 _H	I/O Port P01 - Data Direction Register	DDR01		R/W
000432 _H	I/O Port P02 - Data Direction Register	DDR02		R/W
000433 _H	I/O Port P03 - Data Direction Register	DDR03		R/W
000434 _H	I/O Port P04 - Data Direction Register	DDR04		R/W
000435 _H	I/O Port P05 - Data Direction Register	DDR05		R/W
000436 _H	I/O Port P06 - Data Direction Register	DDR06		R/W
000437 _H	I/O Port P07 - Data Direction Register	DDR07		R/W
000438 _H	I/O Port P08 - Data Direction Register	DDR08		R/W
000439 _H	I/O Port P09 - Data Direction Register	DDR09		R/W
00043A _H	I/O Port P10 - Data Direction Register	DDR10		R/W
00043B _H -000443 _H	Reserved			-

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000444 _H	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445 _H	I/O Port P01 - Port Input Enable Register	PIER01		R/W
000446 _H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447 _H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448 _H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449 _H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044A _H	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044B _H	I/O Port P07 - Port Input Enable Register	PIER07		R/W
00044C _H	I/O Port P08 - Port Input Enable Register	PIER08		R/W
00044D _H	I/O Port P09 - Port Input Enable Register	PIER09		R/W
00044E _H	I/O Port P10 - Port Input Enable Register	PIER10		R/W
00044F _H -000457 _H	Reserved			-
000458 _H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459 _H	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045A _H	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045B _H	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045C _H	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045D _H	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045E _H	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045F _H	I/O Port P07 - Port Input Level Register	PILR07		R/W
000460 _H	I/O Port P08 - Port Input Level Register	PILR08		R/W
000461 _H	I/O Port P09 - Port Input Level Register	PILR09		R/W
000462 _H	I/O Port P10 - Port Input Level Register	PILR10		R/W
000463 _H -00046B _H	Reserved			-
00046C _H	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046D _H	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046E _H	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046F _H	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470 _H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471 _H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472 _H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473 _H	I/O Port P07 - Extended Port Input Level Register	EPILR07		R/W

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Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000474 _H	I/O Port P08 - Extended Port Input Level Register	EPILR08		R/W
000475 _H	I/O Port P09 - Extended Port Input Level Register	EPILR09		R/W
000476 _H	I/O Port P10 - Extended Port Input Level Register	EPILR10		R/W
000477 _H -00047F _H	Reserved			-
000480 _H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481 _H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482 _H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483 _H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484 _H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485 _H	I/O Port P05 - Port Output Drive Register	PODR05		R/W
000486 _H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487 _H	I/O Port P07 - Port Output Drive Register	PODR07		R/W
000488 _H	I/O Port P08 - Port Output Drive Register	PODR08		R/W
000489 _H	I/O Port P09 - Port Output Drive Register	PODR09		R/W
00048A _H	I/O Port P10 - Port Output Drive Register	PODR10		R/W
00048B _H -00049B _H	Reserved			-
00049C _H	I/O Port P08 - Port High Drive Register	PHDR08		R/W
00049D _H	I/O Port P09 - Port High Drive Register	PHDR09		R/W
00049E _H	I/O Port P10 - Port High Drive Register	PHDR10		R/W
00049F _H -0004A7 _H	Reserved			-
0004A8 _H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9 _H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
0004AA _H	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004AB _H	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004AC _H	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004AD _H	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AE _H	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AF _H	I/O Port P07 - Pull-Up resistor Control Register	PUCR07		R/W
0004B0 _H	I/O Port P08 - Pull-Up resistor Control Register	PUCR08		R/W
0004B1 _H	I/O Port P09 - Pull-Up resistor Control Register	PUCR09		R/W
0004B2 _H	I/O Port P10 - Pull-Up resistor Control Register	PUCR10		R/W
0004B3 _H -0004BB _H	Reserved			-

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004BC _H	I/O Port P00 - External Pin State Register	EPSR00		R
0004BD _H	I/O Port P01 - External Pin State Register	EPSR01		R
0004BE _H	I/O Port P02 - External Pin State Register	EPSR02		R
0004BF _H	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0 _H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1 _H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2 _H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3 _H	I/O Port P07 - External Pin State Register	EPSR07		R
0004C4 _H	I/O Port P08 - External Pin State Register	EPSR08		R
0004C5 _H	I/O Port P09 - External Pin State Register	EPSR09		R
0004C6 _H	I/O Port P10 - External Pin State Register	EPSR10		R
0004C7 _H -0004CF _H	Reserved			-
0004D0 _H	ADC analog input enable register 0	ADER0		R/W
0004D1 _H	ADC analog input enable register 1	ADER1		R/W
0004D2 _H	ADC analog input enable register 2	ADER2		R/W
0004D3 _H	ADC analog input enable register 3	ADER3		R/W
0004D4 _H	ADC analog input enable register 4	ADER4		R/W
0004D5 _H	Reserved			-
0004D6 _H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7 _H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8 _H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9 _H	Peripheral Resource Relocation Register 3	PRRR3		R/W
0004DA _H	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB _H	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC _H	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD _H	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE _H	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF _H	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0 _H	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1 _H	RTC - Sub Second Register M	WTBRH0		R/W
0004E2 _H	RTC - Sub-Second Register H	WTBR1		R/W
0004E3 _H	RTC - Second Register	WTSR		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004E4 _H	RTC - Minutes	WTMR		R/W
0004E5 _H	RTC - Hour	WTHR		R/W
0004E6 _H	RTC - Timer Control Extended Register	WTCER		R/W
0004E7 _H	RTC - Clock select register	WTCKSR		R/W
0004E8 _H	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9 _H	RTC - Timer Control Register High	WTCRH		R/W
0004EA _H	CAL - Calibration unit Control register	CUCR		R/W
0004EB _H	Reserved			-
0004EC _H	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED _H	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE _H	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF _H	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0 _H	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1 _H	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2 _H -0004F9 _H	Reserved			-
0004FA _H	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB _H -00053D _H	Reserved			-
00053E _H	USART7 - Serial Mode Register	SMR7		R/W
00053F _H	USART7 - Serial Control Register	SCR7		R/W
000540 _H	USART7 - Serial TX Register	TDR7		W
000540 _H	USART7 - Serial RX Register	RDR7		R
000541 _H	USART7 - Serial Status Register	SSR7		R/W
000542 _H	USART7 - Ext. Control/Com. Register	ECCR7		R/W
000543 _H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544 _H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545 _H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546 _H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547 _H	Reserved			-
000548 _H	USART8 - Serial Mode Register	SMR8		R/W
000549 _H	USART8 - Serial Control Register	SCR8		R/W
00054A _H	USART8 - Serial TX Register	TDR8		W
00054A _H	USART8 - Serial RX Register	RDR8		R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00054B _H	USART8 - Serial Status Register	SSR8		R/W
00054C _H	USART8 - Ext. Control/Com. Register	ECCR8		R/W
00054D _H	USART8 - Ext. Status Com. Register	ESCR8		R/W
00054E _H	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
00054F _H	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550 _H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551 _H	Reserved			-
000552 _H	USART9 - Serial Mode Register	SMR9		R/W
000553 _H	USART9 - Serial Control Register	SCR9		R/W
000554 _H	USART9 - Serial TX Register	TDR9		W
000554 _H	USART9 - Serial RX Register	RDR9		R
000555 _H	USART9 - Serial Status Register	SSR9		R/W
000556 _H	USART9 - Ext. Control/Com. Register	ECCR9		R/W
000557 _H	USART9 - Ext. Status Com. Register	ESCR9		R/W
000558 _H	USART9 - Baud Rate Generator Register Low	BGRL9	BGR9	R/W
000559 _H	USART9 - Baud Rate Generator Register High	BGRH9		R/W
00055A _H	USART9 - Extended Serial Interrupt Register	ESIR9		R/W
00055B _H -00055F _H	Reserved			-
000560 _H	ALARM0 - Control Status Register	ACSR0		R/W
000561 _H	ALARM0 - Extended Control Status Register	AECSR0		R/W
000562 _H	ALARM1 - Control Status Register	ACSR1		R/W
000563 _H	ALARM1 - Extended Control Status Register	AECSR1		R/W
000564 _H	PPG6 - Timer register		PTMR6	R
000565 _H	PPG6 - Timer register			R
000566 _H	PPG6 - Period setting register		PCSR6	W
000567 _H	PPG6 - Period setting register			W
000568 _H	PPG6 - Duty cycle register		PDUT6	W
000569 _H	PPG6 - Duty cycle register			W
00056A _H	PPG6 - Control status register Low	PCNL6	PCN6	R/W
00056B _H	PPG6 - Control status register High	PCNH6		R/W
00056C _H	PPG7 - Timer register		PTMR7	R
00056D _H	PPG7 - Timer register			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00056E _H	PPG7 - Period setting register		PCSR7	W
00056F _H	PPG7 - Period setting register			W
000570 _H	PPG7 - Duty cycle register		PDUT7	W
000571 _H	PPG7 - Duty cycle register			W
000572 _H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573 _H	PPG7 - Control status register High	PCNH7		R/W
000574 _H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575 _H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576 _H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577 _H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578 _H	PPG8 - Timer register		PTMR8	R
000579 _H	PPG8 - Timer register			R
00057A _H	PPG8 - Period setting register		PCSR8	W
00057B _H	PPG8 - Period setting register			W
00057C _H	PPG8 - Duty cycle register		PDUT8	W
00057D _H	PPG8 - Duty cycle register			W
00057E _H	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057F _H	PPG8 - Control status register High	PCNH8		R/W
000580 _H	PPG9 - Timer register		PTMR9	R
000581 _H	PPG9 - Timer register			R
000582 _H	PPG9 - Period setting register		PCSR9	W
000583 _H	PPG9 - Period setting register			W
000584 _H	PPG9 - Duty cycle register		PDUT9	W
000585 _H	PPG9 - Duty cycle register			W
000586 _H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587 _H	PPG9 - Control status register High	PCNH9		R/W
000588 _H	PPG10 - Timer register		PTMR10	R
000589 _H	PPG10 - Timer register			R
00058A _H	PPG10 - Period setting register		PCSR10	W
00058B _H	PPG10 - Period setting register			W
00058C _H	PPG10 - Duty cycle register		PDUT10	W
00058D _H	PPG10 - Duty cycle register			W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058E _H	PPG10 - Control status register Low	PCNL10	PCN10	R/W
00058F _H	PPG10 - Control status register High	PCNH10		R/W
000590 _H	PPG11 - Timer register		PTMR11	R
000591 _H	PPG11 - Timer register			R
000592 _H	PPG11 - Period setting register		PCSR11	W
000593 _H	PPG11 - Period setting register			W
000594 _H	PPG11 - Duty cycle register		PDUT11	W
000595 _H	PPG11 - Duty cycle register			W
000596 _H	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597 _H	PPG11 - Control status register High	PCNH11		R/W
000598 _H	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599 _H	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A _H	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B _H	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C _H	PPG12 - Timer register		PTMR12	R
00059D _H	PPG12 - Timer register			R
00059E _H	PPG12 - Period setting register		PCSR12	W
00059F _H	PPG12 - Period setting register			W
0005A0 _H	PPG12 - Duty cycle register		PDUT12	W
0005A1 _H	PPG12 - Duty cycle register			W
0005A2 _H	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3 _H	PPG12 - Control status register High	PCNH12		R/W
0005A4 _H	PPG13 - Timer register		PTMR13	R
0005A5 _H	PPG13 - Timer register			R
0005A6 _H	PPG13 - Period setting register		PCSR13	W
0005A7 _H	PPG13 - Period setting register			W
0005A8 _H	PPG13 - Duty cycle register		PDUT13	W
0005A9 _H	PPG13 - Duty cycle register			W
0005AA _H	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB _H	PPG13 - Control status register High	PCNH13		R/W
0005AC _H	PPG14 - Timer register		PTMR14	R
0005AD _H	PPG14 - Timer register			R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005AE _H	PPG14 - Period setting register		PCSR14	W
0005AF _H	PPG14 - Period setting register			W
0005B0 _H	PPG14 - Duty cycle register		PDUT14	W
0005B1 _H	PPG14 - Duty cycle register			W
0005B2 _H	PPG14 - Control status register Low	PCNL14	PCN14	R/W
0005B3 _H	PPG14 - Control status register High	PCNH14		R/W
0005B4 _H	PPG15 - Timer register		PTMR15	R
0005B5 _H	PPG15 - Timer register			R
0005B6 _H	PPG15 - Period setting register		PCSR15	W
0005B7 _H	PPG15 - Period setting register			W
0005B8 _H	PPG15 - Duty cycle register		PDUT15	W
0005B9 _H	PPG15 - Duty cycle register			W
0005BA _H	PPG15 - Control status register Low	PCNL15	PCN15	R/W
0005BB _H	PPG15 - Control status register High	PCNH15		R/W
0005BC _H -00065F _H	Reserved			-
000660 _H	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661 _H	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662 _H	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663 _H	Peripheral Resource Relocation Register 13	PRRR13		W
000664 _H -0006DF _H	Reserved			-
0006E0 _H	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
0006E1 _H	External Bus - Area configuration register 0 High	EACH0		R/W
0006E2 _H	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
0006E3 _H	External Bus - Area configuration register 1 High	EACH1		R/W
0006E4 _H	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
0006E5 _H	External Bus - Area configuration register 2 High	EACH2		R/W
0006E6 _H	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
0006E7 _H	External Bus - Area configuration register 3 High	EACH3		R/W
0006E8 _H	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
0006E9 _H	External Bus - Area configuration register 4 High	EACH4		R/W
0006EA _H	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
0006EB _H	External Bus - Area configuration register 5 High	EACH5		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006EC _H	External Bus - Area select register 2	EAS2		R/W
0006ED _H	External Bus - Area select register 3	EAS3		R/W
0006EE _H	External Bus - Area select register 4	EAS4		R/W
0006EF _H	External Bus - Area select register 5	EAS5		R/W
0006F0 _H	External Bus - Mode register	EBM		R/W
0006F1 _H	External Bus - Clock and Function register	EBCF		R/W
0006F2 _H	External Bus - Address output enable register 0	EBAE0		R/W
0006F3 _H	External Bus - Address output enable register 1	EBAE1		R/W
0006F4 _H	External Bus - Address output enable register 2	EBAE2		R/W
0006F5 _H	External Bus - Control signal register	EBCS		R/W
0006F6 _H -0006FF _H	Reserved			-
000700 _H	CAN0 - Control register Low	CTRLRL0	CTRLR0	R/W
000701 _H	CAN0 - Control register High (reserved)	CTRLRH0		R
000702 _H	CAN0 - Status register Low	STATRL0	STATR0	R/W
000703 _H	CAN0 - Status register High (reserved)	STATRH0		R
000704 _H	CAN0 - Error Counter Low (Transmit)	ERRCNTL0	ERRCNT0	R
000705 _H	CAN0 - Error Counter High (Receive)	ERRCNTH0		R
000706 _H	CAN0 - Bit Timing Register Low	BTRL0	BTR0	R/W
000707 _H	CAN0 - Bit Timing Register High	BTRH0		R/W
000708 _H	CAN0 - Interrupt Register Low	INTRL0	INTR0	R
000709 _H	CAN0 - Interrupt Register High	INTRH0		R
00070A _H	CAN0 - Test Register Low	TESTRL0	TESTR0	R/W
00070B _H	CAN0 - Test Register High (reserved)	TESTRH0		R
00070C _H	CAN0 - BRP Extension register Low	BRPERL0	BRPER0	R/W
00070D _H	CAN0 - BRP Extension register High (reserved)	BRPERH0		R
00070E _H -00070F _H	Reserved			-
000710 _H	CAN0 - IF1 Command request register Low	IF1CREQL0	IF1CREQ0	R/W
000711 _H	CAN0 - IF1 Command request register High	IF1CREQH0		R/W
000712 _H	CAN0 - IF1 Command Mask register Low	IF1CMSKL0	IF1CMSK0	R/W
000713 _H	CAN0 - IF1 Command Mask register High (reserved)	IF1CMSKH0		R
000714 _H	CAN0 - IF1 Mask 1 Register Low	IF1MSK1L0	IF1MSK10	R/W
000715 _H	CAN0 - IF1 Mask 1 Register High	IF1MSK1H0		R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000716 _H	CAN0 - IF1 Mask 2 Register Low	IF1MSK2L0	IF1MSK20	R/W
000717 _H	CAN0 - IF1 Mask 2 Register High	IF1MSK2H0		R/W
000718 _H	CAN0 - IF1 Arbitration 1 Register Low	IF1ARB1L0	IF1ARB10	R/W
000719 _H	CAN0 - IF1 Arbitration 1 Register High	IF1ARB1H0		R/W
00071A _H	CAN0 - IF1 Arbitration 2 Register Low	IF1ARB2L0	IF1ARB20	R/W
00071B _H	CAN0 - IF1 Arbitration 2 Register High	IF1ARB2H0		R/W
00071C _H	CAN0 - IF1 Message Control Register Low	IF1MCTRL0	IF1MCTR0	R/W
00071D _H	CAN0 - IF1 Message Control Register High	IF1MCTRH0		R/W
00071E _H	CAN0 - IF1 Data A1 Low	IF1DTA1L0	IF1DTA10	R/W
00071F _H	CAN0 - IF1 Data A1 High	IF1DTA1H0		R/W
000720 _H	CAN0 - IF1 Data A2 Low	IF1DTA2L0	IF1DTA20	R/W
000721 _H	CAN0 - IF1 Data A2 High	IF1DTA2H0		R/W
000722 _H	CAN0 - IF1 Data B1 Low	IF1DTB1L0	IF1DTB10	R/W
000723 _H	CAN0 - IF1 Data B1 High	IF1DTB1H0		R/W
000724 _H	CAN0 - IF1 Data B2 Low	IF1DTB2L0	IF1DTB20	R/W
000725 _H	CAN0 - IF1 Data B2 High	IF1DTB2H0		R/W
000726 _H -00073F _H	Reserved			-
000740 _H	CAN0 - IF2 Command request register Low	IF2CREQL0	IF2CREQ0	R/W
000741 _H	CAN0 - IF2 Command request register High	IF2CREQH0		R/W
000742 _H	CAN0 - IF2 Command Mask register Low	IF2CMSKL0	IF2CMSK0	R/W
000743 _H	CAN0 - IF2 Command Mask register High (reserved)	IF2CMSKH0		R
000744 _H	CAN0 - IF2 Mask 1 Register Low	IF2MSK1L0	IF2MSK10	R/W
000745 _H	CAN0 - IF2 Mask 1 Register High	IF2MSK1H0		R/W
000746 _H	CAN0 - IF2 Mask 2 Register Low	IF2MSK2L0	IF2MSK20	R/W
000747 _H	CAN0 - IF2 Mask 2 Register High	IF2MSK2H0		R/W
000748 _H	CAN0 - IF2 Arbitration 1 Register Low	IF2ARB1L0	IF2ARB10	R/W
000749 _H	CAN0 - IF2 Arbitration 1 Register High	IF2ARB1H0		R/W
00074A _H	CAN0 - IF2 Arbitration 2 Register Low	IF2ARB2L0	IF2ARB20	R/W
00074B _H	CAN0 - IF2 Arbitration 2 Register High	IF2ARB2H0		R/W
00074C _H	CAN0 - IF2 Message Control Register Low	IF2MCTRL0	IF2MCTR0	R/W
00074D _H	CAN0 - IF2 Message Control Register High	IF2MCTRH0		R/W
00074E _H	CAN0 - IF2 Data A1 Low	IF2DTA1L0	IF2DTA10	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00074F _H	CAN0 - IF2 Data A1 High	IF2DTA1H0		R/W
000750 _H	CAN0 - IF2 Data A2 Low	IF2DTA2L0	IF2DTA20	R/W
000751 _H	CAN0 - IF2 Data A2 High	IF2DTA2H0		R/W
000752 _H	CAN0 - IF2 Data B1 Low	IF2DTB1L0	IF2DTB10	R/W
000753 _H	CAN0 - IF2 Data B1 High	IF2DTB1H0		R/W
000754 _H	CAN0 - IF2 Data B2 Low	IF2DTB2L0	IF2DTB20	R/W
000755 _H	CAN0 - IF2 Data B2 High	IF2DTB2H0		R/W
000756 _H -00077F _H	Reserved			-
000780 _H	CAN0 - Transmission Request 1 Register Low	TREQR1L0	TREQR10	R
000781 _H	CAN0 - Transmission Request 1 Register High	TREQR1H0		R
000782 _H	CAN0 - Transmission Request 2 Register Low	TREQR2L0	TREQR20	R
000783 _H	CAN0 - Transmission Request 2 Register High	TREQR2H0		R
000784 _H -00078F _H	Reserved			-
000790 _H	CAN0 - New Data 1 Register Low	NEWDT1L0	NEWDT10	R
000791 _H	CAN0 - New Data 1 Register High	NEWDT1H0		R
000792 _H	CAN0 - New Data 2 Register Low	NEWDT2L0	NEWDT20	R
000793 _H	CAN0 - New Data 2 Register High	NEWDT2H0		R
000794 _H -00079F _H	Reserved			-
0007A0 _H	CAN0 - Interrupt Pending 1 Register Low	INTPND1L0	INTPND10	R
0007A1 _H	CAN0 - Interrupt Pending 1 Register High	INTPND1H0		R
0007A2 _H	CAN0 - Interrupt Pending 2 Register Low	INTPND2L0	INTPND20	R
0007A3 _H	CAN0 - Interrupt Pending 2 Register High	INTPND2H0		R
0007A4 _H -0007AF _H	Reserved			-
0007B0 _H	CAN0 - Message Valid 1 Register Low	MSGVAL1L0	MSGVAL10	R
0007B1 _H	CAN0 - Message Valid 1 Register High	MSGVAL1H0		R
0007B2 _H	CAN0 - Message Valid 2 Register Low	MSGVAL2L0	MSGVAL20	R
0007B3 _H	CAN0 - Message Valid 2 Register High	MSGVAL2H0		R
0007B4 _H -0007CD _H	Reserved			-
0007CE _H	CAN0 - Output enable register	COER0		R/W
0007CF _H -0007FF _H	Reserved			-
000800 _H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801 _H	CAN1 - Control register High (reserved)	CTRLRH1		R

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000802 _H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803 _H	CAN1 - Status register High (reserved)	STATRH1		R
000804 _H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805 _H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806 _H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807 _H	CAN1 - Bit Timing Register High	BTRH1		R/W
000808 _H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809 _H	CAN1 - Interrupt Register High	INTRH1		R
00080A _H	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080B _H	CAN1 - Test Register High (reserved)	TESTRH1		R
00080C _H	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080D _H	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080E _H -00080F _H	Reserved			-
000810 _H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811 _H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812 _H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813 _H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814 _H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815 _H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816 _H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817 _H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818 _H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819 _H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081A _H	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081B _H	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081C _H	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081D _H	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081E _H	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081F _H	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820 _H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821 _H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822 _H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000823 _H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824 _H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825 _H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W
000826 _H -00083F _H	Reserved			-
000840 _H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841 _H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842 _H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843 _H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844 _H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845 _H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846 _H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847 _H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848 _H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849 _H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
00084A _H	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
00084B _H	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
00084C _H	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084D _H	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
00084E _H	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084F _H	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850 _H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851 _H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852 _H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853 _H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854 _H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855 _H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856 _H -00087F _H	Reserved			-
000880 _H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881 _H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882 _H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883 _H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R
000884 _H -00088F _H	Reserved			-

Table 4: I/O map CY96(F)34x

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000890 _H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891 _H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892 _H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893 _H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894 _H -00089F _H	Reserved			-
0008A0 _H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1 _H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2 _H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3 _H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4 _H -0008AF _H	Reserved			-
0008B0 _H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1 _H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2 _H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3 _H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4 _H -0008CD _H	Reserved			-
0008CE _H	CAN1 - Output enable register	COER1		R/W
0008CF _H -0009FF _H	Reserved			-
000A00 _H	DMA - IO address block register 0	IOABK0		R/W
000A01 _H	DMA - IO address block register 1	IOABK1		R/W
000A02 _H	DMA - IO address block register 2	IOABK2		R/W
000A03 _H	DMA - IO address block register 3	IOABK3		R/W
000A04 _H	DMA - IO address block register 4	IOABK4		R/W
000A05 _H	DMA - IO address block register 5	IOABK5		R/W
000A06 _H -000BFF _H	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading 'X'. Registers of resources which are described in this table, but which are not supported by the device, should also be handled as "Reserved".

12. Interrupt Vector Table

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC _H	CALLV0	No	-	
1	3F8 _H	CALLV1	No	-	
2	3F4 _H	CALLV2	No	-	
3	3F0 _H	CALLV3	No	-	
4	3EC _H	CALLV4	No	-	
5	3E8 _H	CALLV5	No	-	
6	3E4 _H	CALLV6	No	-	
7	3E0 _H	CALLV7	No	-	
8	3DC _H	RESET	No	-	
9	3D8 _H	INT9	No	-	
10	3D4 _H	EXCEPTION	No	-	
11	3D0 _H	NMI	No	-	Non-Maskable Interrupt
12	3CC _H	DLY	No	12	Delayed Interrupt
13	3C8 _H	RC_TIMER	No	13	RC Timer
14	3C4 _H	MC_TIMER	No	14	Main Clock Timer
15	3C0 _H	SC_TIMER	No	15	Sub Clock Timer
16	3BC _H	RESERVED	No	16	Reserved
17	3B8 _H	EXTINT0	Yes	17	External Interrupt 0
18	3B4 _H	EXTINT1	Yes	18	External Interrupt 1
19	3B0 _H	EXTINT2	Yes	19	External Interrupt 2
20	3AC _H	EXTINT3	Yes	20	External Interrupt 3
21	3A8 _H	EXTINT4	Yes	21	External Interrupt 4
22	3A4 _H	EXTINT5	Yes	22	External Interrupt 5
23	3A0 _H	EXTINT6	Yes	23	External Interrupt 6
24	39C _H	EXTINT7	Yes	24	External Interrupt 7
25	398 _H	EXTINT8	Yes	25	External Interrupt 8
26	394 _H	EXTINT9	Yes	26	External Interrupt 9
27	390 _H	EXTINT10	Yes	27	External Interrupt 10
28	38C _H	EXTINT11	Yes	28	External Interrupt 11
29	388 _H	EXTINT12	Yes	29	External Interrupt 12

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
30	384 _H	EXTINT13	Yes	30	External Interrupt 13
31	380 _H	EXTINT14	Yes	31	External Interrupt 14
32	37C _H	EXTINT15	Yes	32	External Interrupt 15
33	378 _H	CAN0	No	33	CAN Controller 0 (except CY96(F)34xAyy or CY96(F)34xCyy)
34	374 _H	CAN1	No	34	CAN Controller 1 (except CY96(F)34xAyy, CY96(F)34xCyy, CY96F345Dyy or CY96F345Fyy)
35	370 _H	PPG0	Yes	35	Programmable Pulse Generator 0
36	36C _H	PPG1	Yes	36	Programmable Pulse Generator 1
37	368 _H	PPG2	Yes	37	Programmable Pulse Generator 2
38	364 _H	PPG3	Yes	38	Programmable Pulse Generator 3
39	360 _H	PPG4	Yes	39	Programmable Pulse Generator 4
40	35C _H	PPG5	Yes	40	Programmable Pulse Generator 5
41	358 _H	PPG6	Yes	41	Programmable Pulse Generator 6
42	354 _H	PPG7	Yes	42	Programmable Pulse Generator 7
43	350 _H	PPG8	Yes	43	Programmable Pulse Generator 8
44	34C _H	PPG9	Yes	44	Programmable Pulse Generator 9
45	348 _H	PPG10	Yes	45	Programmable Pulse Generator 10
46	344 _H	PPG11	Yes	46	Programmable Pulse Generator 11
47	340 _H	PPG12	Yes	47	Programmable Pulse Generator 12
48	33C _H	PPG13	Yes	48	Programmable Pulse Generator 13
49	338 _H	PPG14	Yes	49	Programmable Pulse Generator 14
50	334 _H	PPG15	Yes	50	Programmable Pulse Generator 15
51	330 _H	RLT0	Yes	51	Reload Timer 0
52	32C _H	RLT1	Yes	52	Reload Timer 1
53	328 _H	RLT2	Yes	53	Reload Timer 2
54	324 _H	RLT3	Yes	54	Reload Timer 3
55	320 _H	PPGRLT	Yes	55	Reload Timer 6 - dedicated for PPG
56	31C _H	ICU0	Yes	56	Input Capture Unit 0
57	318 _H	ICU1	Yes	57	Input Capture Unit 1
58	314 _H	ICU2	Yes	58	Input Capture Unit 2
59	310 _H	ICU3	Yes	59	Input Capture Unit 3

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
60	30C _H	ICU4	Yes	60	Input Capture Unit 4
61	308 _H	ICU5	Yes	61	Input Capture Unit 5
62	304 _H	ICU6	Yes	62	Input Capture Unit 6
63	300 _H	ICU7	Yes	63	Input Capture Unit 7
64	2FC _H	OCU0	Yes	64	Output Compare Unit 0
65	2F8 _H	OCU1	Yes	65	Output Compare Unit 1
66	2F4 _H	OCU2	Yes	66	Output Compare Unit 2
67	2F0 _H	OCU3	Yes	67	Output Compare Unit 3
68	2EC _H	OCU4	Yes	68	Output Compare Unit 4
69	2E8 _H	OCU5	Yes	69	Output Compare Unit 5
70	2E4 _H	OCU6	Yes	70	Output Compare Unit 6
71	2E0 _H	OCU7	Yes	71	Output Compare Unit 7
72	2DC _H	FRT0	Yes	72	Free Running Timer 0
73	2D8 _H	FRT1	Yes	73	Free Running Timer 1
74	2D4 _H	IIC0	Yes	74	I2C interface
75	2D0 _H	IIC1	Yes	75	I2C interface
76	2CC _H	ADC0	Yes	76	A/D Converter
77	2C8 _H	ALARM0	No	77	Alarm Comparator 0 (except CY96F345Dyy or CY96F345Fyy)
78	2C4 _H	ALARM1	No	78	Alarm Comparator 1 (except CY96F345Dyy or CY96F345Fyy)
79	2C0 _H	LINR0	Yes	79	LIN USART 0 RX
80	2BC _H	LINT0	Yes	80	LIN USART 0 TX
81	2B8 _H	LINR1	Yes	81	LIN USART 1 RX
82	2B4 _H	LINT1	Yes	82	LIN USART 1 TX
83	2B0 _H	LINR2	Yes	83	LIN USART 2 RX
84	2AC _H	LINT2	Yes	84	LIN USART 2 TX
85	2A8 _H	LINR3	Yes	85	LIN USART 3 RX
86	2A4 _H	LINT3	Yes	86	LIN USART 3 TX
87	2A0 _H	FLASH_A	No	87	Flash memory A (only Flash devices)
88	29C _H	FLASH_B	No	88	Flash memory B (only CY96F348T/H/C)
89	298 _H	LINR7	Yes	89	LIN USART 7 RX

Table 5: Interrupt vector table CY96(F)34x

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
90	294 _H	LINT7	Yes	90	LIN USART 7 TX
91	290 _H	LINR8	Yes	91	LIN USART 8 RX
92	28C _H	LINT8	Yes	92	LIN USART 8 TX
93	288 _H	LINR9	Yes	93	LIN USART 9 RX
94	284 _H	LINT9	Yes	94	LIN USART 9 TX
95	280 _H	RTC0	No	95	Real Timer Clock
96	27C _H	CAL0	No	96	Clock Calibration Unit
97	278 _H	DFLASH_A	Yes	97	Data Flash A (only CY96F345Dyy, CY96F345Fyy)

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication
- Handling of Data Flash

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 k Ω .

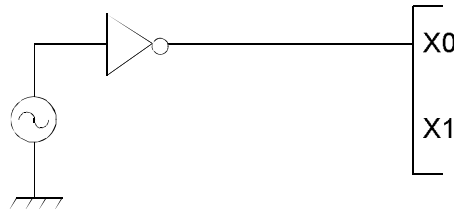
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See [AC Characteristics](#) for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

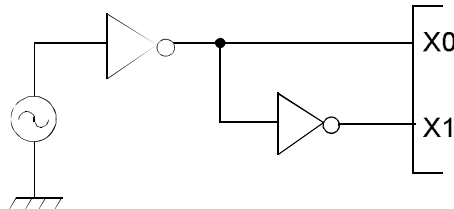
13.3.1 Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



13.3.2 Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



13.4 Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

13.5 Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.6 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC} -level as well as all V_{SS} -level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

13.7 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

13.8 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC} , $AVRH$, $AVRL$) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed $AVRH$ or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

13.9 Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

13.10 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 μ s from 0.2 V to 2.7 V.

13.11 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/ μ s or less in instantaneous fluctuation for power supply switching.

13.12 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication. Therefore, design a printed circuit board so as to avoid noise. Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.13 Handling of Data Flash

The Data Flash requires different and additional control signals for parallel programming. Please check with your programming equipment maker for support of this interface.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ [1]
AD Converter voltage references	AVRH, AVRL	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_I \leq V_{CC} + 0.3V$ [2]
Output voltage	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_O \leq V_{CC} + 0.3V$ [2]
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins [3]
Total Maximum Clamp Current	$\Sigma I_{CLAMP} $	-	40	mA	Applicable to general purpose I/O pins [3]
"L" level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
"L" level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
"L" level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
"L" level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
"H" level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
"H" level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
"H" level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
"H" level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices in QFP package) [4]	P_D	-	430 ^[5]	mW	$T_A = 105^\circ\text{C}$
		-	750 ^[5]	mW	$T_A = 90^\circ\text{C}$
		-	540 ^[5]	mW	$T_A = 125^\circ\text{C}$, no Flash program/erase [6]
Permitted Power dissipation (CY96F346/F347/F348 in LQFP package) [4]	P_D	-	375 ^[5]	mW	$T_A = 105^\circ\text{C}$
		-	750 ^[5]	mW	$T_A = 85^\circ\text{C}$
		-	470 ^[5]	mW	$T_A = 125^\circ\text{C}$, no Flash program/erase [6]
		-	560 ^[5]	mW	$T_A = 120^\circ\text{C}$, no Flash program/erase [6]
Permitted Power dissipation (CY96F345 in LQFP package) [4]	P_D	-	335 ^[5]	mW	$T_A = 105^\circ\text{C}$
		-	670 ^[5]	mW	$T_A = 85^\circ\text{C}$
		-	840 ^[5]	mW	$T_A = 75^\circ\text{C}$
		-	420 ^[5]	mW	$T_A = 125^\circ\text{C}$, no Flash program/erase [6]
		-	590 ^[5]	mW	$T_A = 115^\circ\text{C}$, no Flash program/erase [6]

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted Power dissipation (Mask ROM devices) ^[4]	P_D	-	350	mW	$T_A=105^{\circ}\text{C}$
		-	360	mW	$T_A=125^{\circ}\text{C}$ ^[6]
Operating ambient temperature	T_A	0	+70	$^{\circ}\text{C}$	CY96V300B
		-40	+105		
		-40	+125		^[6]
Storage temperature	T_{STG}	-55	+150	$^{\circ}\text{C}$	

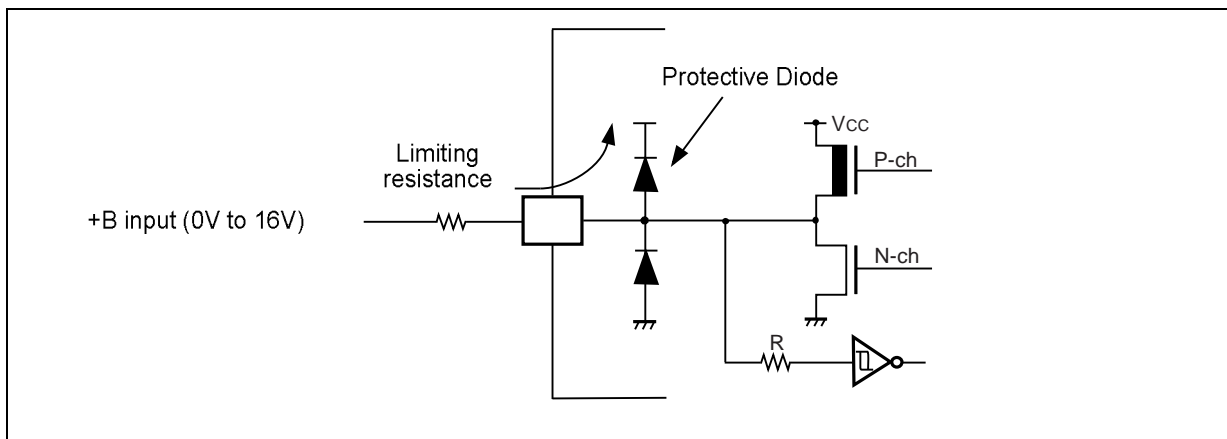
[1]: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

[2]: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC} .

[3]:

- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

Sample recommended circuits:



[4]: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB. The actual power dissipation depends on the customer application and can be calculated as follows:

$$P_D = P_{IO} + P_{INT}$$

$$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH}) \text{ (IO load power dissipation, sum is performed on all IO ports)}$$

$$P_{INT} = V_{CC} * (I_{CC} + I_A) \text{ (internal power dissipation)}$$

I_{CC} is the total core current consumption into V_{CC} as described in the "DC characteristics" and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator. I_A is the analog current consumption into AV_{CC} .

[5]: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

[6]: Please contact Cypress for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed any of these ratings.

14.2 Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	μF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

14.3 DC characteristics

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$0.7 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} \geq 4.5\text{V}$
				$0.74 V_{CC}$	-	$V_{CC} + 0.3$	V	$V_{CC} < 4.5\text{V}$
			AUTOMOTIVE Hys- teresis input selected	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	
			TTL input selected	2.0	-	$V_{CC} + 0.3$	V	
	V_{IHx0F}	X0	External clock in "Fast Clock Input mode"	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	Not available in CY96F34xY/R/AxA
	V_{IHx0S}	X0,X1, X0A,X1A	External clock in "oscil- lation mode"	2.5	-	$V_{CC} + 0.3$	V	
	V_{IHR}	RSTX	-	$0.8 V_{CC}$	-	$V_{CC} + 0.3$	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	$V_{CC} - 0.3$	-	$V_{CC} + 0.3$	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	
			CMOS Hysteresis 0.7/0.3 input selected	$V_{SS} - 0.3$	-	$0.3 V_{CC}$	V	
			AUTOMOTIVE Hys- teresis input selected	$V_{SS} - 0.3$	-	$0.5 V_{CC}$	V	$V_{CC} \geq 4.5\text{V}$
				$V_{SS} - 0.3$	-	$0.46 V_{CC}$		$V_{CC} < 4.5\text{V}$
			TTL input selected	$V_{SS} - 0.3$	-	0.8	V	
	V_{ILx0F}	X0	External clock in "Fast Clock Input mode"	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	Not available in CY96F34xY/R/AxA
	V_{ILx0S}	X0,X1, X0A,X1A	External clock in "oscillation mode"	$V_{SS} - 0.3$	-	0.4	V	
	V_{ILR}	RSTX	-	$V_{SS} - 0.3$	-	$0.2 V_{CC}$	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	$V_{SS} - 0.3$	-	$V_{SS} + 0.3$	V	
Output H voltage	V_{OH2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -2\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -1.6\text{mA}$					
	V_{OH5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -5\text{mA}$	$V_{CC} - 0.5$	-	-	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -3\text{mA}$					
	V_{OH3}	3mA outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OH} = -3\text{mA}$	$V_{CC} - 0.5$	-	-	V	
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OH} = -2\text{mA}$					

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL2}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +2\text{mA}$	-	-	0.4	V	Driving strength set to 2mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OL} = +1.6\text{mA}$					
	V_{OL5}	Normal outputs	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +5\text{mA}$	-	-	0.4	V	Driving strength set to 5mA
			$3.0\text{V} \leq V_{CC} < 4.5\text{V}$ $I_{OL} = +3\text{mA}$					
	V_{OL3}	3mA outputs	$3.0\text{V} \leq V_{CC} \leq 5.5\text{V}$ $I_{OL} = +3\text{mA}$	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ $AV_{SS}, AVR_L < V_I < AV_{CC}, AVR_H$	-1	-	+1	μA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	$V_{CC} = 3.3\text{V} \pm 10\%$	40	100	160	k Ω	
			$V_{CC} = 5.0\text{V} \pm 10\%$	25	50	100	k Ω	

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCPLL}	PLL Run mode with $CLKS1/2 = 48\text{MHz}$, $CLKB = CLKP1/2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	35	44	mA	Flash devices at 0 Flash wait states
			+125°C	36	47		
			+25°C	17	23	mA	CY96345/346 at 0 ROM wait states
			+125°C	18	25		
		PLL Run mode with $CLKS1/2 = CLKB = CLKP1 = 56\text{MHz}$, $CLKP2 = 28\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	44	57	mA	CY96F346/F347/F348 at 2 Flash wait states
			+125°C	45	60		
			+25°C	25	35	mA	CY96345/346 at 2 ROM wait states
			+125°C	26	37		
		PLL Run mode with $CLKS1/2 = 72\text{MHz}$, $CLKB = CLKP1 = 36\text{MHz}$, $CLKP2 = 18\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	38	50	mA	CY96F346/F347/F348Y/R/Ayy at 1 Flash wait state
			+125°C	39	53		
		PLL Run mode with $CLKS1/2 = 80\text{MHz}$, $CLKB = CLKP1 = 40\text{MHz}$, $CLKP2 = 20\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	38	51	mA	CY96F345 at 1 Flash wait state
			+125°C	40	54		
		PLL Run mode with $CLKS1/2 = 96\text{MHz}$, $CLKB = CLKP1 = 48\text{MHz}$, $CLKP2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	49	62	mA	CY96F348T/H/CyB/C at 1 Flash wait state
			+125°C	50	65		
			+25°C	26	36	mA	CY96345/346 at 1 ROM wait state
			+125°C	27	38		
	I_{CCMAIN}	Main Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 4\text{MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	4.5	5.5	mA	Flash devices at 1 Flash wait state
			+125°C	5.1	8.5		
			+25°C	2.5	3.5	mA	CY96345/346 at 1 ROM wait state
			+125°C	3.1	5.5		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes ^[1]	I_{CCRCH}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	2.9	4	mA	Flash devices at 1 Flash wait state
			+125°C	3.5	6.5		
			+25°C	1.7	2.7	mA	CY96345/346 at 1 ROM wait state
			+125°C	2.3	4.7		
	I_{CCRCL}	RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.4	0.6	mA	CY96F346/F347/F348 at 1 Flash wait state
			+125°C	0.9	3.5		
			+25°C	0.18	0.3	mA	CY96F345 at 1 Flash wait state
			+125°C	0.68	3.3		
		RC Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 100\text{kHz}$, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25°C	0.4	0.6	mA	CY96345/346 at 1 ROM wait state
			+125°C	0.9	2.4		
			+25°C	0.15	0.25	mA	Flash devices at 1 Flash wait state
			+125°C	0.65	3.2		
			+25°C	0.15	0.25	mA	CY96345/346 at 1 ROM wait state
			+125°C	0.65	2.1		
	I_{CCSUB}	Sub Run mode with $CLKS1/2 = CLKB = CLKP1/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25°C	0.1	0.2	mA	Flash devices at 1 Flash wait state
			+125°C	0.6	3		
			+25°C	0.1	0.2	mA	CY96345/346 at 1 ROM wait state
			+125°C	0.6	2		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes ^[1]	I_{CCSPLL}	PLL Sleep mode with $CLKS1/2 = 48\text{MHz}$, $CLKP1/2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	9	10.5	mA	Flash devices
			+125°C	9.7	13		
			+25°C	8	9.5	mA	CY96345/346
			+125°C	8.7	11.5		
		PLL Sleep mode with $CLKS1/2 =$ $CLKP1 = 56\text{MHz}$, $CLKP2 = 28\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	14	15.5	mA	CY96F346/F347/F348
			+125°C	14.8	18		
			+25°C	13.5	15	mA	CY96345/346
			+125°C	14.3	17		
		PLL Sleep mode with $CLKS1/2 = 72\text{MHz}$, $CLKP1 = 36\text{MHz}$, $CLKP2 = 18\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	10.5	12	mA	CY96F346/F347/F348Y/R/Ayy
			+125°C	11.3	14.5		
		PLL Sleep mode with $CLKS1/2 = 80\text{MHz}$, $CLKP1 = 40\text{MHz}$, $CLKP2 = 20\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	11	13.5	mA	CY96F345
			+125°C	11.7	16		
		PLL Sleep mode with $CLKS1/2 = 96\text{MHz}$, $CLKP1 = 48\text{MHz}$, $CLKP2 = 24\text{MHz}$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	15	16.5	mA	CY96F348T/H/CyB/C
			+125°C	15.8	19		
			+25°C	14	15.5	mA	CY96345/346
			+125°C	14.8	17.5		
	$I_{CCSMAIN}$	Main Sleep mode with $CLKS1/2 =$ $CLKP1/2 = 4\text{MHz}$ (CLKPLL, CLKSC and CLKRC stopped)	+25°C	1.5	1.8	mA	Flash devices
			+125°C	2	4.5		
			+25°C	1.5	1.8	mA	CY96345/346
			+125°C	2	3.8		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes ^[1]	I_{CCSRCH}	RC Sleep mode with $\text{CLKS1}/2 = \text{CLKP1}/2 = 2\text{MHz}$ (CLKMC, CLKPLL and CLKSC stopped)	+25°C	0.9	1.4	mA	Flash devices
			+125°C	1.5	4.1		
			+25°C	0.9	1.4	mA	CY96345/346
			+125°C	1.5	3.1		
	I_{CCSRCL}	RC Sleep mode with $\text{CLKS1}/2 = \text{CLKP1}/2 = 100\text{kHz}$, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.5	mA	CY96F346/F347/F348
			+125°C	0.8	3.4		
			+25°C	0.09	0.2	mA	CY96F345
			+125°C	0.59	3.1		
			+25°C	0.3	0.5	mA	CY96345/346
			+125°C	0.8	2.3		
		RC Sleep mode with $\text{CLKS1}/2 = \text{CLKP1}/2 = 100\text{kHz}$, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.06	0.15	mA	Flash devices
			+125°C	0.56	3		
			+25°C	0.06	0.15	mA	CY96345/346
			+125°C	0.56	1.9		
	I_{CCSSUB}	Sub Sleep mode with $\text{CLKS1}/2 = \text{CLKP1}/2 = 32\text{kHz}$ (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.04	0.12	mA	Flash devices
			+125°C	0.54	2.9		
			+25°C	0.04	0.12	mA	CY96345/346
			+125°C	0.54	1.85		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes ^[1]	I_{OCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25°C	1.6	2	mA	Flash devices
			+125°C	2.1	5		
			+25°C	1.6	2	mA	CY96345/346
			+125°C	2.1	4		
	$I_{OCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	CY96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	CY96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	CY96345/346
			+125°C	0.85	2.3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15		CY96345/346
			+125°C	0.6	1.9		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.35	0.5	mA	CY96F346/F347/F348
			+125°C	0.85	3.3		
			+25°C	0.13	0.2	mA	CY96F345
			+125°C	0.63	3		
			+25°C	0.35	0.5	mA	CY96345/346
			+125°C	0.85	2.3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.1	0.15	mA	Flash devices
			+125°C	0.6	2.9		
			+25°C	0.1	0.15	mA	CY96345/346
			+125°C	0.6	1.9		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes ^[1]	I_{CCTROL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25°C	0.3	0.45	mA	CY96F346/F347/F348
			+125°C	0.8	3.2		
			+25°C	0.08	0.15	mA	CY96F345
			+125°C	0.58	2.95		
			+25°C	0.3	0.45	mA	CY96345/346
			+125°C	0.8	2.2		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25°C	0.05	0.1	mA	Flash devices
			+125°C	0.55	2.85		
			+25°C	0.05	0.1	mA	CY96345/346
			+125°C	0.55	1.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25°C	0.03	0.1	mA	Flash devices
			+125°C	0.53	2.85		
			+25°C	0.03	0.1	mA	CY96345/346
			+125°C	0.53	1.85		
Power supply current in Stop Mode	I_{OCH}	VR CR:LPM B[2:0] = 110 _B (Core voltage at 1.8V)	+25°C	0.02	0.08	mA	Flash devices
			+125°C	0.52	2.8		
			+25°C	0.02	0.08	mA	CY96345/346
			+125°C	0.52	1.8		
		VR CR:LPM B[2:0] = 000 _B (Core voltage at 1.2V)	+25°C	0.015	0.06	mA	Flash devices
			+125°C	0.4	2.3		
			+25°C	0.015	0.06	mA	CY96345/346
			+125°C	0.4	1.4		
Power supply current for active Low Voltage detector	I_{COLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	μA	CY96F345 Must be added to all current above
			+25°C	90	140	μA	Other devices Must be added to all current above
			+125°C	100	150		

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current for active Clock modulator	I_{CCLOMO}	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
	$I_{CCDFLASH}$	Current for one Data Flash module		10	20	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC} , AV_{SS} , AVRH, AVRL, V_{CC} , V_{SS}

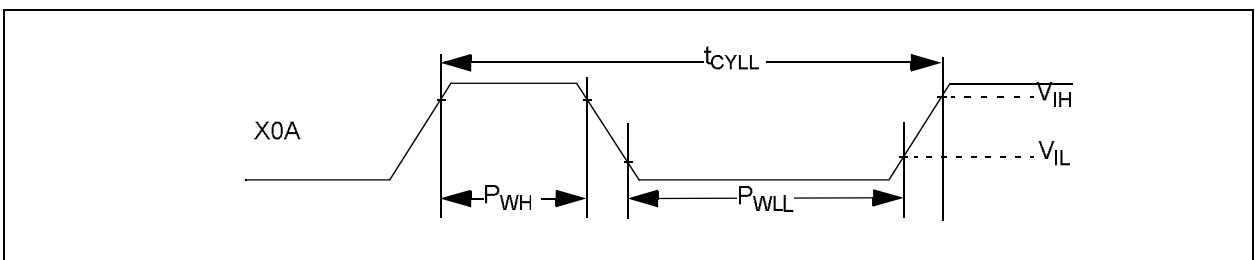
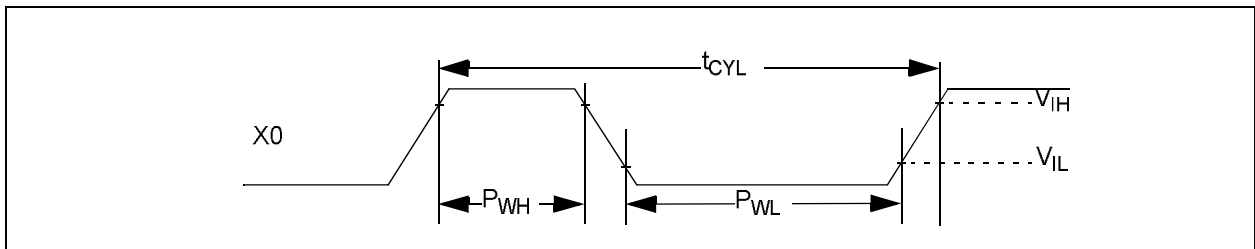
[1]: The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter "Standby mode and voltage regulator control circuit" of the Hardware Manual for further details about voltage regulator control.

14.4 AC Characteristics

14.4.1 Source Clock timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" (not available in CY96F34xY/R/AxA), PLL off
			3.5	-	56	MHz	When using a single phase external clock in "Fast Clock Input mode" (not available in CY96F34xY/R/AxA), PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) $\geq 4\text{MHz}$
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	μs	



14.4.2 Internal Clock timing

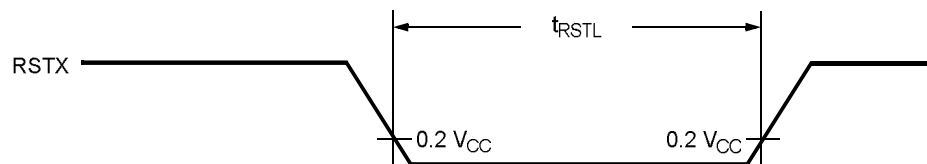
($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f _{CLKS1} , f _{CLKS2}	0	92	0	96	MHz	Others than below
		0	86	0	96	MHz	CY96F348T/H/CxB/C
		0	72	0	80	MHz	CY96F345
		0	68	0	74	MHz	CY96F34xY/R/Axx
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f _{CLKB} , f _{CLKP1}	0	52	0	56	MHz	Others than below
		0	36	0	40	MHz	CY96F345
Internal peripheral clock frequency (CLKP2)	f _{CLKP2}	0	28	0	32	MHz	Others than below
		0	26	0	28	MHz	CY96F34xY/R/Axx

14.4.3 External Reset timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

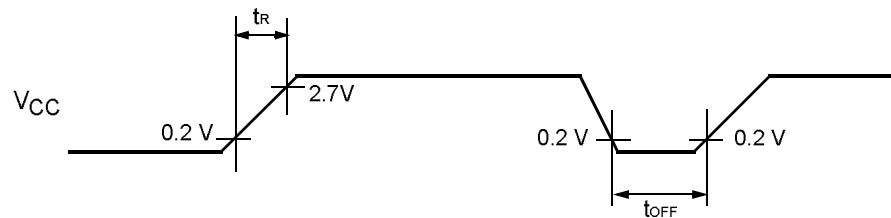
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



14.4.4 Power On Reset timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	V_{CC}	0.05	-	30	ms	
Power off time	t_{OFF}	V_{CC}	1	-	-	ms	



If the power supply is changed too rapidly, a power-on reset may occur.
 We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

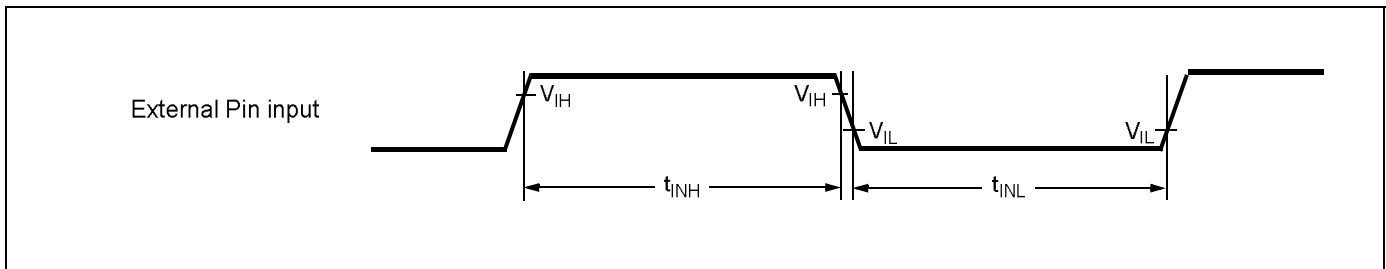


14.4.5 External Input timing

($T_A = -40^{\circ}\text{C}$ to 125°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	-	200	-	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2 \cdot t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)	-	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics



14.4.6 External Bus timing

Note: The values given below are for an I/O driving strength $IO_{drive} = 5\text{mA}$. If IO_{drive} is 2mA , all the maximum output timing described in the different tables must then be increased by 10ns .

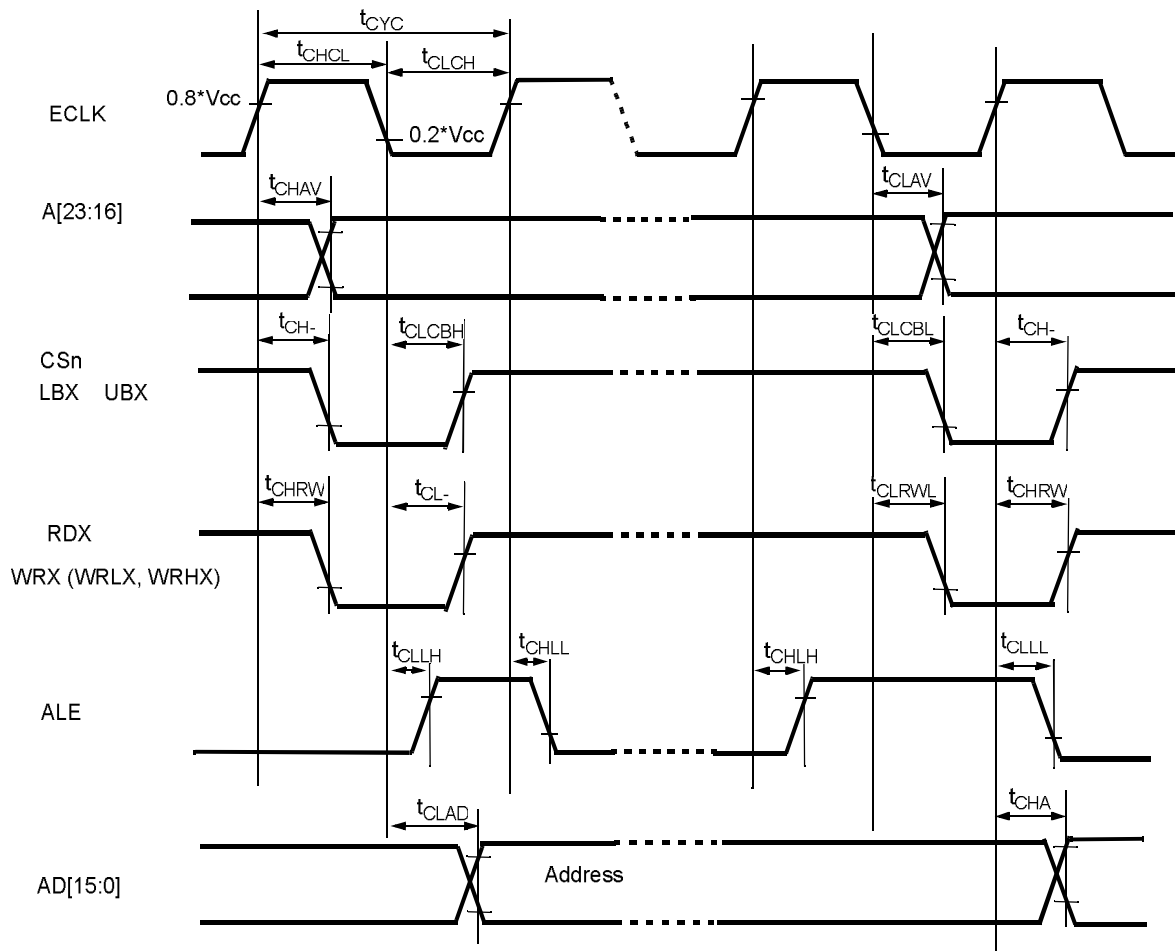
14.4.7 Basic Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	25	-	ns	
	t_{CHCL}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
	t_{CLCH}			$t_{CYC}/2-5$	$t_{CYC}/2+5$		
ECLK → UB _X / LB _X / CS _n time	t_{CHCBH}	CS _n , UB _X , LB _X , ECLK	-	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	-	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWL}	RDX, WRX, WRLX, WRHX, ECLK	-	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	-	30	-	ns	
	t_{CHCL}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
	t_{CLCH}			$t_{CYC}/2-8$	$t_{CYC}/2+8$		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	-	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	-	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	-	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	-	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWL}	RDX, WRX, WRLX, WRHX, ECLK	-	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		



Refer to the Hardware Manual for detailed Timing Charts

14.4.8 Bus Timing (Read)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYD}/2 - 5$	-	ns	
			EACL:STS=1	$t_{CYC} - 5$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYD}/2 - 5$	-		
Valid address \Rightarrow ALE \downarrow time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYD}/2 - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYD}/2 - 15$	-		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYD}/2 - 15$	-	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	-		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYD}/2 - 15$	-		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	-		
ALE $\downarrow \Rightarrow$ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYD}/2 - 15$	-	ns	
			EACL:STS=1	-15	-		
Valid address \Rightarrow RDX \downarrow time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYD}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYD}/2 - 15$	-		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
Valid address \Rightarrow Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYD}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYD}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	-	$3 t_{CYD}/2 - 5$	-	ns	w/o cycle extension
RDX $\downarrow \Rightarrow$ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3 t_{CYD}/2 - 50$	ns	w/o cycle extension
RDX $\uparrow \Rightarrow$ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid \Rightarrow Data hold time	t_{AXDX}	A[23:16], AD[15:0]	-	0	-	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

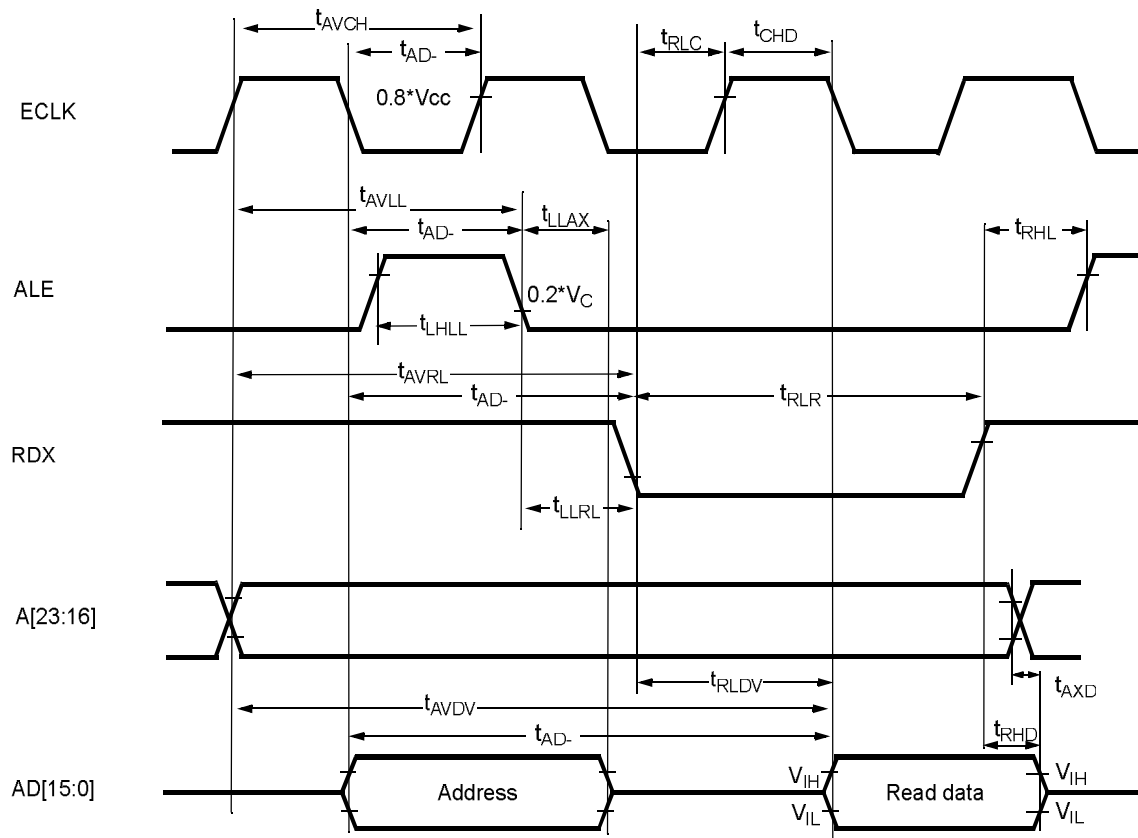
Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
RDX $\uparrow \Rightarrow$ ALE \uparrow time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYD}/2 - 10$	-	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYD}/2 - 10$	-		
Valid address \Rightarrow ECLK \uparrow time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 15$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYD}/2 - 15$	-		
RDX $\downarrow \Rightarrow$ ECLK \uparrow time	t_{RLCH}	RDX, ECLK	-	$t_{CYD}/2 - 10$	-	ns	
ALE $\downarrow \Rightarrow$ RDX \downarrow time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYD}/2 - 10$	-	ns	
			EACL:STS=1	-10	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 50$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t _{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	t _{CYD} /2 – 8	-	ns	
			EACL:STS=1	t _{CYC} – 8	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYD} /2 – 8	-		
Valid address ⇒ ALE ↓ time	t _{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	3t _{CYD} /2 – 20	-		
			EACL:STS=0 and EACL:ACE=1	2t _{CYC} – 20	-		
			EACL:STS=1 and EACL:ACE=1	5t _{CYD} /2 – 20	-		
	t _{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	t _{CYD} /2 – 20	-	ns	
			EACL:STS=1 and EACL:ACE=0	t _{CYC} – 20	-		
			EACL:STS=0 and EACL:ACE=1	3t _{CYD} /2 – 20	-		
			EACL:STS=1 and EACL:ACE=1	2t _{CYC} – 20	-		
ALE ↓ ⇒ Address valid time	t _{LLAX}	ALE, AD[15:0]	EACL:STS=0	t _{CYD} /2 – 20	-	ns	
			EACL:STS=1	-20	-		
Valid address ⇒ RDX ↓ time	t _{AVRL}	RDX, A[23:16]	EACL:ACE=0	3t _{CYD} /2 – 20	-	ns	
			EACL:ACE=1	5t _{CYD} /2 – 20	-		
	t _{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	t _{CYC} – 20	-	ns	
			EACL:ACE=1	2t _{CYC} – 20	-		

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address \Rightarrow Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	-	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1	-	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	-	$5t_{CYD}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1	-	$7t_{CYD}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	-	$3t_{CYD}/2 - 8$	-	ns	w/o cycle extension
RDX $\downarrow \Rightarrow$ Valid data input	t_{RLDV}	RDX, AD[15:0]	-	-	$3t_{CYD}/2 - 55$	ns	w/o cycle extension
RDX $\uparrow \Rightarrow$ Data hold time	t_{RHDX}	RDX, AD[15:0]	-	0	-	ns	
Address valid \Rightarrow Data hold time	t_{AXDX}	A[23:16]	-	0	-	ns	
RDX $\uparrow \Rightarrow$ ALE \uparrow time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYD}/2 - 15$	-	ns	
			other ECL:STS, EA-CL:ACE setting	$t_{CYD}/2 - 15$	-		
Valid address \Rightarrow ECLK \uparrow time	t_{AVCH}	A[23:16], ECLK	-	$t_{CYC} - 20$	-	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYD}/2 - 20$	-		
RDX $\downarrow \Rightarrow$ ECLK \uparrow time	t_{RLCH}	RDX, ECLK	-	$t_{CYD}/2 - 15$	-	ns	
ALE $\downarrow \Rightarrow$ RDX \downarrow time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYD}/2 - 15$	-	ns	
			EACL:STS=1	- 15	-		
ECLK $\uparrow \Rightarrow$ Valid data input	t_{CHDV}	AD[15:0], ECLK	-	-	$t_{CYC} - 55$	ns	



Refer to the Hardware Manual for detailed Timing Charts

14.4.9 Bus Timing (Write)

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

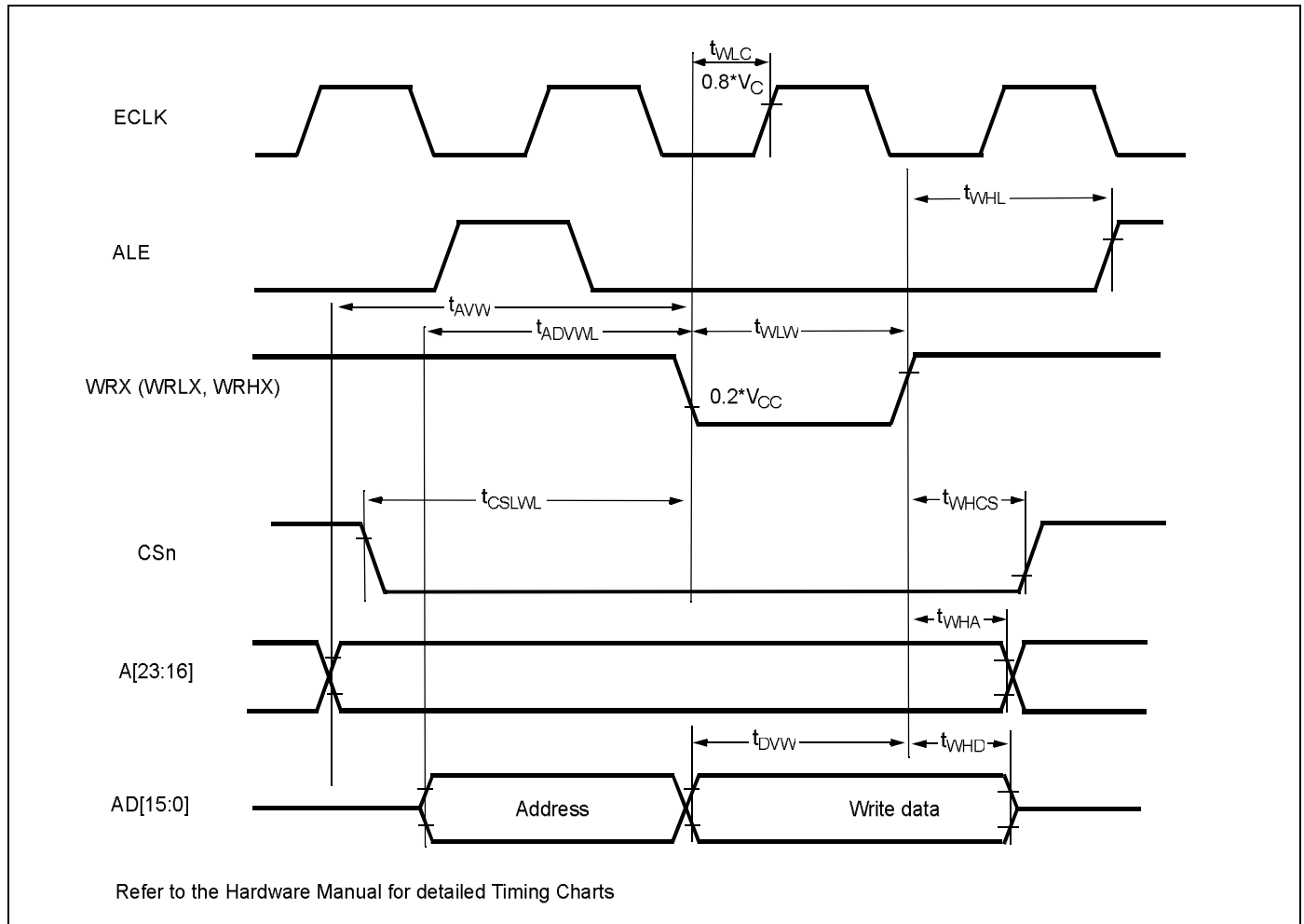
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address \Rightarrow WRX \downarrow time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYD}/2 - 15$	-	ns	
			EACL:ACE=1	$5t_{CYD}/2 - 15$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	-		
WRX pulse width	t_{WLWH}	WRX, WRLX, WRHX	-	$t_{CYC} - 5$	-	ns	w/o cycle extension
Valid data output \Rightarrow WRX \uparrow time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 20$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYD}/2 - 15$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYD}/2 - 15$	-	ns	
WRX $\uparrow \Rightarrow$ ALE \uparrow time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	-		
WRX $\downarrow \Rightarrow$ ECLK \uparrow time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYD}/2 - 10$	-	ns	
CSn \Rightarrow WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYD}/2 - 15$	ns	
			EACL:ACE=1	-	$5t_{CYD}/2 - 15$		
WRX \Rightarrow CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYD}/2 - 15$	-	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address \Rightarrow WRX \downarrow time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYD}/2 - 20$	-	ns	
			EACL:ACE=1	$5t_{CYD}/2 - 20$	-		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	-	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	-		

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX pulse width	t_{WLWH}	WRX, WRLX, WRHX	-	$t_{CYC} - 8$	-	ns	w/o cycle extension
Valid data output \Rightarrow WRX \uparrow time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC} - 25$	-	ns	w/o cycle extension
WRX $\uparrow \Rightarrow$ Data hold time	t_{VHDX}	WRX, WRLX, WRHX, AD[15:0]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ Address valid time	t_{VHAX}	WRX, WRLX, WRHX, A[23:16]	-	$t_{CYC}/2 - 20$	-	ns	
WRX $\uparrow \Rightarrow$ ALE \uparrow time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 15$	-	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 15$	-		
WRX $\downarrow \Rightarrow$ ECLK \uparrow time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	-	$t_{CYC}/2 - 15$	-	ns	
CSn \Rightarrow WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	-	$3t_{CYC}/2 - 20$	ns	
			EACL:ACE=1	-	$5t_{CYC}/2 - 20$		
WRX \Rightarrow CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	-	$t_{CYC}/2 - 20$	-	ns	



14.4.10 Ready Input Timing

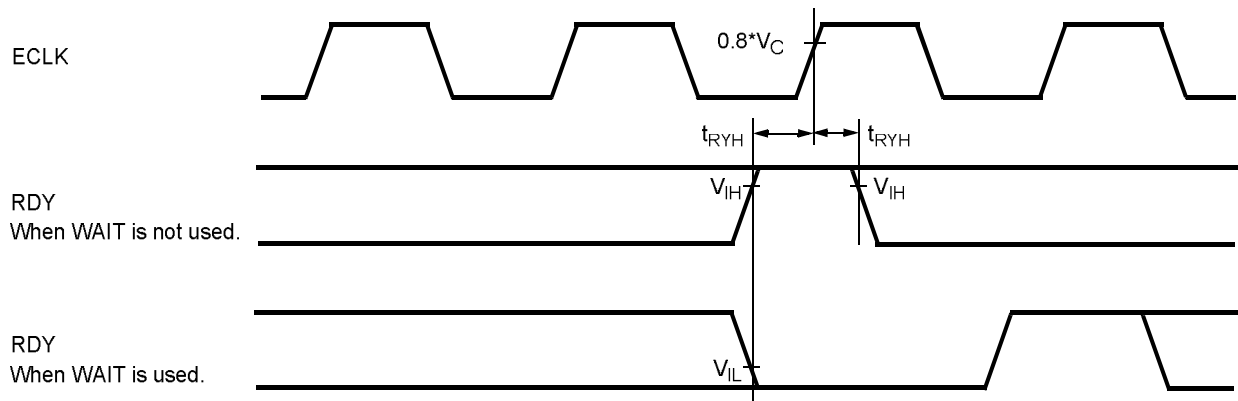
($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	35	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	-	45	-	ns	
RDY hold time	t_{RYHH}	RDY		0	-	ns	

Note: If the RDY setup time is insufficient, use the auto-ready function.



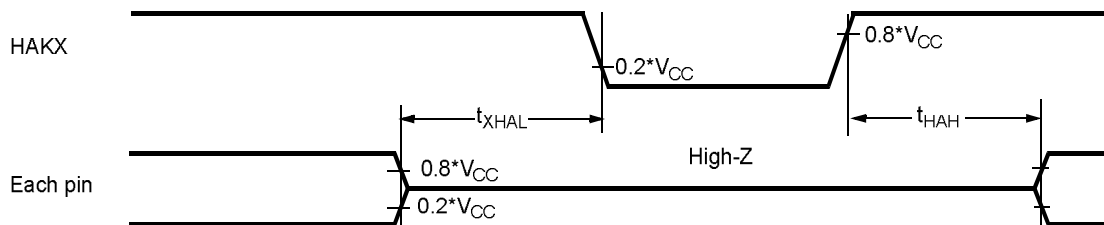
14.4.11 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating \Rightarrow HAKX \downarrow time	t_{XHAL}	HAKX	-	$t_{CYC} - 20$	$t_{CYC} + 20$	ns	
HAKX \uparrow time \Rightarrow Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 20$	$t_{CYC} + 20$	ns	

($T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 3.0$ to 4.5V , $V_{SS} = 0.0\text{ V}$, $I_{Odrive} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating \Rightarrow HAKX \downarrow time	t_{XHAL}	HAKX	-	$t_{CYC} - 25$	$t_{CYC} + 25$	ns	
HAKX \uparrow time \Rightarrow Pin valid time	t_{HAHV}	HAKX		$t_{CYC} - 25$	$t_{CYC} + 25$	ns	



14.4.12 USART timing

WARNING: The values given below are for an I/O driving strength $I_{O_{drive}} = 5\text{mA}$. If $I_{O_{drive}}$ is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

($T_A = -40^\circ\text{C}$ to 125°C , $V_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$, $I_{O_{drive}} = 5\text{mA}$, $C_L = 50\text{pF}$)

Parameter	Symbol	Pin	Condition	$V_{CC} = AV_{CC} = 4.5\text{V to } 5.5\text{V}$		$V_{CC} = AV_{CC} = 3.0\text{V to } 4.5\text{V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	$4 t_{CLKP1}$	-	$4 t_{CLKP1}$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT \rightarrow SCK \uparrow delay time	t_{OVSHI}	SCKn, SOTn		$N * t_{CLKP1} - 20^{[1]}$	-	$N * t_{CLKP1} - 30^{[1]}$	-	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSHI}	SCKn, SINn		$t_{CLKP1} + 45$	-	$t_{CLKP1} + 55$	-	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{LSLSE}	SCKn	External Shift Clock Mode	$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
Serial clock "H" pulse width	t_{SHSLE}	SCKn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2 t_{CLKP1} + 45$	-	$2 t_{CLKP1} + 55$	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2 + 10$	-	$t_{CLKP1}/2 + 10$	-	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK fall time	t_{FE}	SCKn		-	20	-	20	ns
SCK rise time	t_{RE}	SCKn		-	20	-	20	ns

Notes:

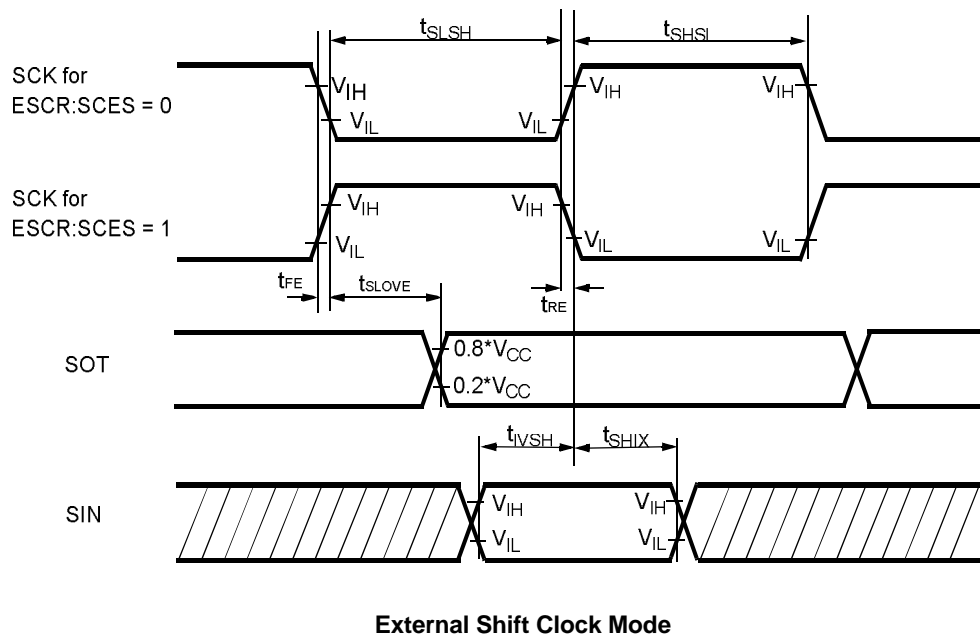
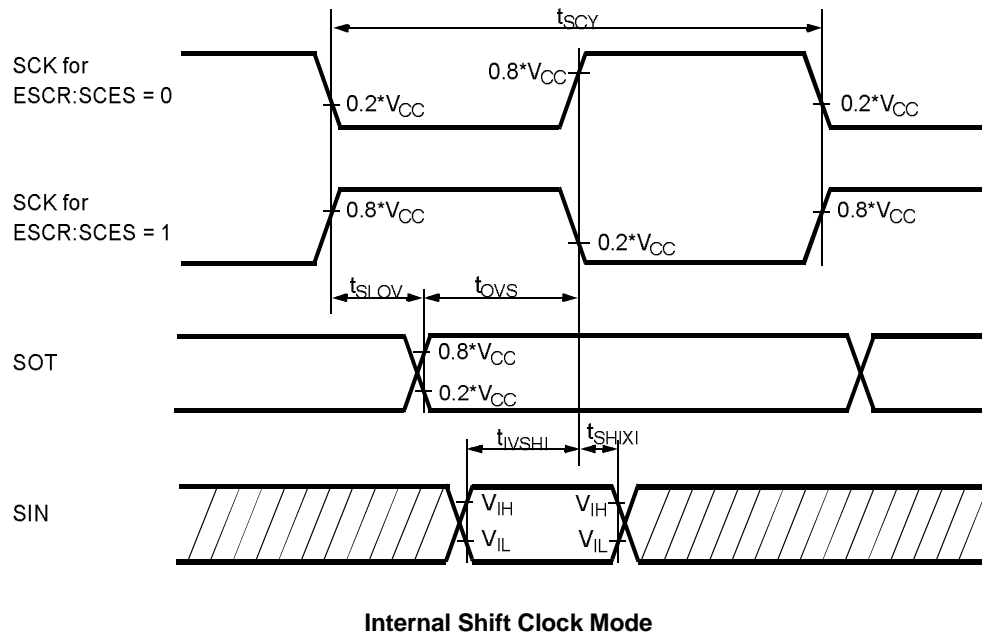
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "CY96300 Super series HARDWARE MANUAL".
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

[1]: Parameter N depends on t_{SCYCI} and can be calculated as follows:

- if $t_{SCYCI} = 2 * k * t_{CLKP1}$, then $N = k$, where k is an integer > 2
- if $t_{SCYCI} = (2 * k + 1) * t_{CLKP1}$, then $N = k + 1$, where k is an integer > 1

Examples:

t_{SCYCI}	N
$4 * t_{CLKP1}$	2
$5 * t_{CLKP1}$	3
$7 * t_{CLKP1}$	4
...	...



14.4.13 I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

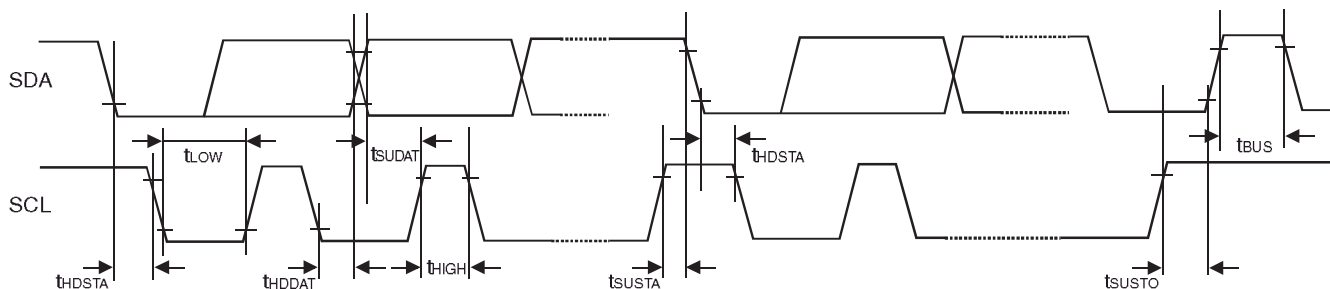
Parameter	Symbol	Condition	Standard-mode		Fast-mode ^[4]		Unit
			Min	Max	Min	Max	
SCL clock frequency	f _{SCL}	R = 1.7 kΩ, C = 50 pF ^[1]	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL→	t _{HDSTA}		4.0	-	0.6	-	μs
"L" width of the SCL clock	t _{LOW}		4.7	-	1.3	-	μs
"H" width of the SCL clock	t _{HIGH}		4.0	-	0.6	-	μs
Set-up time for a repeated START condition SCL↓→SDA↑	t _{SUSTA}		4.7	-	0.6	-	μs
Data hold time SCL↑→SDA↓	t _{HDDAT}		0	3.45 ^[2]	0	0.9 ^[3]	μs
Data set-up time SDA↑↓→SCL↑	t _{SUDAT}		250	-	100	-	ns
Set-up time for STOP condition SCL↑→SDA↑	t _{SUSTO}		4.0	-	0.6	-	μs
Bus free time between a STOP and START condition	t _{BUS}		4.7	-	1.3	-	μs

[1] : R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

[2]: The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

[3] : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met.

[4] : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



14.5 Analog Digital Converter

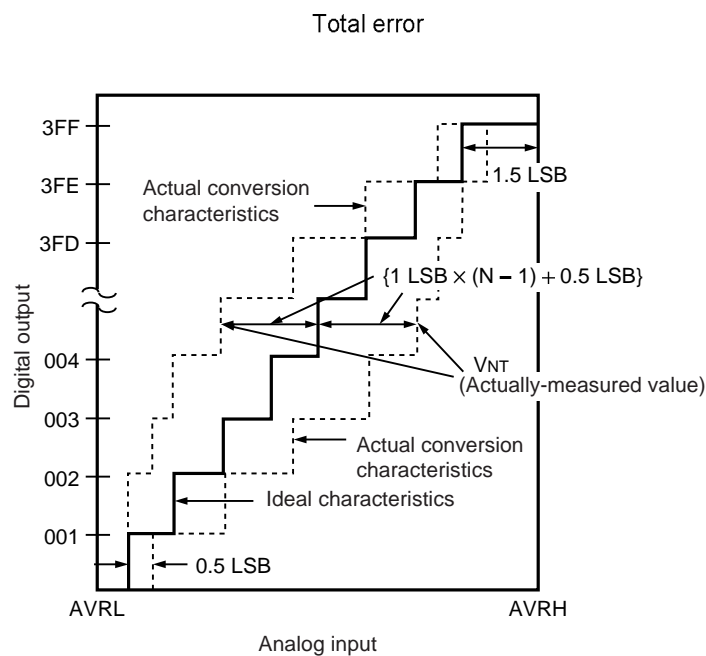
($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $3.0\text{ V} \leq \text{AVRH} - \text{AVRL}$, $V_{CC} = \text{AV}_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = \text{AV}_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	$\text{AVRL} - 1.5\text{ LSB}$	$\text{AVRL} + 0.5\text{ LSB}$	$\text{AVRL} + 2.5\text{ LSB}$	V	
Full scale reading voltage	V_{FST}	ANn	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	-	-	1.0	-	16,500	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			2.0	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Sampling time	-	-	0.5	-	-	μs	$4.5\text{V} \leq \text{AV}_{CC} \leq 5.5\text{V}$
			1.2	-	-	μs	$3.0\text{V} \leq \text{AV}_{CC} < 4.5\text{V}$
Analog port input curren	I_{AIN}	ANn	-3	-	+3	μA	AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog port input curren	I_{AIN}	ANn	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$, AV_{SS} , $\text{AVRL} < V_I < \text{AV}_{CC}$, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH/ AVRL 2	0.75 AV_{CC}	-	AV_{CC}	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AV_{CC}	-	2.5	5	mA	A/D Converter active
	I_{AH}	AV_{CC}	-	-	5	μA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	μA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as $|\text{AVRH} - \text{AVRL}|$ becomes smaller.

14.5.1 Definition of A/D Converter Terms

- **Resolution:** Analog variation that is recognized by an A/D converter.
- **Total error:** Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- **Nonlinearity error:** Deviation between a line across zero-transition line ("00 0000 0000" <--> "00 0000 0001") and full-scale transition line ("11 1111 1110" <--> "11 1111 1111") and actual conversion characteristics.
- **Differential nonlinearity error:** Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- **Zero reading voltage:** Input voltage which results in the minimum conversion value.
- **Full scale reading voltage:** Input voltage which results in the maximum conversion value.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \times \frac{AVRH - AVRL}{1024} \quad [\text{V}]$$

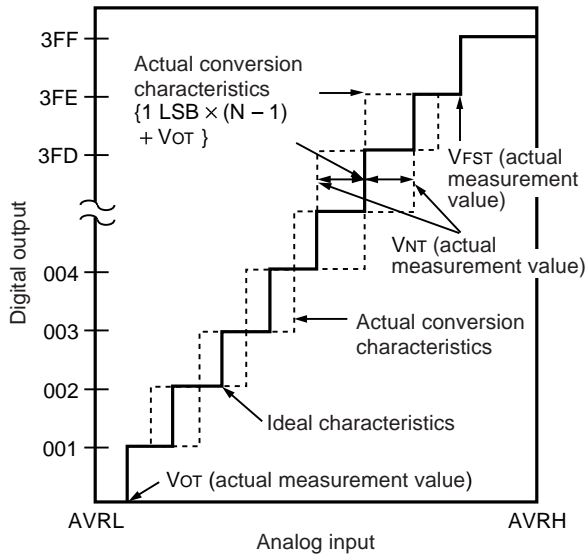
N: A/D converter digital output value

$$V_{OT} (\text{Ideal value}) = AVRL + 0.5 \text{ LSB} \quad [\text{V}]$$

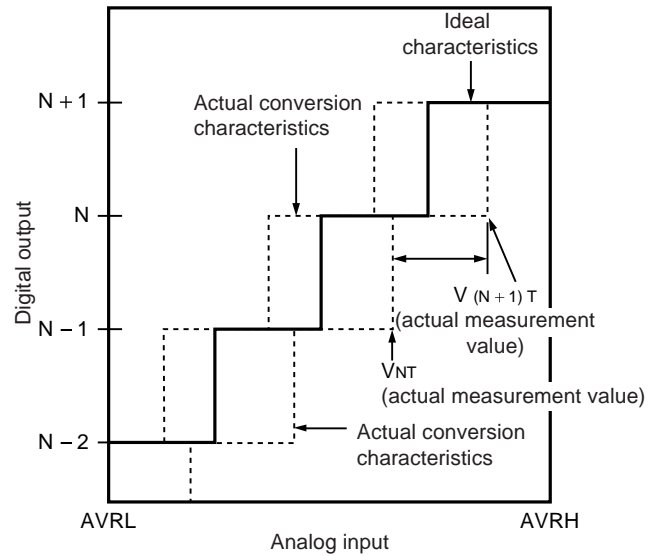
$$V_{FST} (\text{Ideal value}) = AVRH - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : A voltage at which digital output transitions from (N - 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential nonlinearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB} \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

N: A/D converter digital output value

V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."

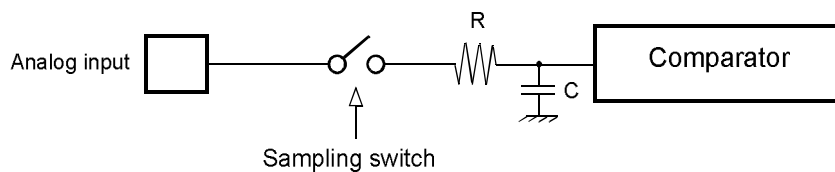
V_{FST} : Voltage at which digital output transits from "3FE_H" to "#FF_H."

14.5.2 Notes on A/D Converter Section

■ About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model:



Reference value:

C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ , where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

$$T_{\text{samp}} [\text{min}] = 7 \times (R_{\text{ext}} + 2.6\text{k}\Omega) \times C \text{ for } 4.5 \leq AV_{\text{cc}} \leq 5.5$$

$$T_{\text{samp}} [\text{min}] = 7 \times (R_{\text{ext}} + 12.1\text{k}\Omega) \times C \text{ for } 3.0 \leq AV_{\text{cc}} \leq 4.5$$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

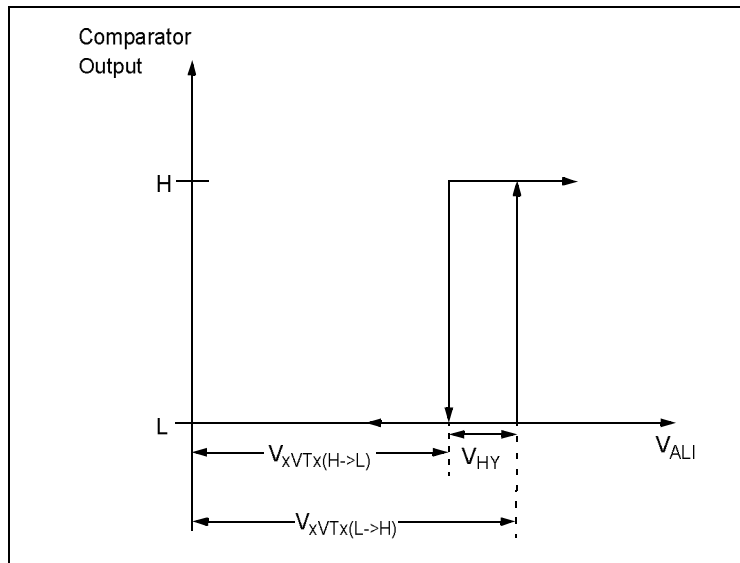
■ About the error

The accuracy gets worse as $|AV_{\text{RH}} - AV_{\text{RL}}|$ becomes smaller.

14.6 Alarm Comparator

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	AV_{CC}	-	25	45	μA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}		-	7	13	μA	Alarm comparator enabled in slow mode (one channel)
	I_{A5ALMH}		-	-	5	μA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM0, ALARM1	-1	-	+1	μA	$T_A = 25\text{ }^{\circ}\text{C}$
			-3	-	+3	μA	$T_A = 125\text{ }^{\circ}\text{C}$
ALARM pin input voltage range	V_{ALIN}		0	-	AV_{CC}	V	
External low threshold high->low transition	$V_{EVTL(H->L)}$		$0.36 * AV_{CC} - 0.25$	$0.36 * AV_{CC} - 0.1$	-	V	INTREF = 0
External low threshold low->high transition	$V_{EVTL(L->H)}$		-	$0.36 * AV_{CC} + 0.1$	$0.36 * AV_{CC} + 0.25$	V	
External high threshold high->low transition	$V_{EVTH(H->L)}$		$0.78 * AV_{CC} - 0.25$	$0.78 * AV_{CC} - 0.1$	-	V	
External high threshold low->high transition	$V_{EVTH(L->H)}$			$0.78 * AV_{CC} + 0.1$	$0.78 * AV_{CC} + 0.25$	V	
Internal low threshold high->low transition	$V_{IVTL(H->L)}$		0.9	1.1	-	V	INTREF = 1
Internal low threshold low->high transition	$V_{IVTL(L->H)}$		-	1.3	1.55	V	
Internal high threshold high->low transition	$V_{IVTH(H->L)}$		2.2	2.4	-	V	
Internal high threshold low->high transition	$V_{IVTH(L->H)}$		-	2.6	2.85	V	
Switching hysteresis	V_{HYS}		50	-	300	mV	
Comparison time	t_{COMPF}		-	0.1	1	μs	CMD = 1 (fast)
	t_{COMPS}		-	1	10	μs	CMD = 0 (slow)
Power-up stabilization time after enabling alarm comparator	t_{PD}		-	1	5	ms	Threshold levels specified above are not guaranteed within this time
Slow/Fast mode transition time	t_{CMD}		-	100	500	μs	



14.7 Low Voltage Detector Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = AV_{CC} = 3.0\text{V} - 5.5\text{V}$, $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Symbol	Value [1]		Value [2]		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	μs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

[1]: valid for all devices except devices listed under "[2]"

[2]: valid for: CY96F345

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

For correct detection, the slope of the voltage level must satisfy $\left| \frac{dV}{dt} \right| \leq 0.004 \frac{\text{V}}{\mu\text{s}}$.

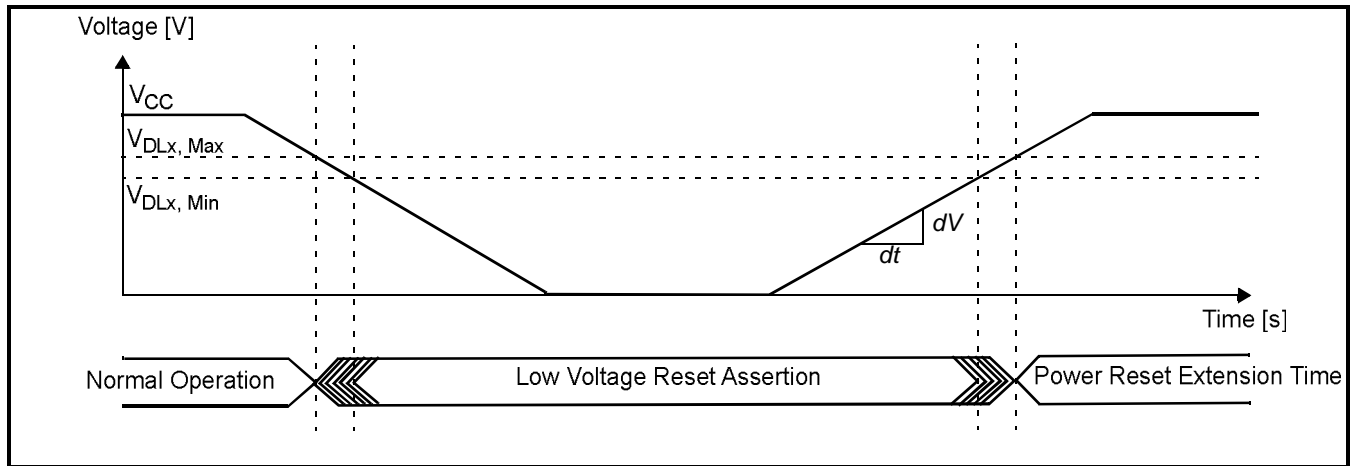
Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of $V_{CC} = 2.7\text{V}$. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

14.7.1 Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup

behavior, please refer to the corresponding hardware manual chapter.



14.8 Flash Memory Program/erase Characteristics

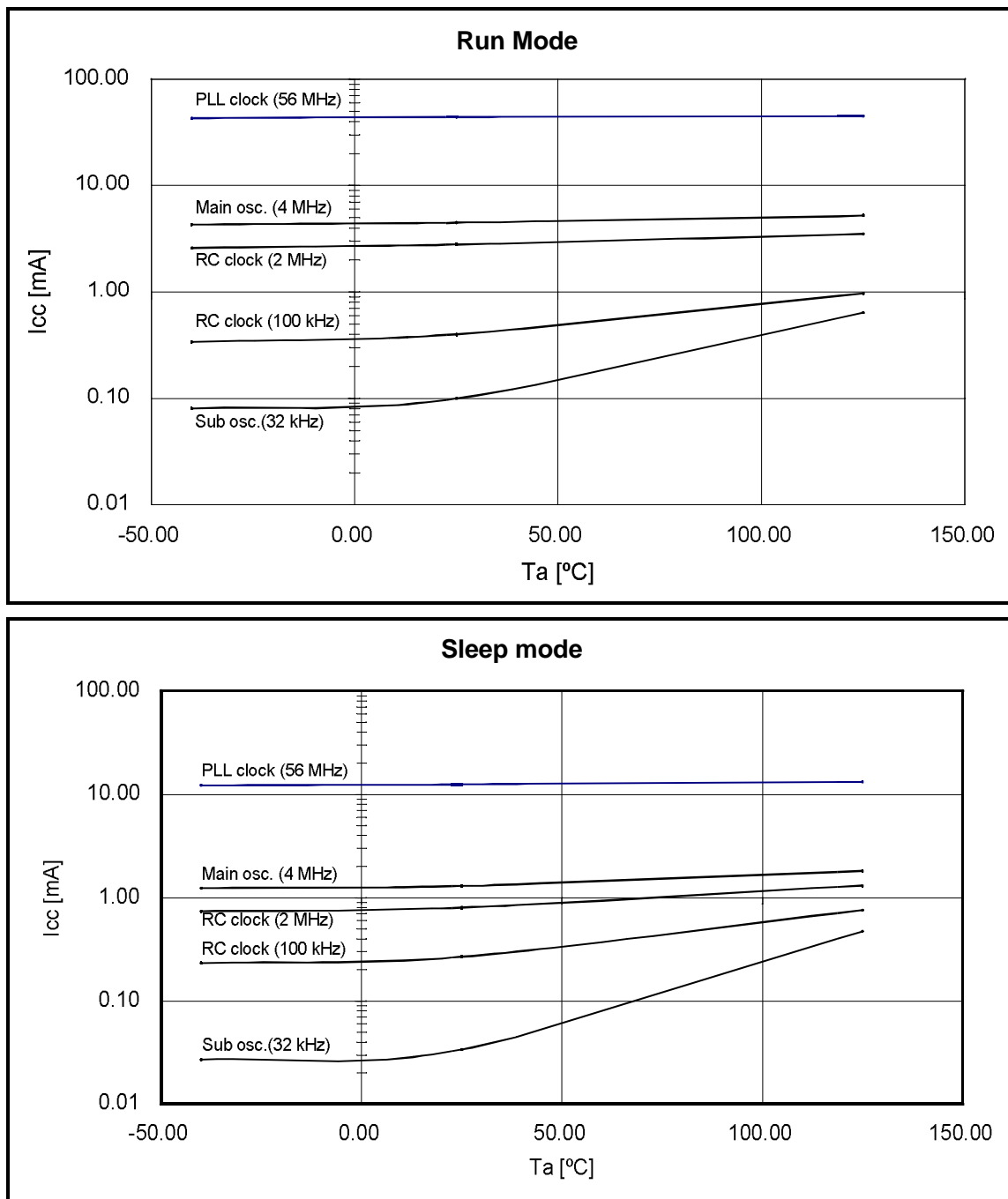
($T_A = -40^{\circ}\text{C}$ to 105°C , $V_{CC} = AV_{CC} = 3.0\text{V}$ to 5.5V , $V_{SS} = AV_{SS} = 0\text{V}$)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time Program/Data Flash (Main Flash)	-	0.9	3.6	s	Without erasure pre-programming time
Sector erase time Data Flash	-	0.5	2	s	Without erasure pre-programming time
	-	0.8	3.6	s	Including erasure pre-programming time
Chip erase time Program/Data Flash (Main Flash)	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Chip erase time Data Flash	-	2.5	10	s	Without erasure pre-programming time
	-	3.7	16.4	s	Including erasure pre-programming time
Word (16-bit width) programming time Program/Data Flash (Main Flash)	-	23	370	us	Without overhead time for submitting write command
Byte (8-bit width) programming time Data Flash	-	15	100	us	Without overhead time for submitting write command
Program/Erase cycle	10000	-	-	cycle	100 000 Program/Erase cycles are under evaluation by Cypress
Flash data retention time	20	-	-	year	[1]

[1]: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

15. Example Characteristics

The diagrams below show the characteristics of one measured sample with typical process parameters.



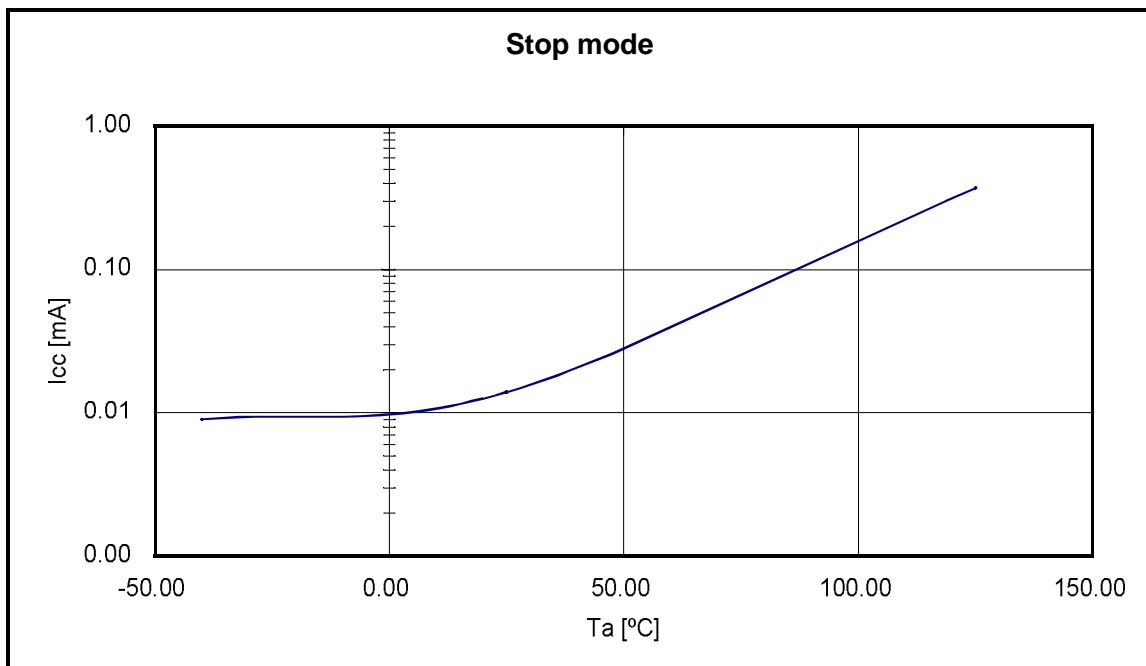
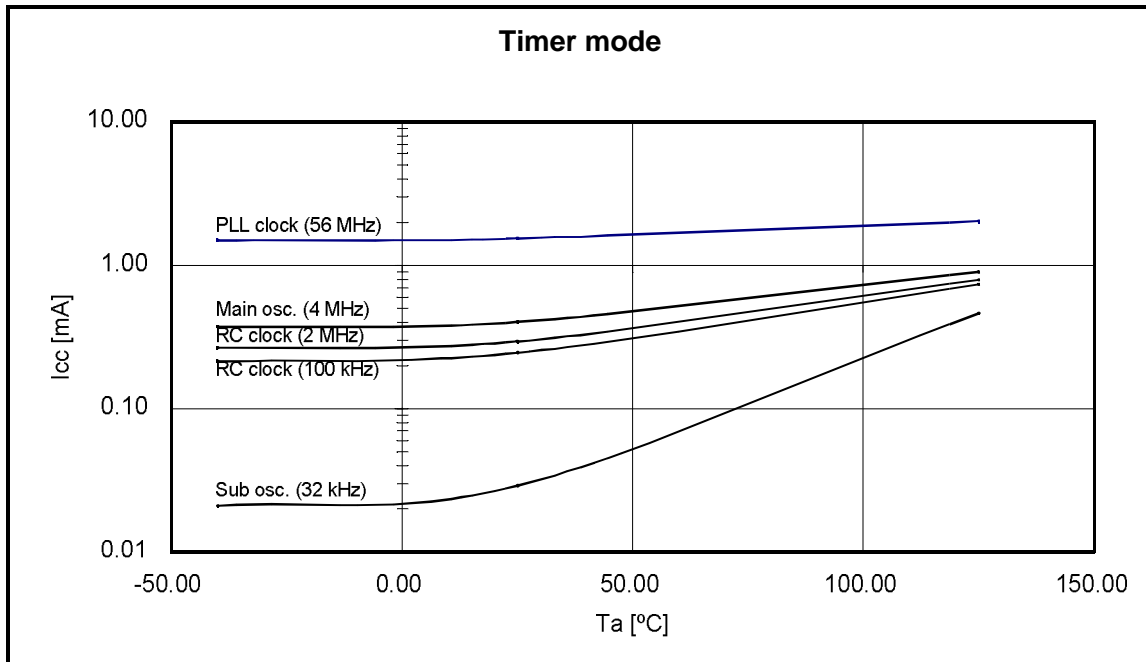


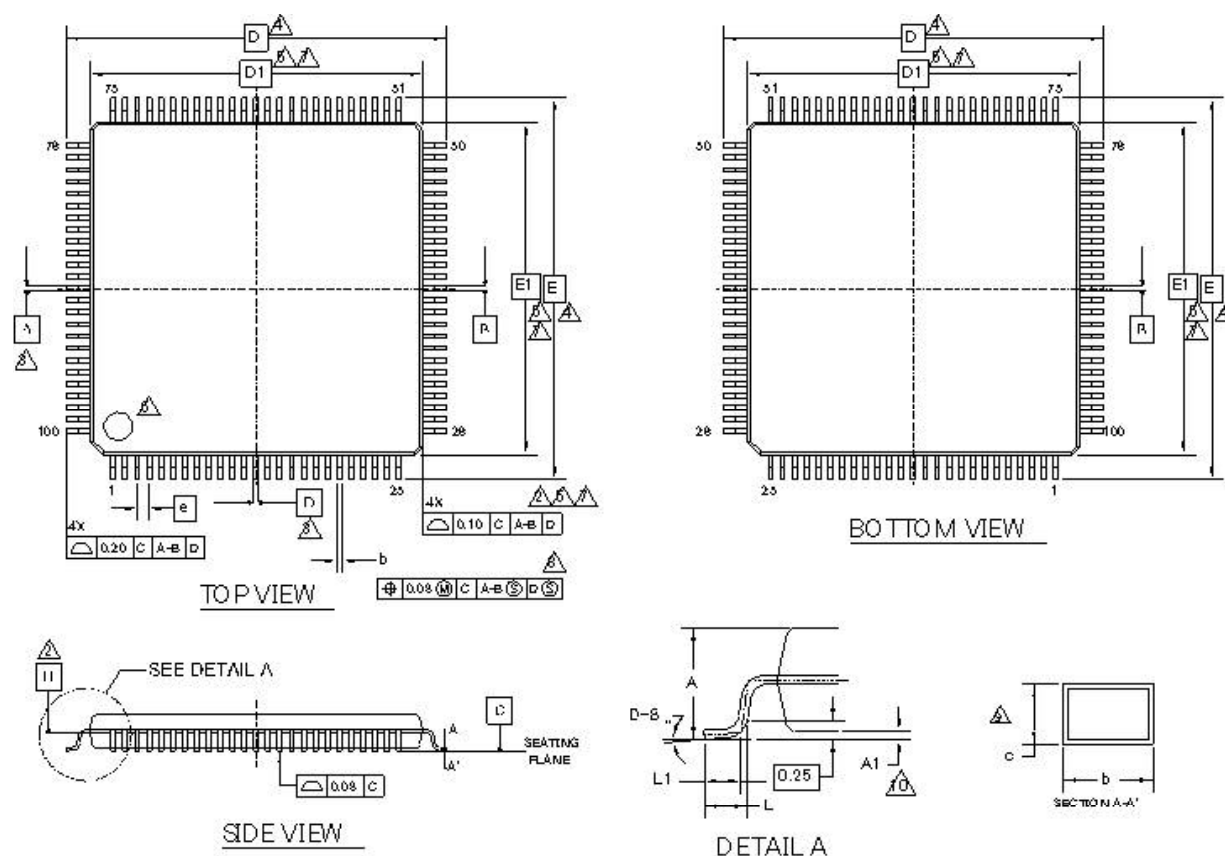
Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

Table 6: Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

16. Package Dimension CY96(F)34x LQFP 100P



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
- △ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- △ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- △ TO BE DETERMINED AT SEATING PLANE.
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE.
DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- △ DETAILS OF FINISH ENTIRE ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- △ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLD BODY.
- △ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- △ O₁ IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 *A

PACKAGE OUTLINE, 100 LEAD QFP
14.00x14.00x1.7 MM LQFP100 REV00.0

[illegible]

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D	23.90 BSC		
D1	20.00 BSC		
e	0.65 BSC		
E	17.90 BSC		
E1	14.00 BSC		
θ	0°	—	8°
L	0.73	0.88	1.03
L1	1.95 REF		
L2	0.25 BSC		

1. ALL DIMENSIONS ARE IN MILLIMETERS.
- △ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- △ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- △ TO BE DETERMINED AT SEATING PLANE C.
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- △ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- △ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- △ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- △ 10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

18. Ordering Information

18.1 MCU with CAN Controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
CY96345RSAPMC-GSE1	ROM (160KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96346RSAPMC-GSE2	ROM (288KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F345DSBPMC-GS-UJE1	Flash A (160KB) Data Flash A (64KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F346RSAPMCR-GS-UJE2	Flash A (288KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F346RWAPMCR-GS-UJE2		Yes		
CY96F346RSAPQCR-GS-UJE2		No	No	100 pin Plastic QFP (PQH100)
CY96F346RWAPQCR-GS-UJE2		Yes		
CY96F346RSBPMC-GS-UJE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F346RWBPMC-GS-UJE2		Yes		
CY96F346RSBPQC-GS-UJE2		No	No	100 pin Plastic QFP (PQH100)
CY96F346RWBPQC-GS-UJE2		Yes		
CY96F346RSCPMC-GS-UJE1		No	No	100 pin Plastic LQFP (LQI100)
CY96F347RSAPQCR-GS-UJE2	Flash A (416KB)	No	No	100 pin Plastic QFP (PQH100)
CY96F347RSBPMC-GS-UJE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F348RSAPMCR-GS-UJE2	Flash A (544KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F348RSAPQCR-GS-UJE2				100 pin Plastic QFP (PQH100)
CY96F348RSBPMC-GS-UJE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F348RSBPQC-GS-UJE2				100 pin Plastic QFP (PQH100)
CY96F348RSBPQCR-GS-UJE2				
CY96F348RWCPMC-G-UJE2		Yes	No	100 pin Plastic LQFP (LQI100)
CY96F348HSBPMCR-GSE2	Flash A (544KB) Flash B (32KB)	No	No	100 pin Plastic LQFP (LQI100)
CY96F348HSBPQCR-GSE2		No	No	100 pin Plastic QFP (PQH100)
CY96F348HSCPMC-GSE2		No	No	100 pin Plastic LQFP (LQI100)
CY96F348HSCPMC-GSE1		No	No	100 pin Plastic LQFP (LQI100)
CY96F348HSBPQC-GSE2		No	No	100 pin Plastic QFP (PQH100)

18.2 MCU without CAN Controller

Part number	Flash/ROM	Subclock	Package
CY96F346ASBPMCR-GS-UJE2	Flash A (288KB)	No	100 pin Plastic LQFP (LQ1100)
CY96F346ASBPQC-G-UJE2			100 pin Plastic QFP (PQH100)
CY96F347ASBPMC-GS-UJE2	Flash A (416KB)		100 pin Plastic LQFP (LQ1100)
CY96F348ASBPMC-GS-UJE2	Flash A (544KB)		

This datasheet is also valid for the following outdated devices:

CY96F346YSA, CY96F346YWA,
 CY96F347YSA, CY96F347YWA, CY96F347RWA,
 CY96F348YSA, CY96F348YWA, CY96F348RWA,
 CY96F348TSB, CY96F348TWB, CY96F348HWB,
 CY96F346ASA, CY96F346AWA,
 CY96F347ASA, CY96F347AWA,
 CY96F348ASA, CY96F348AWA,
 CY96F348CSB, CY96F348CWB

19. Major Changes

Page	Section	Change Results
Rev *A		
89	Electrical Characteristics 14.5. Analog Digital Converter	<p>Corrected "Value" and "Unit" of Zero reading voltage. (AVRL - 1.5 → AVRL - 1.5 LSB AVRL + 0.5 → AVRL + 0.5 LSB AVRL + 2.5 → AVRL + 2.5 LSB LSB → V) Corrected "Value" and "Unit" of Full scale reading voltage. (AVRH - 3.5 → AVRH - 3.5 LSB AVRH - 1.5 → AVRH - 1.5 LSB AVRH + 0.5 → AVRH + 0.5 LSB LSB → V)</p>
Rev *B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
1	-	Deleted the following comment. MB96F345: These devices are under development and specification is preliminary. These products under development may change its specification without notice.
7	1. Product Lineup	Deleted the following comment. [1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.
63	14. Electrical Characteristics 14.3 DC characteristics	<p>Updated below I_{CCPLL} value for MB96F345 at 1 Flash wait state.</p> <p>"PLL Run mode with $CLKS1/2 = 80MHz$, $CLKB = CLKP1 = 40MHz$, $CLKP2 = 20MHz$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)"</p> <p>"$T_A = +25\text{ }^{\circ}C$" (before) Typ: TBD Max: TBD (after) Typ: 38 Max: 51</p> <p>"$T_A = +125\text{ }^{\circ}C$" (before) Typ: TBD Max: TBD (after) Typ: 40 Max: 54</p>

Page	Section	Change Results
65	14. Electrical Characteristics 14.3 DC characteristics	<p>Updated below I_{CCSPLL} value for MB96F345.</p> <p>"PLL Sleep mode with $CLKS1/2 = 80MHz$, $CLKP1 = 40MHz$, $CLKP2 = 20MHz$ (CLKRC and CLKSC stopped. Core voltage at 1.9V)"</p> <p>"$T_A = +25\text{ }^{\circ}C$" (before) Typ: TBD Max: TBD (after) Typ: 11 Max: 13.5</p> <p>"$T_A = +125\text{ }^{\circ}C$" (before) Typ: TBD Max: TBD (after) Typ: 11.7 Max: 16</p>
10 101 103, 104	3. Pin Assignment 16. Package Dimension CY96(F)34x LQFP 100P 18. Ordering Information	<p>Package description modified to JEDEC description.</p> <p>(before) FPT-100P-M20 (after) LQI100</p>
9 102 103, 104	3. Pin Assignment 17. Package Dimension CY96(F)34x QFP 100P 18. Ordering Information	<p>Package description modified to JEDEC description.</p> <p>(before) FPT-100P-M22 (after) PQH100</p>

Page	Section	Change Results
103, 104	18. Ordering Information	<p>Deleted the following comment.</p> <p>[1]: These devices are under development and specification is preliminary. These products under development may change its specification without notice.</p> <p>Deleted the following part number.</p> <ul style="list-style-type: none"> - MB96345YSA PQC-GSE2 - MB96345RSA PQC-GSE2 - MB96345YWA PQC-GSE2 - MB96345RWA PQC-GSE2 - MB96345YSA PMC-GSE2 - MB96345RSA PMC-GSE2 - MB96345YWA PMC-GSE2 - MB96345RWA PMC-GSE2 - MB96346YSA PQC-GSE2 - MB96346RSA PQC-GSE2 - MB96346YWA PQC-GSE2 - MB96346RWA PQC-GSE2 - MB96346YSA PMC-GSE2 - MB96346YWA PMC-GSE2 - MB96346RWA PMC-GSE2 - MB96F345FSA PQC-GSE2 - MB96F345DSA PQC-GSE2 - MB96F345FWA PQC-GSE2 - MB96F345DWA PQC-GSE2 - MB96F345FSA PMC-GSE2 - MB96F345DSA PMC-GSE2 - MB96F345FWA PMC-GSE2 - MB96F345DWA PMC-GSE2 - MB96F346YSB PQC-GSE2 - MB96F346YWB PQC-GSE2 - MB96F346YSB PMC-GSE2 - MB96F346YWB PMC-GSE2 - MB96F347YSB PQC-GSE2 - MB96F347RSB PQC-GSE2 - MB96F347YWB PQC-GSE2 - MB96F347RWB PQC-GSE2 - MB96F347YSB PMC-GSE2 - MB96F347YWB PMC-GSE2 - MB96F347RWB PMC-GSE2 - MB96F348YSB PQC-GSE2 - MB96F348YWB PQC-GSE2 - MB96F348RWB PQC-GSE2 - MB96F348YSB PMC-GSE2 - MB96F348YWB PMC-GSE2 - MB96F348RWB PMC-GSE2 - MB96F348TSC PQC-GSE2 - MB96F348TWC PQC-GSE2 - MB96F348HWC PQC-GSE2 - MB96F348TSC PMC-GSE2 - MB96F348TWC PMC-GSE2 - MB96F348HWC PMC-GSE2 - MB96V300BRB-ES(for evaluation)

Page	Section	Change Results
103, 104	18. Ordering Information	<p>Deleted the following part number. (Continue)</p> <ul style="list-style-type: none"> - MB96F346ASB PQC-GSE2 - MB96F346AWB PQC-GSE2 - MB96F346ASB PMC-GSE2 - MB96F346AWB PMC-GSE2 - MB96F347ASB PQC-GSE2 - MB96F347AWB PQC-GSE2 - MB96F347AWB PMC-GSE2 - MB96F348ASB PQC-GSE2 - MB96F348AWB PQC-GSE2 - MB96F348AWB PMC-GSE2 - MB96F348CSC PQC-GSE2 - MB96F348CWC PQC-GSE2 - MB96F348CSC PMC-GSE2 - MB96F348CWC PMC-GSE2 <p>Revised the following parts number. (before)</p> <ul style="list-style-type: none"> - MB96346RSA PMC-GSE2 - MB96F346RSB PQC-GSE2 - MB96F346RWB PQC-GSE2 - MB96F346RSB PMC-GSE2 - MB96F346RWB PMC-GSE2 - MB96F347RSB PMC-GSE2 - MB96F348RSB PQC-GSE2 - MB96F348RSB PMC-GSE2 - MB96F348HSC PQC-GSE2 - MB96F348HSC PMC-GSE2 - MB96F347ASB PMC-GSE2 - MB96F348ASB PMC-GSE2 <p>(after)</p> <ul style="list-style-type: none"> - CY96346RSAPMC-GSE2 - CY96F346RSBPQC-GS-UJE2 - CY96F346RWBPQC-GS-UJE2 - CY96F346RSBPMC-GS-UJE2 - CY96F346RWBPMC-GS-UJE2 - CY96F347RSBPMC-GS-UJE2 - CY96F348RSBPQC-GS-UJE2 - CY96F348RSBPMC-GS-UJE2 - CY96F348HSCPQC-GS-UJE2 - CY96F348HSCPMC-GS-UJE2 - CY96F347ASBPMC-GS-UJE2 - CY96F348ASBPMC-GS-UJE2 <p>Added the following parts number.</p> <ul style="list-style-type: none"> - CY96345RSAPMC-GSE1 - CY96F345DSBPMC-GS-UJE1 - CY96F346RSAPMCR-GS-UJE2 - CY96F346RWAPMCR-GS-UJE2 - CY96F346RSAPQCR-GS-UJE2 - CY96F346RWAPQCR-GS-UJE2 - CY96F346RSCPMC-GS-UJE1 - CY96F347RSAPQCR-GS-UJE2 - CY96F348RSAPMCR-GS-UJE2 - CY96F348RSAPQCR-GS-UJE2 - CY96F348RSBPQCR-GS-UJE2 - CY96F348RWCPMC-G-UJE2 - CY96F348HSBPMCR-GSE2 - CY96F348HSBPQCR-GSE2 - CY96F348HSCPMC-GSE1 - CY96F346ASBPMCR-GS-UJE2 - CY96F346ASBPQC-G-UJE2

Page	Section	Change Results
103, 104	18. Ordering Information	<p>Changed and deleted the parts number in Note.</p> <p>(before) MB96F346YSA, MB96F346RSA, MB96F346YWA, MB96F346RWA, MB96F347YSA, MB96F347RSA, MB96F347YWA, MB96F347RWA, MB96F348YSA, MB96F348RSA, MB96F348YWA, MB96F348RWA, MB96F348TSB, MB96F348HSB, MB96F348TWB, MB96F348HWB, MB96F346ASA, MB96F346AWA, MB96F347ASA, MB96F347AWA, MB96F348ASA, MB96F348AWA, MB96F348CSB, MB96F348CWB</p> <p>(after)</p> <p>CY96F346YSA, CY96F346YWA, CY96F347YSA, CY96F347YWA, CY96F347RWA, CY96F348YSA, CY96F348YWA, CY96F348RWA, CY96F348TSB, CY96F348TWB, CY96F348HWB, CY96F346ASA, CY96F346AWA, CY96F347ASA, CY96F347AWA, CY96F348ASA, CY96F348AWA, CY96F348CSB, CY96F348CWB</p>
105	19. Major Changes	<p>Changed section title and section number.</p> <p>(before) 20. Main Changes in this Edition</p> <p>(after) 19. Major Changes</p>
110	20. Revision History	<p>Changed section number.</p> <p>(before) 19. Revision History</p> <p>(after) 20. Revision History</p>

20. Revision History

Revision	Date	Modification
Prelim 1	2007-05-07	Creation
Prelim 2	2007-05-10	External bus hold timing update
Prelim 3	2007-05-23	Electrical characteristics updates
Prelim 4	2007-08-02	Electrical characteristics updates, Product lineup, changes and ordering information
Prelim 5	2007-09-12	Addition of the electrical characteristic examples and the LVD characteristics specifications, updates of the DC characteristics. Pin circuit type drawing modifications.
Prelim 6	2007-11-21	LVD typo correction. Update of the DC characteristics. Typos corrections.
Prelim 7	2007-12-04	Absolute maximum rating asterisks numbering corrected. Typos page 59: Hardware -> Hardware. IO map table regenerated. Typos corrections. IO circuit drawings modified. Renaming of the Main/Satellite Flash into Flash memory A/B. Memory map reworked.
Prelim 8	2008-02-04	<ul style="list-style-type: none"> ■ Satellite Flash -> 32kB Data Flash ■ MB96345 added (under development) ■ MB96F348 TSA/HSA/TWA/HWA removed (outdated devices) ■ Block diagram and pin assignment corrected (existing resource pins) ■ Pin function table corrected ■ I/O circuit type diagrams corrected ■ Memory map cleaned up ■ "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices", "ROM configuration" replaced by "User ROM Memory map for Mask ROM devices" ■ Parallel Flash programming pinning removed ■ IO map table regenerated: <ul style="list-style-type: none"> □ Port register: Naming style corrected □ Memory control registers renamed (Main/Sat -> A/B) □ addresses after 000BFFh removed ■ Absolute maximum ratings: Pd and Ta specified more precisely ■ oscillator input levels in oscillation mode with external clock added ■ Run and Sleep mode currents: 96/48MHz and 72/36MHz settings added ■ Run mode current spec in 48/24MHz mode corrected ■ Maximum CLKs1/2 frequency for all devices correctly specified ■ Maximum CLKP2 for MB96F34xY/R/Axx corrected ■ External bus timings: missing conditions added and readability improved ■ Alarm comparator spec updated (transition voltages defined) ■ MB96V300A removed ■ Ordering information updated ■ Typos and formatting corrected

Revision	Date	Modification
9	2009-01-09	<ul style="list-style-type: none"> ■ Format adjusted to official Cypress datasheet standard (mainly style changes and official notes and disclaimer added) ■ Numbering of Electrical Characteristics subchapters automated ■ Note about devices under development modified ■ I/O map: Note added about reserved addresses ■ ICCSPLL for CLKS1=96MHz mode: increased by 1mA ■ Serial programming interface: Note about handshaking pins improved ■ specified AD converter channel offset to 4LSB ■ package code of MB96V300 corrected in ordering information ■ Added voltage condition to pull-up resistance spec ■ Lineup: Term "Data Flash" replaced by "independent 32KB Flash" ■ Ordering information: column "Independent 32KB Data Flash" replaced by new column "Flash/ROM", column "Remarks" removed ■ Official package dimension drawing with additional notes added ■ Empty pages removed ■ Alarm comparator: Power supply current max values increased, comparison time reduced, mode transition time and power-up stabilization time newly added ■ Handling devices: Notes added about Serial communication and about using ceramic resonators. ■ Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor ■ AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz ■ VOL3 spec improved: spec valid for 3mA load for full Vcc range ■ MB96F345 added ■ Preliminary DC spec of MB96345/346 added ■ Permitted power dissipation of Flash devices in QFP package improved ■ C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted ■ "Preliminary" watermark removed
10	To be released	<ul style="list-style-type: none"> ■ I/O map: IOABK0-5 added at address 000A00H-000A05H ■ Ordering Information: Suffix "A" added to all MB96F345 device versions ■ AD converter I_{AIN} spec improved: 1uA valid up to 105deg, 1.2uA above 105deg

NOTE: Please see "Document History" for later revised information.

Document History

Spanion Publication Number: **DS07-13802-3E**

Document Title: CY96345/346, CY96F346/F347/F348, F²MC-16FX, CY96340 Series, 16-bit Proprietary Microcontroller Datasheet Document Number: 002-04579				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	06/17/2009	Migrated to Cypress and assigned document number 002-04579. No change to document contents or format.
*A	5198948	AKIH	04/01/2016	Updated to Cypress template
*B	6184340	GSHI	05/31/2018	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 3.Pin Assignments 16.Package Dimension 17.Package Dimension 18.Ordering Information Added 19. Major Changes For details, please see 19.Major Changes

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Cypress Semiconductor Automotive Reliability Qualification Report

AEC-Q100 Automotive Qualification Test Plan Report for

Fab25 180nm Technology (CU80F) Product, Grade-1 -40 to 125°C, Grade-2 -40 to 105°C

Contents:

Page 1: Cover Page

Page 2 – 5: AEC-Q100

Page 6: Revision History

Q100 Qualification Test Plan

Automotive Grade Level = 1, 2

MSL = 3

Supplier Name:	CYPRESS	General Specification:	AEC-Q100 Rev. H
Supplier Code:		Supplier Wafer Fabrication:	CYPRESS FAB25
Supplier Part Number:		Supplier Wafer Test:	TERAPROBE
Supplier Contact:		Supplier Assembly Site:	AMKOR TECHNOLOGY JAPAN - USUKI
Supplier Family Type:	QFP	Supplier Final Test Site:	AMKOR TECHNOLOGY JAPAN - USUKI
Device Description:	180nm TECHNOLOGY WITH FLASH	Supplier Reliability Signature:	
PPAP Submission Date:		Customer Test ID:	
Reason for Qualification:	Qualification at Fab25	Customer Part Number:	
Prepared by Signature:	KUMI	Customer Approval Signature:	
	Date: 13 th Feb., 2020		Date:

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP A – ACCELERATED ENVIRONMENT STRESS TESTS

PC	A1	J-STD-020	Preconditioning: (Test @ Rm) SMD only; Moisture Preconditioning for HAST, UHST, TC, Peak Reflow Temp = 260°C -0/+5°C	MSL = 3			MSL = 3	693 Units / 0 Fails (3X Reflow)
HAST	A2	JESD22 A110	Highly Accelerated Stress Test: (Test @ Rm/Hot) 110°C/85%RH, 264hrs	3	77	231	0 of 231	
UHST	A3	JESD22 A118	Unbiased Highly Accelerated Stress Test: (Test @ Rm) 110°C/85%RH, 264hrs	3	77	231	0 of 231	
TC	A4	JESD22 A104	Temperature Cycle: (Test @ Hot) -65°C to 150°C, 500cycles	3	77	231	0 of 231	
PTC	A5	JESD22 A105	Power Temperature Cycle: (Test @ Rm/Hot) -40°C to 125°C, 1000 Cycles	-	-	-	-	
HTSL	A6	JESD22 A103	High Temperature Storage Life: (Test @ Rm/Hot) 150°C, 1000hrs	1	45	45	0 of 45	

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP B – ACCELERATED LIFETIME SIMULATION TESTS

HTOL	B1	JESD22 A108	High Temp Operating Life: (Test @ Rm/Cold/Hot) 125°C, 1000 Hrs	3	77	231	0 of 231	
ELFR	B2	AEC-Q100-008	Early Life Failure Rate: (Test @ Rm/Hot) 125°C, 96 Hrs	3	800	2400	0 of 2400	
EDR	B3	AEC-Q100-005	NVM Endurance & Data Retention Test: (Test @ Rm/Hot) a. 125°C, 100K Cycles + 150°C Bake, 732 Hrs b. 125°C, 100K Cycles + 125°C HTOL, 1K Hrs c. 25°C, 100K Cycles + 25°C Bake, 1K Hrs	3	77(a) 77(b) 77(c)	231(a) 231(b) 231(c)	0 of 693	

TEST GROUP C – PACKAGE ASSEMBLY INTEGRITY TESTS

WBS	C1	AEC-Q100-001	Wire Bond Shear Test: (Cpk > 1.67)	30 bonds	5 parts Min.	30 bonds	4.12	
WBP	C2	Mil-STD-883, Method 2011	Wire Bond Pull: (Cpk > 1.67); Each bonder used	30 bonds	5 parts Min.	30 bonds	3.41	3.41
SD	C3	JESD22 B102	Solderability: (>95% coverage) 8hr steam aging prior to testing	1	15	15	-	
PD	C4	JESD22 B100, JESD22 B108	Physical Dimensions: (Cpk > 1.67)	3	10	30	-	
SBS	C5	AEC-Q100-010 AEC-Q003	Solder Ball Shear: (Cpk > 1.67); 5 balls from min. of 10 devices	-	-	-	-	
LI	C6	JESD22 B105	Lead Integrity: (No lead cracking or breaking); Through-hole only; 10 leads from each of 5 devices	-	-	-	-	

TEST GROUP D – DIE FABRICATION RELIABILITY TESTS

EM	D1	JESD61	Electromigration: Ta=125°C	-	-	-	Pass	Pass 100K Hrs
TDDb	D2	JESD35	Time Dependent Dielectric Breakdown: Ta=125°C	-	-	-	Pass	Pass 100K Hrs

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
HCI	D3	JESD60 & 28	Hot Carrier Injection: 125°C, 25°C	-	-	-	Pass	Pass 100K Hrs
NBTI	D4	JESD90	Negative Bias Temperature Instability: Ta=125°C	-	-	-	Pass	Pass 100K Hrs
SM	D5	JESD61, 87, & 202	Stress Migration: Ta = 125°C	-	-	-	Pass	Pass 100K Hrs

TEST GROUP E- ELECTRICAL VERIFICATION

TEST	E1	User/Supplier Specification	Pre and Post Stress Electrical Test:	All	All	All	All	Performed for all TEST Group-A & B
HBM	E2	AEC-Q100-002	Electrostatic Discharge, Human Body Model: (Test @ Rm/Hot); (2KV HBM / Class 2 or better)	1	3	3	0 of 3	
CDM	E3	AEC-Q100-011	Electrostatic Discharge, Charged Device Model: (Test @ Rm/Hot); (750V corner leads, 500V all other leads / Class C4B or better)	1	3	3	0 of 3	
LU	E4	AEC-Q100-004	Latch-Up: (Test @ Rm/Hot) 125°C, +/- 100mA	1	6	6	0 of 6	
ED	E5	AEC-Q100-009 AEC-Q003	Electrical Distributions: (Test @ Rm/Hot/Cold) (where applicable, Cpk > 1.67)	3	30	90	PASS	
FG	E6	AEC-Q100-007	Fault Grading:	-	-	-	-	
CHAR	E7	AEC-Q003	Characterization: (Test @ Rm/Hot/Cold)	-	-	-	-	
EMC	E9	SAE J1752/3	Electromagnetic Compatibility (Radiated Emissions)	-	-	-	-	
SC	E10	AEC Q100-012	Short Circuit Characterization	-	-	-	-	
SER	E11	JESD89-1 JESD89-2 JESD89-3	Soft Error Rate	-	-	-	-	
LF	E12	AEC-Q005	Lead (Pb) Free: (see AEC-Q005)	-	-	-	-	

Test	#	Reference	Test Conditions	Lots	S.S.	Total	Results Lot/Pass/Fail	Comments: (N/A =Not Applicable)
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TEST GROUP F – DEFECT SCREENING TESTS

PAT	F1	AEC-Q001	Process Average Testing: (see AEC-Q001)	-	-	-	-	
SBA	F2	AEC-Q002	Statistical Bin/Yield Analysis: (see AEC-Q002)	-	-	-	-	

TEST GROUP G – CAVITY PACKAGE INTEGRITY TESTS (for Ceramic Package testing only)

MS	G1	JESD22 B104	Mechanical Shock: (Test @ Rm)	1	15	15	of	N/A
VFV	G2	JESD22 B103	Variable Frequency Vibration: (Test @ Rm)	1	15	15	of	N/A
CA	G3	MIL-STD-883 Method 2001	Constant Acceleration: (Test @ Rm)	1	15	15	of	N/A
GFL	G4	MIL-STD-883 Method 1014	Gross and Fine Leak:	1	15	15	of	N/A
DROP	G5	-----	Drop Test: (Test @ Rm) MEMS cavity parts only. Drop part on each of 6 axes once from a height of 1.2m onto a concrete surface.	1	5	5	of	N/A
LT	G6	MIL-STD-883 Method 2004	Lid Torque:	1	5	5	of	N/A
DS	G7	MIL-STD-883 Method 2019	Die Shear:	1	5	5	of	N/A
IWV	G8	MIL-STD-883 Method 1018	Internal Water Vapor:	1	5	5	of	N/A

Document History Page

Document Title: AEC-Q100 Automotive Qualification Test Plan Report for Fab25 180nm Technology (CU80F) Product
Document Number: 002-29698

Rev.	ECN No.	Orig. of Change	Description of Change
**	6806393	KUMI	Initial Release (QTP#172504, 188406)

Marketing Part Number	Sample/Replacement Ordering Part #	Package	Sample Availability	LTBD for Old MB MPN	LTSD for Old MB MPN
MB96F346ASBPQC-GE2	CY96F346ASBPQC-G-UJE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21
MB96F346ASBPQC-G-N2E2	CY96F346ASBPQC-G-UJE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21
MB96F346RSAPQCR-GSE2	CY96F346RSAPQCR-GS-UJE2	PQH100	10-Apr-20	7-Oct-20	14-Jun-21
MB96F346RSAPQCR-GS-N2E2	CY96F346RSAPQCR-GS-UJE2	PQH100	10-Apr-20	7-Oct-20	14-Jun-21
MB96F346RSBPQC-GSE2	CY96F346RSBPQC-GS-UJE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21
MB96F346RSBPQC-GS-N2E2	CY96F346RSBPQC-GS-UJE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21
MB96F346RWBPQC-GSE2	CY96F346RWBPQC-GS-UJE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21
MB96F346RWBPQC-GS-N2E2	CY96F346RWBPQC-GS-UJE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21
MB96F347RSAPQCR-GS-ERE2	CY96F347RSAPQCR-GSUJERE2	PQH100	10-Apr-20	7-Oct-20	14-Jun-21
MB96F348RSBPQC-GSE2	CY96F348RSBPQC-GS-UJE2	PQH100	10-Apr-20	7-Oct-20	14-Jun-21
MB96F348RSBPQC-GS-N2E2	CY96F348RSBPQC-GS-UJE2	PQH100	10-Apr-20	7-Oct-20	14-Jun-21
MB96F348RSBPQCR-GS-ERE2	CY96F348RSBPQCR-GSUJERE2	PQH100	Subject to leadtime	7-Oct-20	14-Jun-21