Cypress Semiconductor Corporation, 198 Champion Court, San Jose, CA 95134. Tel: (408) 943-6200

PRODUCT CHANGE NOTIFICATION

PCN:PCN201006 **Date:** March 12, 2020

Subject: Qualification of UMC as an Alternate Wafer Fab Site for Select Industrial-Grade 8Mb MoBL™ SRAM Products

To: PCN Coordinator PCN Coordinator
FUTURE
PCN.System@Future.ca

Description of Change:
Cypress announces the qualification of UMC's 65nm (No. 3, Li-Hsin 2nd Rd., Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.) as an alternate wafer fab site for select 90nm 1.65V – 3.6V industrial grade 8Mb MoBL™ products. The 65nm products are drop-in replacement parts and form, fit, and function compatible with the 90nm 8Mb Async MoBL™ SRAM products manufactured at SkyWater, Minnesota.

There are some updates to certain DC specifications, including a revision in the V_{CC} operating supply current at f = 1MHz (I_{CC}) at 85ºC from 3mA to 7mA and data retention current (I_{CCDR}) at 85ºC from 5µA to 8µA for the 3.0V device and from 3µA to 9µA for the 1.8V device. The updated product datasheets are attached to this notification and can be downloaded from the Cypress Website (www.cypress.com). There is no change to the existing marketing part numbers.

Benefit of Change:
Qualification of alternate manufacturing sites and technologies is part of Cypress' ongoing flexible manufacturing initiative. The goal of the flexible manufacturing initiative is to provide the means for Cypress to continue to meet delivery commitments through dynamic, changing market conditions.

Part Numbers Affected: 22
See the attached 'Affected Parts List' file for a list of all part numbers affected by this change. Note that any new parts that are introduced after the publication of this PCN will include all changes outlined in this PCN.

Qualification Status:
This technology has been qualified through a series of tests documented in the Qualification Test Plan QTP#193601. This qualification report can be found as an attachment to this PCN or by visiting www.cypress.com and typing the QTP number in the keyword search window.

Sample Status:
Qualification samples may not be built ahead of time for all part numbers affected by this change. Please review the attached 'Affected Parts List' file for a list of affected part numbers with their associated sample ordering part numbers. If you require qualification samples, please contact your local Cypress Sales Representative as soon as possible, preferably within 30 days of the date of this PCN, to place any sample orders.

Approximate Implementation Date:
Effective 90 days from the date of this notification, all shipments of the affected part numbers will be fabricated at either SkyWater or UMC.

Anticipated Impact:
None anticipated. Products manufactured at UMC are completely compatible with existing product from form, fit, functional, parametric, and quality performance perspectives.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,
Cypress PCN Administration

CY62157EV30 MoBL

8-Mbit (512K × 16) Static RAM

Features

- Thin small outline package (TSOP) I package configurable as 512K × 16 or 1M × 8 static RAM (SRAM)
- High speed: 45 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
  - Automotive-A: –40 °C to +85 °C
  - Automotive-E: –40 °C to +125 °C
- Wide voltage range: 2.20 V to 3.60 V
- Pin compatible with CY62157DV30
- Ultra low standby power
  - Typical standby current: 2 µA
  - Maximum standby current: 8 µA (Industrial)
- Ultra low active power
  - Typical active current: 6 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary Metal Oxide Semiconductor (CMOS) for optimum speed and power
- Available in Pb-free and non Pb-free 48-ball very fine-pitch ball grid array (VFBGA), Pb-free 44-pin thin small outline package (TSOP) II and 48-pin TSOP I packages

Functional Description

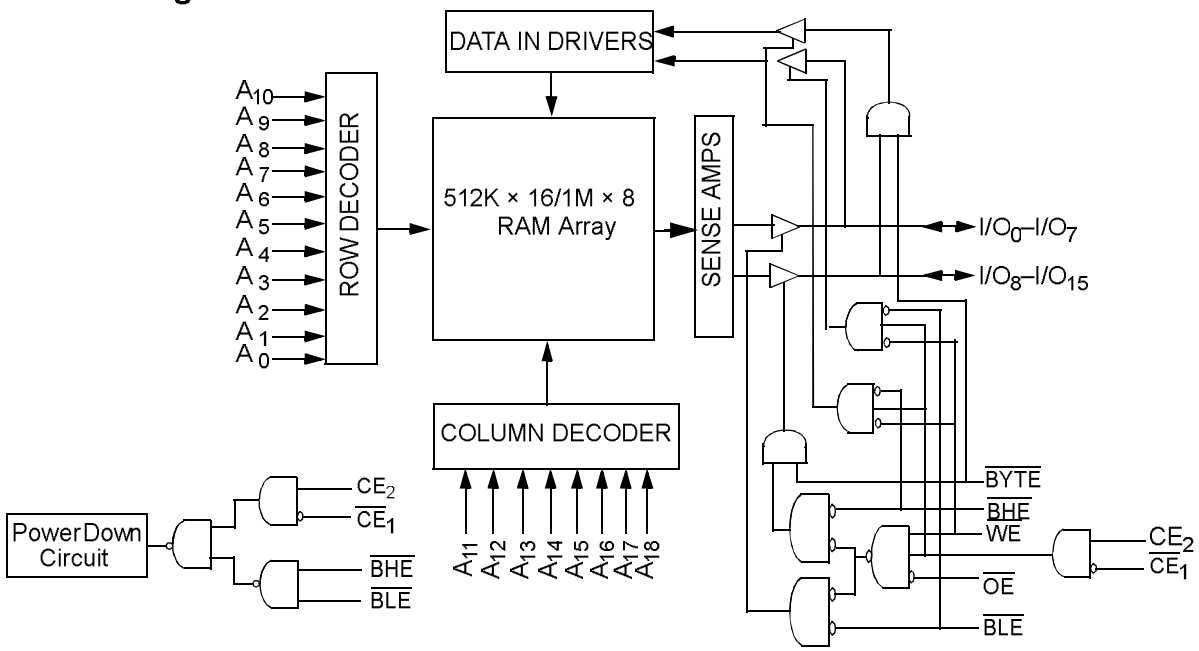
The CY62157EV30 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation is active ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See Truth Table on page 13 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]

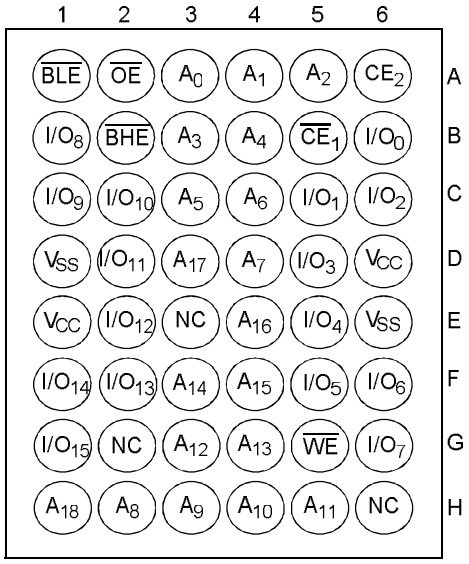


Figure 2. 44-pin TSOP II pinout (Top View) [2]

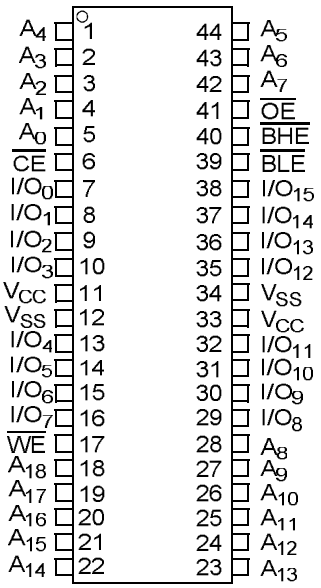
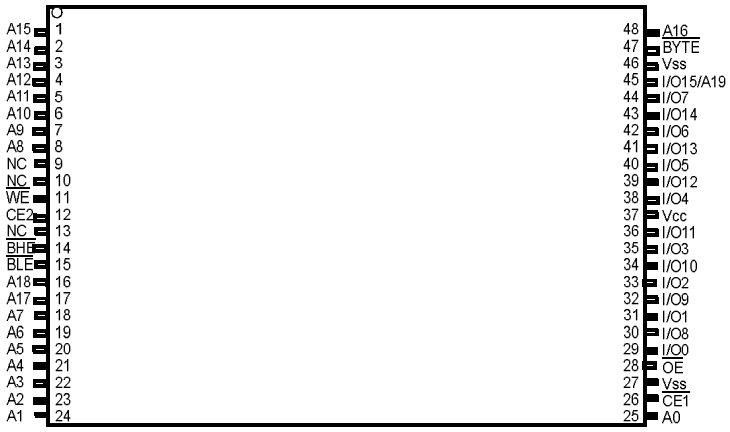


Figure 3. 48-pin TSOP I pinout (Top View) [1, 3]



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [4]	Max		Typ [4]	Max	Typ [4]	Max	Typ [4]	Max
CY62157EV30LL	Industrial/Automotive-A	2.2	3.0	3.6	45	6	7	18	25	2	8
	Automotive-E	2.2	3.0	3.6	55	1.8	4	18	35	2	30

Notes
1. NC pins are not connected on the die.
2. The 44-pin TSOP II package has only one chip enable ($\overline{CE}$) pin.
3. The $\overline{BYTE}$ pin in the 48-pin TSOP I package must be tied HIGH to use the device as a 512K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the $\overline{BYTE}$ signal LOW. In the 1M x 8 configuration, Pin 45 is A19, while $\overline{BHE}$, $\overline{BLE}$ and I/O_8 to I/O_{14} pins are not used.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to + 150 °C

Ambient Temperature with Power Applied ..... –55 °C to + 125 °C

Supply Voltage to Ground Potential .....–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC Voltage Applied to Outputs in High Z State [5, 6] .....–0.3 V to 3.9 V (V_{CCmax} + 0.3 V)

DC Input Voltage [5, 6] .....–0.3 V to 3.9 V ($V_{CC\ max}$ + 0.3 V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-Up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [7]
CY62157EV30LL	Industrial / Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V
	Automotive-E	–40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns (Industrial/ Automotive-A)			55 ns (Automotive-E)			Unit
			Min	Typ [8]	Max	Min	Typ [8]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	2.0	–	–	2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V	2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	–	–	0.4	–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V	–	–	0.4	–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V	1.8	–	V_{CC} + 0.3	1.8	–	V_{CC} + 0.3	V
		V_{CC} = 2.7 V to 3.6 V	2.2	–	V_{CC} + 0.3	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V	–0.3	–	0.6	–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V	–0.3	–	0.8	–0.3	–	0.8	V
I_{IX}	Input leakage current	GND ≤ $V_I \leq V_{CC}$	–1	–	+1	–4	–	+4	µA
I_{OZ}	Output leakage current	GND ≤ $V_O \leq V_{CC}$, Output Disabled	–1	–	+1	–4	–	+4	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$; V_{CC} = V_{CCmax}	–	18	25	–	18	35	mA
		f = 1 MHz; I_{OUT} = 0 mA CMOS levels	–	6	7	–	1.8	4	
I_{SB1} [9]	Automatic CE power down current – CMOS inputs	$\overline{CE_1} \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V	–	2	8	–	2	30	µA
I_{SB2} [9]	Automatic CE power down current – CMOS inputs	$\overline{CE_1} \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V or ($\overline{BHE}$ and $\overline{BLE}$) ≥ V_{CC} – 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V	–	2	8	–	2	30	µA

Notes

5. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
7. Full device AC operation assumes a 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{CC} stabilization.
8. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
9. Chip enables ($\overline{CE_1}$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ (48-pin TSOP I only) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

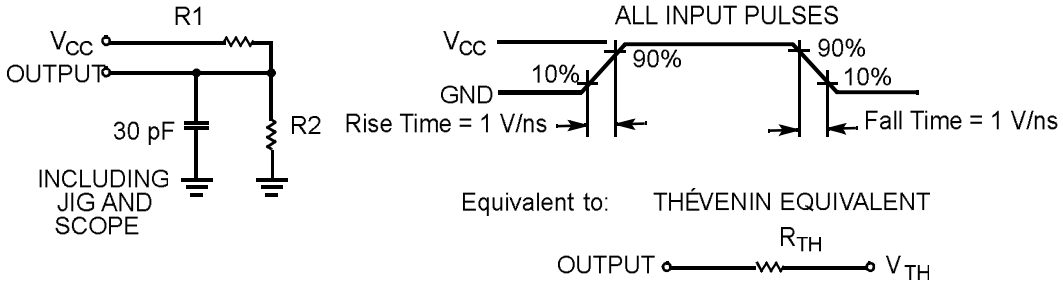
Parameter [10]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [10]	Description	Test Conditions	48-ball BGA	48-pin TSOP I	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	36.92	60.07	65.91	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.55	9.73	13.96	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
10. Tested initially and after any design or process changes that may affect these parameters.

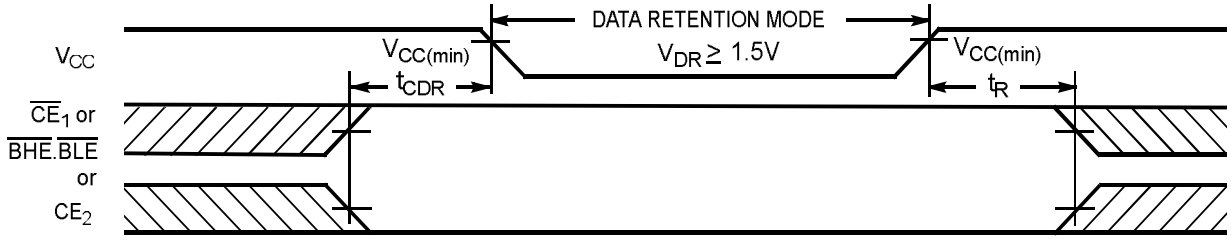
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR} [12]	Data retention current	V_{CC} = 1.5 V, $\overline{CE_1} \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, ($\overline{BHE}$ and $\overline{BLE}$) $\geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial / Automotive-A	–	3.2	8	µA
			Automotive-E	–	–	30	
t_{CDR} [13]	Chip deselect to data retention time			0	–		ns
t_R [14]	Operation recovery time		CY62157EV30LL-45	45	–	–	ns
			CY62157EV30LL-55	55	–	–	

Data Retention Waveform

Figure 5. Data Retention Waveform [15]



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
12. Chip enables ($\overline{CE_1}$ and CE_2), byte enables ($\overline{BHE}$ and $\overline{BLE}$) and $\overline{BYTE}$ (48-pin TSOP I only) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
15. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [16, 17]	Description	45 ns (Industrial/ Automotive-A)		55 ns (Automotive-E)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[18]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[18, 19]	–	18	–	20	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[18]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[18, 19]	–	18	–	20	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0	–	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down	–	45	–	55	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	45	–	55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[18, 20]	5	–	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High Z[18, 19]	–	18	–	20	ns
Write Cycle [21, 22]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	40	–	ns
t_{AW}	Address setup to write end	35	–	40	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[18, 19]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[18]	10	–	10	–	ns

Notes

16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 4 on page 5.
17. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
18. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
19. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
20. If both byte enables are toggled together, this value is 10 ns.
21. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
22. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 6. Read Cycle No. 1 (Address Transition Controlled) [23, 24]

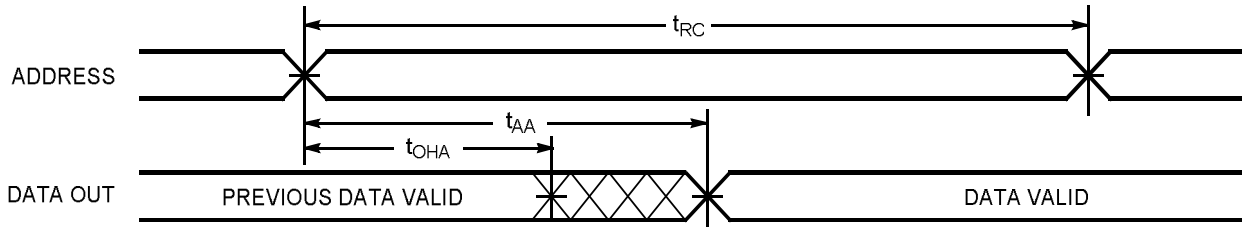
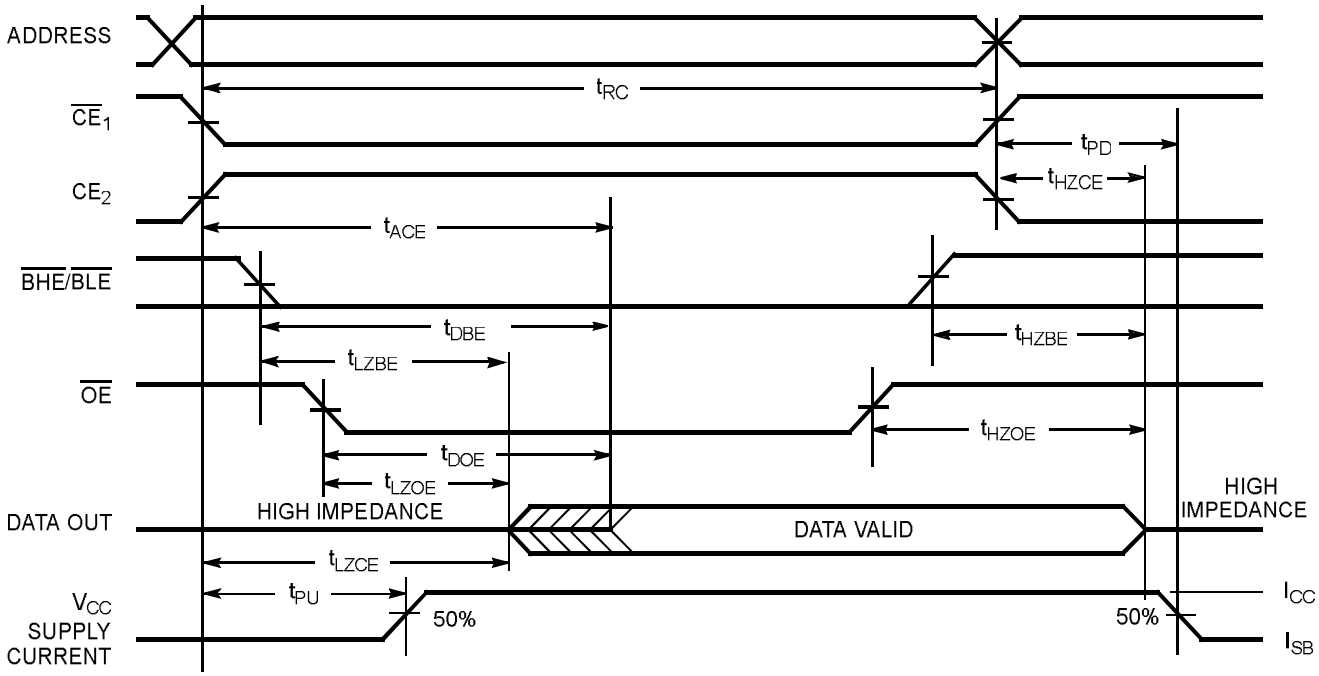


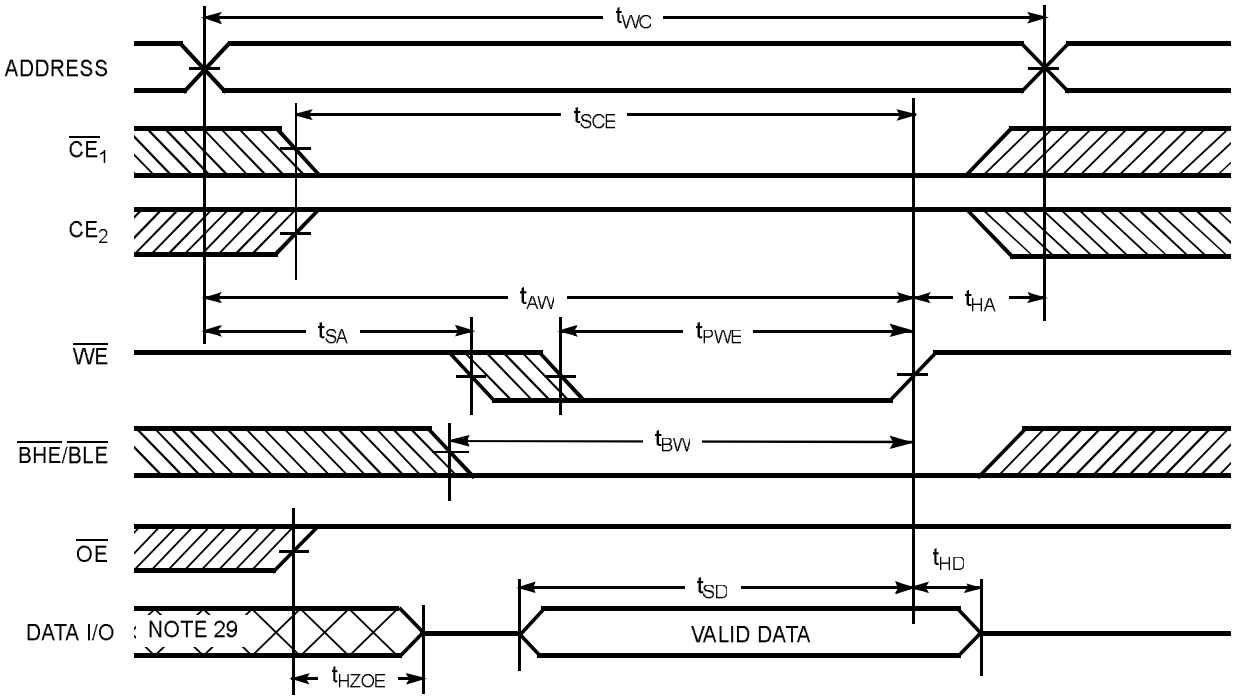
Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [24, 25]



Notes
23. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}, and CE_2 = V_{IH}.
24. $\overline{WE}$ is HIGH for read cycle.
25. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled) [26, 27, 28]

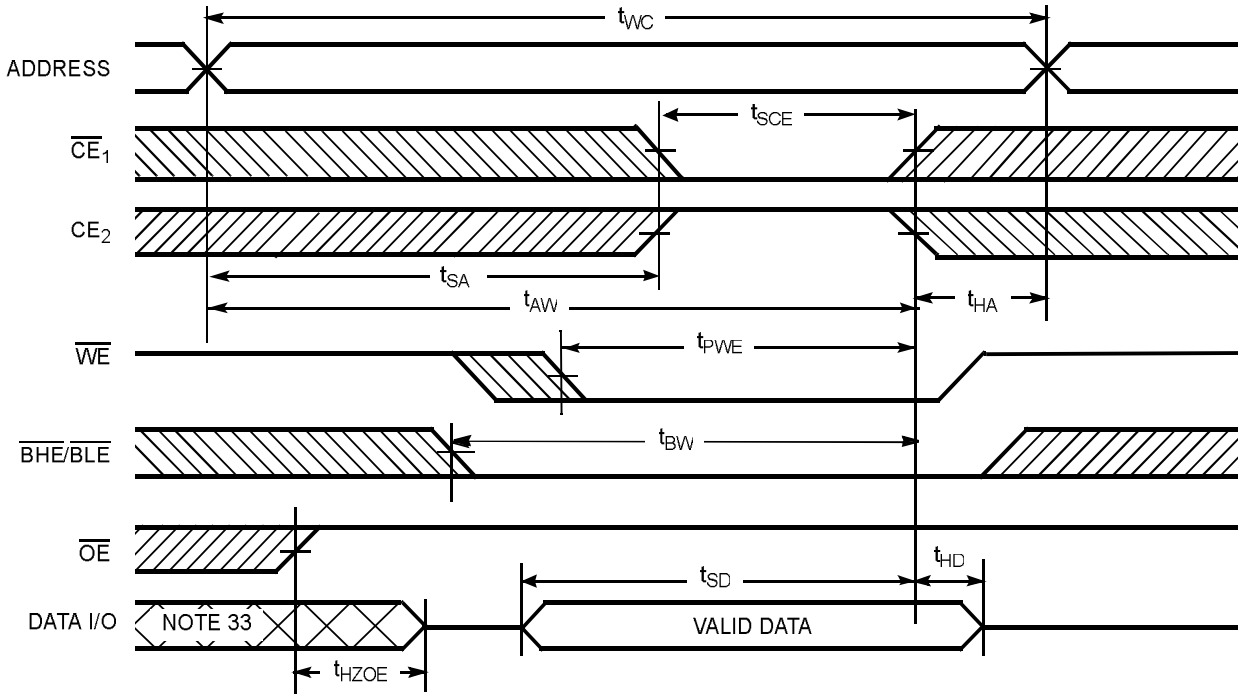


Notes

26. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
27. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
28. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
29. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [30, 31, 32]

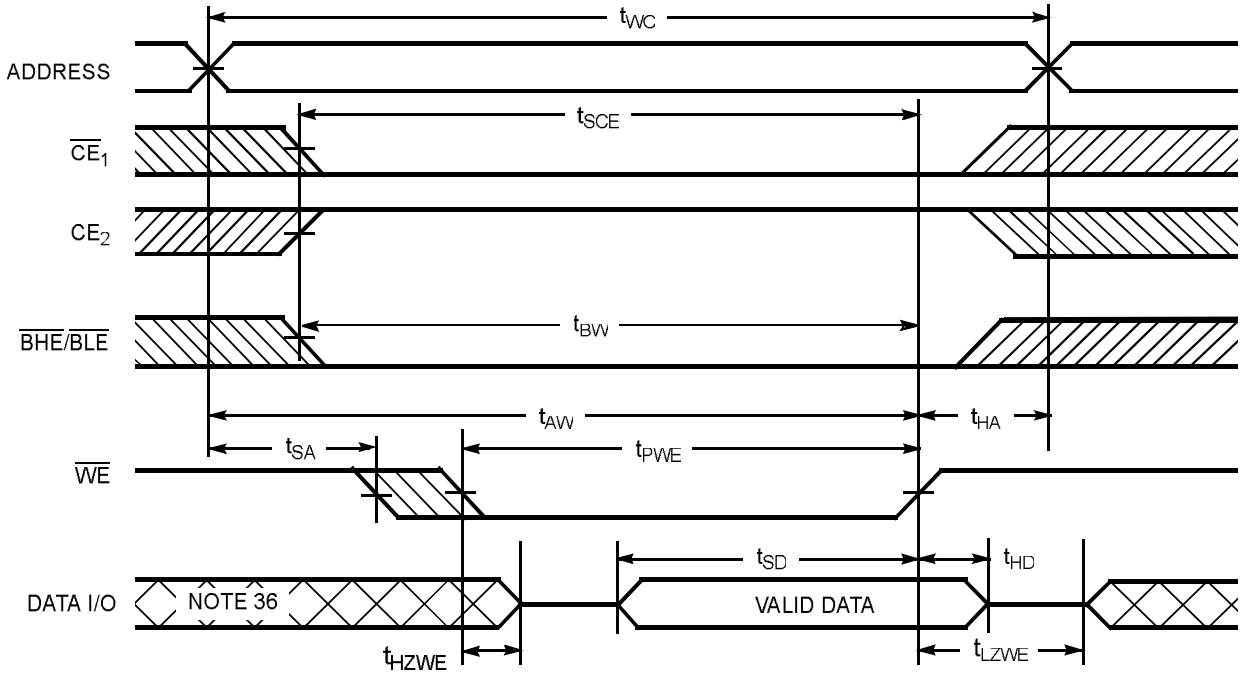


Notes

30. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
31. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
32. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
33. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

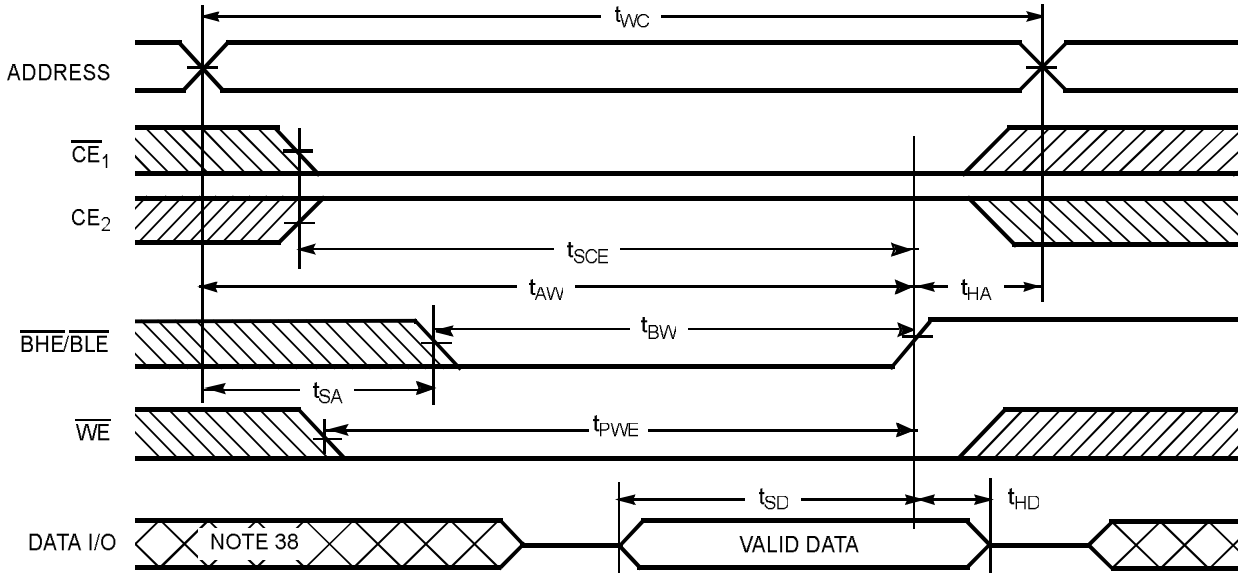
Figure 10. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [34, 35]



Notes
34. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
35. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
36. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 11. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [37]



Notes
37. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
38. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[39]	X	X	X	X	High Z	Deselect/power down	Standby (I_{SB})
X[39]	L	X	X	X	X	High Z	Deselect/power down	Standby (I_{SB})
X[39]	X[39]	X	X	H	H	High Z	Deselect/power down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data Out (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data In (I/O_0–I/O_7); High Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

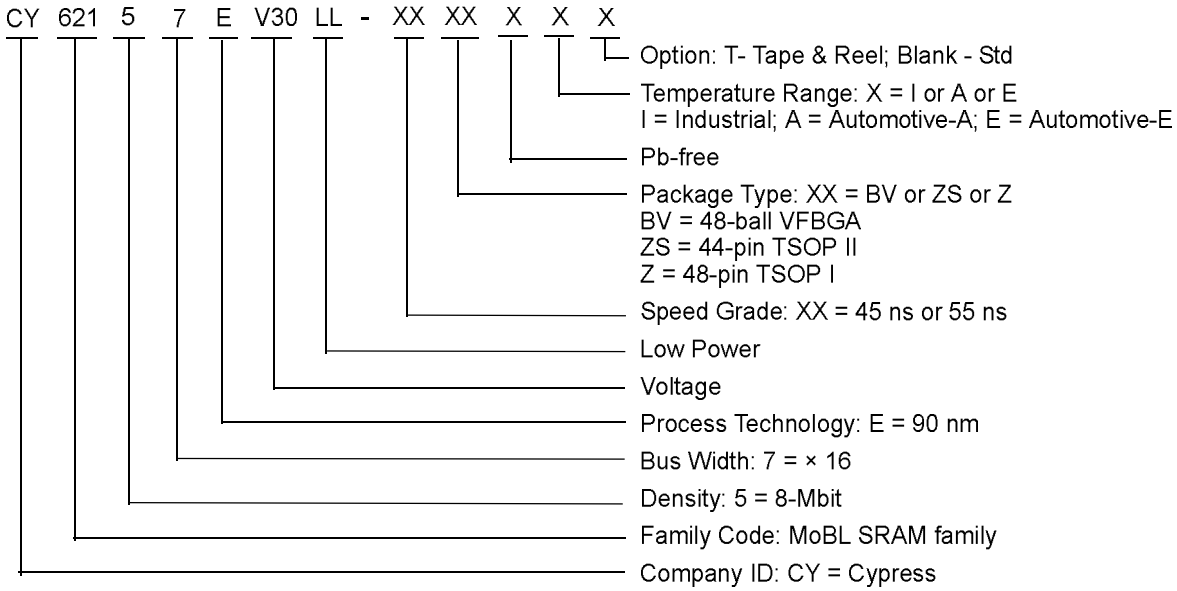
Note
39. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157EV30LL-45BVI	51-85150	48-ball VFBGA	Industrial
	CY62157EV30LL-45BVIT	51-85150	48-ball VFBGA	
	CY62157EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	
	CY62157EV30LL-45BVXIT	51-85150	48-ball VFBGA (Pb-free)	
	CY62157EV30LL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY62157EV30LL-45ZSXIT	51-85087	44-pin TSOP Type II (Pb-free)	
	CY62157EV30LL-45ZXI	51-85183	48-pin TSOP Type I (Pb-free)	
	CY62157EV30LL-45ZXIT	51-85183	48-pin TSOP Type I (Pb-free)	
	CY62157EV30LL-45BVXA	51-85150	48-ball VFBGA (Pb-free)	Automotive-A
	CY62157EV30LL-45BVXAT	51-85150	48-ball VFBGA (Pb-free)	
	CY62157EV30LL-45ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	
	CY62157EV30LL-45ZSXAT	51-85087	44-pin TSOP Type II (Pb-free)	
	CY62157EV30LL-45ZXA	51-85183	48-pin TSOP Type I (Pb-free)	
	CY62157EV30LL-45ZXAT	51-85183	48-pin TSOP Type I (Pb-free)	
55	CY62157EV30LL-55ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-E
	CY62157EV30LL-55ZSXET	51-85087	44-pin TSOP Type II (Pb-free)	
	CY62157EV30LL-55ZXE	51-85183	48-pin TSOP Type I (Pb-free)	
	CY62157EV30LL-55ZXET	51-85183	48-pin TSOP Type I (Pb-free)	

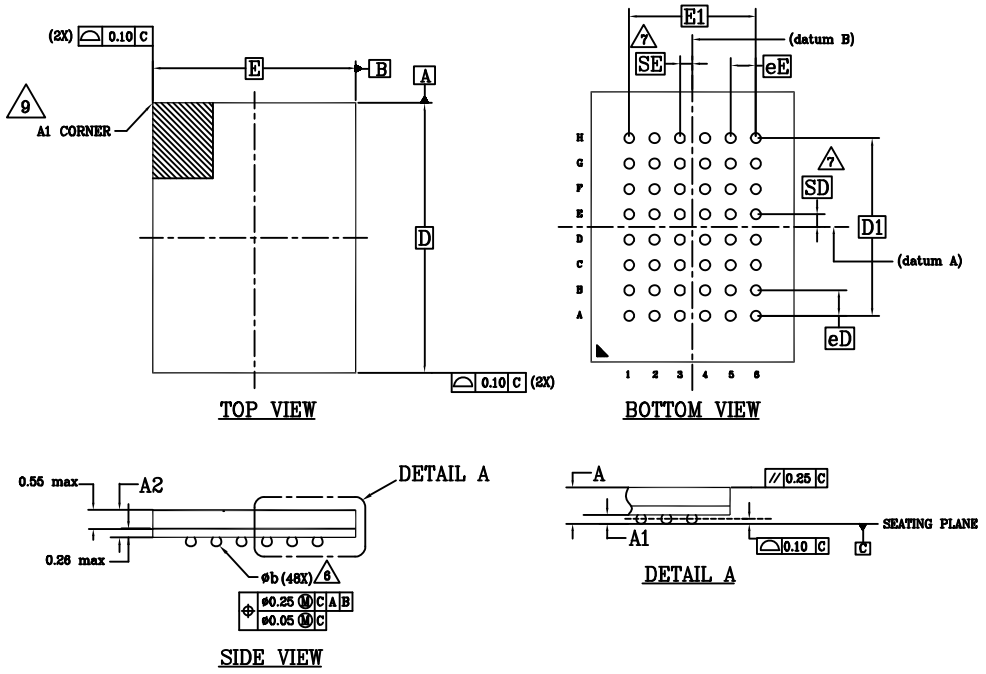
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 12. 48-pin VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

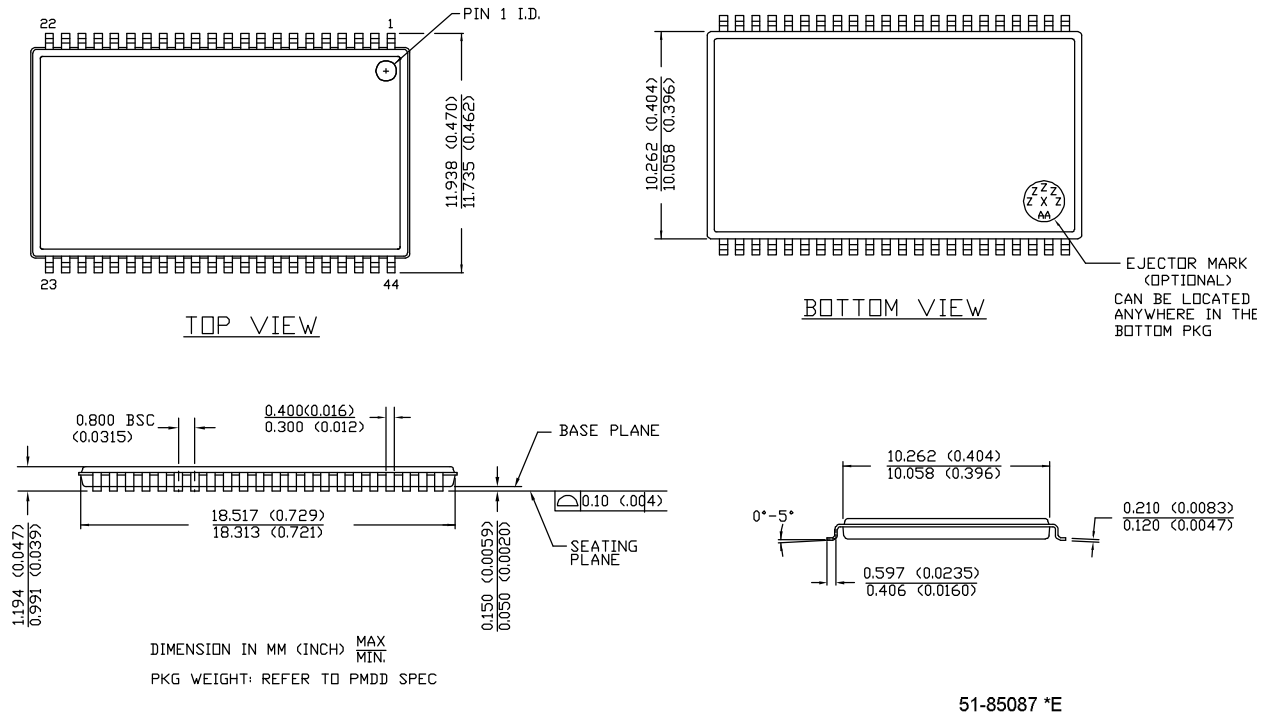
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALLIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

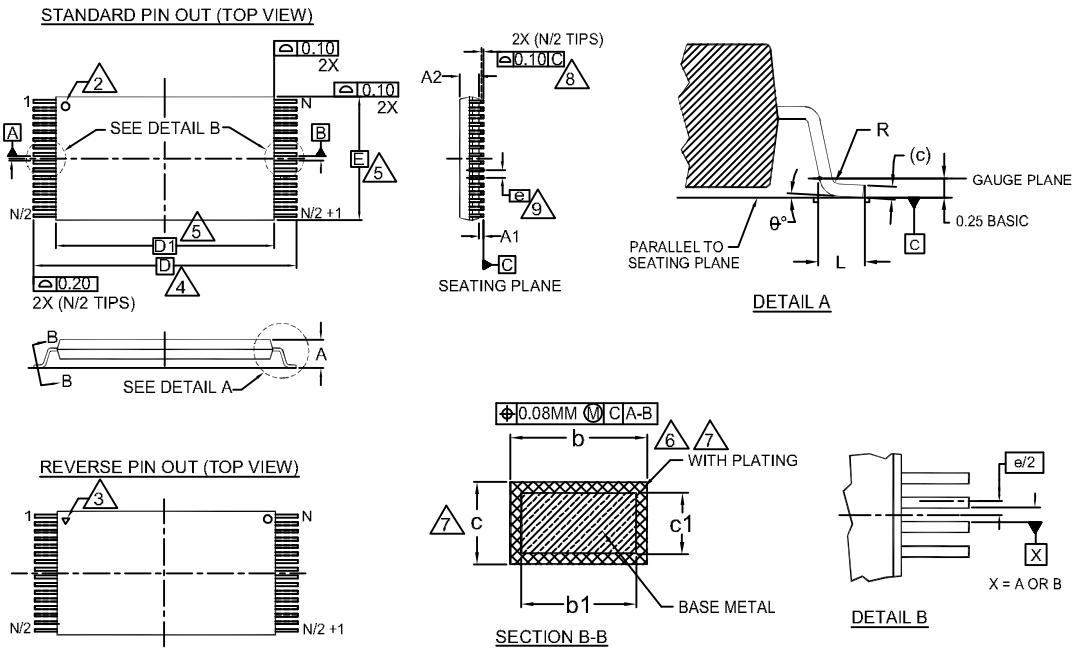
Package Diagrams (continued)

Figure 13. 44-pin TSOP II Package Outline, 51-85087



Package Diagrams (continued)

Figure 14. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62157EV30 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05445			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	202940	01/29/2004	New data sheet.
*A	291272	11/19/2004	Changed status from Advance Information to Preliminary. Removed 48-pin TSOP I Package related information in all instances across the document. Updated Pin Configurations: Added Note 2 and referred the same note in Figure 2. Updated Operating Range: Updated Note 7 (Replaced 100 µs with 200 µs). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 4 µA to 4.5 µA. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bins. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZCE} parameter from 15 ns to 22 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZBE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZBE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SCE} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin. Changed minimum value of t_{SCE} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{AW} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin. Changed minimum value of t_{AW} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{BW} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin. Changed minimum value of t_{BW} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed minimum value of t_{SD} parameter from 20 ns to 22 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZWE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZWE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin. Updated Ordering Information: Updated part numbers.

Document History Page (continued)

Document Title: CY62157EV30 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05445			
Revision	**ECN**	**Submission Date**	**Description of Change**
*B	444306	04/13/2006	Changed status from Preliminary to Final. Removed 35 ns speed bin related information in all instances across the document. Added 55 ns speed bin related information in all instances across the document. Added 48-pin TSOP I Package related information in all instances across the document. Added Automotive Temperature Range related information in all instances across the document. Updated Pin Configurations: Updated Figure 1 (Replaced DNU with NC in ball E3). Removed Note "DNU pins have to be left floating or tied to V_{SS} to ensure proper application." and its reference. Updated Product Portfolio: Removed "L" and "LL" from the part numbers. Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 16 mA to 18 mA corresponding to 45 ns speed bin and Test Condition "f = fax = $1/t_{RC}$". Changed maximum value of I_{CC} parameter from 28 mA to 25 mA corresponding to 45 ns speed bin and Test Condition "f = fax = $1/t_{RC}$". Changed maximum value of I_{CC} parameter from 2.3 mA to 3 mA corresponding to 45 ns speed bin and Test Condition "f = 1 MHz". Updated details in "Test Condition" column corresponding to I_{SB1} parameter. Changed typical value of I_{SB1} parameter from 0.9 µA to 2 µA corresponding to 45 ns speed bin. Changed maximum value of I_{SB1} parameter from 4.5 µA to 8 µA corresponding to 45 ns speed bin. Changed typical value of I_{SB2} parameter from 0.9 µA to 2 µA corresponding to 45 ns speed bin. Changed maximum value of I_{SB2} parameter from 4.5 µA to 8 µA corresponding to 45 ns speed bin. Updated Thermal Resistance: Replaced TBD with values in TSOP II column and updated all remaining values. Updated AC Test Loads and Waveforms: Updated Figure 4 (Replaced 50 pF with 30 pF). Updated Data Retention Characteristics: Added value in "Typ" column for I_{CCDR} parameter. Changed maximum value of I_{CCDR} parameter from 4.5 µA to 5 µA corresponding to Test Condition "Industrial". Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZBE} parameter from 6 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Added Note 20 and referred the same note in t_{LZBE} parameter.

Document History Page (continued)

Document Title: CY62157EV30 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05445			
Revision	**ECN**	**Submission Date**	**Description of Change**
*B (cont.)	444306	04/13/2006	Updated Ordering Information: Updated part numbers. Removed "Package Name" column. Added "Package Diagram" column.
*C	467052	06/06/2006	Added 1M × 8 configuration related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*D	925501	04/09/2007	Removed Automotive-E temperature range related information in all instances across the document. Added Preliminary Automotive-A related information in all instances across the document. Updated Electrical Characteristics: Added Note 9 and referred the same note in I_{SB2} parameter. Updated Switching Characteristics: Added Note 17 and referred the same note in "Parameter" column.
*E	1045801	05/08/2007	Changed Automotive-A temperature range related information from Preliminary to Final. Updated Electrical Characteristics: Updated Note 9.
*F	2724889	06/26/2009	Added Automotive-E temperature range related information in all instances across the document. Updated Ordering Information: Updated part numbers. Updated to new template.
*G	2927528	05/04/2010	Updated Pin Configurations: Updated Figure 3 (Renamed "DNU" pins as "NC"). Updated Truth Table: Added Note 39 and referred the same note in "X" in "$\overline{CE}_1$" and "CE_2" columns. Updated Package Diagrams: spec 51-85150 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *A to *C. spec 51-85183 – Changed revision from *A to *B. Updated to new template.
*H	3110053	12/14/2010	Changed Table Footnotes to Notes. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions.
*I	3269771	05/30/2011	Updated Functional Description: Updated description. Updated Electrical Characteristics: Updated details in "Conditions" column corresponding to I_{SB1} and I_{SB2} parameters. Updated Data Retention Characteristics: Updated details in "Conditions" and "Min" columns corresponding to I_{CCDR} and t_R parameters. Updated Package Diagrams: spec 51-85150 – Changed revision from *E to *F. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*J	3578601	04/11/2012	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *G. spec 51-85087 – Changed revision from *C to *D. spec 51-85183 – Changed revision from *B to *C. Completing Sunset Review.

Document History Page (continued)

Document Title: CY62157EV30 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05445			
Revision	**ECN**	**Submission Date**	**Description of Change**
*K	4102449	08/22/2013	Updated Switching Characteristics: Updated Note 17. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template.
*L	4126231	09/18/2013	Updated Switching Characteristics: Updated Note 17 (Removed last sentence from Note 17 and added the same sentence as a new note namely Note 18).
*M	4214977	12/09/2013	Updated Pin Configurations: Updated Note 3 (Removed 'NC' mentioned at the end of the note).
*N	4578508	11/24/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 22 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 35 and referred the same note in Figure 10.
*O	4748627	04/30/2015	Updated Package Diagrams: spec 51-85183 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*P	5320972	06/23/2016	Updated Thermal Resistance: Replaced "two-layer" with "four-layer" in "Test Conditions" column. Updated values of Θ_{JA}, Θ_{JC} parameters corresponding to all packages. Updated Ordering Information: Updated part numbers. Updated to new template.
*Q	5731504	05/10/2017	Updated Package Diagrams: spec 51-85183 – Changed revision from *D to *F. Updated to new template. Completing Sunset Review.
*R	6517814	03/21/2019	Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template.
*S		02/26/2020	Updated Features: Updated description. Updated Product Portfolio: Updated all values of "Operating I_{CC}" corresponding to "f = 1 MHz". Updated Electrical Characteristics: Updated all values of I_{CC} parameter corresponding to "45 ns (Industrial/Automotive-A)" and "f = 1 MHz". Updated Thermal Resistance: Updated all values of Θ_{JA}, Θ_{JC} parameters corresponding to all packages. Updated Data Retention Characteristics: Updated all values of I_{CCDR} parameter corresponding to Condition "Industrial/Automotive-A". Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
Product Qualification Report

QTP# 193601 VERSION**
February 2020

8-MBIT Ultra Low Power Asynchronous SRAM Family, ULP65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	
CY62157G*	**8-MBIT (512K WORDS X 16 BITS / 1M WORDS X 8 BITS) STATIC RAM WITH ERROR-CORRECTING CODE (ECC), W/ AND W/O ERR PIN (AMAZON EQUIVALENT)**
CY62158G*	**8-MBIT (1M WORDS X 8 BITS) STATIC RAM WITH ERROR-CORRECTING CODE (ECC), W/ AND W/O ERR PIN (AMAZON EQUIVALENT)**
CY62157EV*	**INDUSTRIAL MoBL® 8-MBIT (512K WORDS X 16 BITS / 1M WORDS X 8 BITS) STATIC RAM (R95 EQUIVALENT)**
CY62158EV**	**INDUSTRIAL MoBL® 16-MBIT (1M WORDS X 8 BITS) STATIC RAM (R95 EQUIVALENT)**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com

Prepared By:
Josephine Pineda (JYF)
Reliability Engineer

Reviewed By:
Sandhya Chandrashekhar (SANC)
Reliability Manager

Approved By:
David Hoffman (DHH)
Reliability Director

QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	Aug. 2009
124902	Qualification of 16-MBIT Asynchronous SRAM Family, ULL65nm (LL65UP-25ODR) Technology at UMC Fab 12A	Aug. 2014
144804	Qualification of 16-MBIT Asynchronous SRAM Family Rev.*D Silicon, ULL65nm (LL65UP-25ODR) Technology at UMC Fab 12A	Feb. 2015
181403	Qualification of 16-MBIT Ultra Low Power Asynchronous SRAM Family - Rev.A0 Silicon, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	June 2019
190713	Qualification of 16-MBIT Ultra Low Power Asynchronous SRAM Family - Rev. A1 Silicon, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	April 2019
191808	Qualification of 16-MBIT Ultra Low Power Asynchronous SRAM Family - Rev. A2 Silicon, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	Oct. 2019
193601	Qualification of 8-MBIT Ultra Low Power Asynchronous SRAM Family - Rev. A0 Silicon, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	Feb. 2020

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify 8-MBIT Ultra Low Power Asynchronous SRAM Family, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A
Marketing Part #:	CY62157G* / CY62158G* / CY62157EV* / CY62158EV*
Device Description:	8-MBIT Ultra Low Power Asynchronous SRAM Family
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65UMP-25ODR			
Number of Metal Layers:	Proprietary	Metal Composition:	Proprietary
Passivation Type and Materials:		Proprietary	
Number of Transistors in Device		Proprietary	
Number of Logic Gates in Device		Proprietary	
Generic Process Technology/Design Rule (µ-drawn):		Proprietary	
Gate Oxide Material/Thickness (MOS):		Proprietary	
Name/Location of Die Fab (prime) Facility:		UMC Fab 12A	
Die Fab Line ID/Wafer Process ID:		L65LL	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY	QTP REFERENCE
48-Ball VFBGA	Bangkok-Taiwan (SB)	QTP# 194606
48L TSOP I	Bangkok-Taiwan (SB)	QTP# 194523
44L TSOP II	CML-RA	QTP# 194601

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BZ48A
Package Outline, Type, or Name:	VFBGA (Very Fine Ball Grid Array)
Mold Compound Name/Manufacturer:	KMC-3580/SHINETSU
Mold Compound Flammability Rating:	V-0 / UL94
Substrate Material:	Substrate Cu/BT
Lead Finish, Composition / Thickness:	Sn/Ag/Cu (SAC-305)
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI 546
Bond Diagram Designation:	002-28274
Wire Bond Method:	Thermosonic
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-97055
Name/Location of Assembly (prime) facility:	BKK-Thailand (SB)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R, Chipmos-Taiwan (GO), Bangkok-Thailand (SB)

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Constructional Analysis	Criteria: Meet external and internal characteristics of Cypress package	P
Dynamic Latch-up	125°C , 8.25V JESD78	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V/750V/1,000V/1,250V/1,500V/1,750V/2,000V JESD22-C101	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V/2,200V/3,300V/4,000V/5,000V/6,000V JESD22-A114	P
Electrostatic Discharge Machine Model (ESD-MM)	200V JESD22-A115	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V 110°C/130°C, 85%RH, 3.65V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
High Accelerated Saturation Test (HAST) - Unbiased	JEDEC STD 22-A110: 130°C, 85%RH Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 1.37/2.25V, 150°C JESD22-A108	P
High Temperature Storage	JESD22-A103:150°C No bias	P
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 1.44V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 1.44V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core, 1.45V,External 2.05V,125°C /150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 1.62V/2.25V, -30°C JESD22-A108	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at 0 hour/500/1000hrs	P
Static Latch-up	125°C , ±/100mA/140mA, 85°C , ±140mA/200mA/300mA JESD78	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C/ 85% RH , 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron)	JESD89	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life[1] Early Failure Rate	1, 542 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[2] Long Term Failure Rate (150°C)	89,000 DHRs	0	0.7	170	11 FIT
High Temperature Operating Life[2] Long Term Failure Rate (125°C)	1,247,840 DHRs	0	0.7	55	

[1]Early Failure Rate was computed from QTP# 193601.

[2] Long Term Failure Rate was computed from QTP# 091706, QTP# 124902, QTP# 181403, QTP# 191808 and QTP# 193601 Data.

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2}-\frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #:091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

Reliability Test Data

QTP #:091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

Reliability Test Data

QTP #:091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEMP, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

Reliability Test Data

QTP #:124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	15	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	170	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	3	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	3	0	
STRESS: CONSTRUCTIONAL ANALYSIS							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	5	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	5	0	
STRESS: DYNAMIC LATCH-UP TESTING, 125C, 8.25V							
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	500	9	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1000	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1250	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	500	9	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1250	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	500	9	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1000	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1250	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	500	9	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1000	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1250	3	0	

Reliability Test Data

QTP #:124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	500	9	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	750	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	500	9	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1000	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1100	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	2200	8	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	3300	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1100	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	2200	8	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	3300	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1100	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	2200	8	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	3300	3	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	1100	3	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	2200	8	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	3300	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1100	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	2200	8	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	3300	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1100	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	2200	8	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	3300	3	0	
STRESS: HI-ACCEL SATURATION TEST, 110C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	264	30	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	128	79	0	

Reliability Test Data

QTP #:124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE – REG-ON, 125C, 6.0V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	96	50	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	96	50	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	96	2107	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	96	1818	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	168	179	0	
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	1000	175	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	168	180	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	1000	180	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	168	179	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	178	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 1.37V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	168	80	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	168	80	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	500	79	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	1000	79	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 1.62V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	500	83	0	
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	1000	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	1000	10+2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	0	10+2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	10+2	0	

Reliability Test Data

QTP #:124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRE/POST LTOL CRITICAL PARAMETERS							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	500	10+2	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	168	79	0	
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	288	79	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	168	78	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	288	78	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V/9.1V, +/-140mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	6	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	6	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	6	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	6	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	6	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	6	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V/9.1V, +/-140mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	2	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	2	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V/9.1V, +/-180mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	2	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	2	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	2	0	

Reliability Test Data

QTP #:124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE SEL, 25C/85C/120C, 1.65V/3.3V/5.5V							
7C1710614GE	0	0	UMC	COMP	3	0	
STRESS: SER – NEUTRON SEL, 85C/125C, 5.25V							
7C17165A	0	0	UMC	COMP	3	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	1000	79	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	1000	78	0	
CY7C1061G30 (7CP1710612A)	9313001	611420263	CML-RA	500	80	0	
CY7C1061G30 (7CP1710612A)	9313001	611420263	CML-RA	1000	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	1000	80	0	
STRESS: X-SECTION/STEM XY AUDIT							
7C17165A	9302002	0	UMC	COMP	1WF	0	

Reliability Test Data

QTP #:144804

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	500	9	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1000	3	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1100	3	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	2200	8	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	3300	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	96	927	0	
CY62167G30 (7CC172167A)	9438001	611503292	G-Taiwan	96	695	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V, +/-140mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-200mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V, +/-140mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
YIELD: CLASS							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		
YIELD: E-TEST							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		
YIELD: SORT							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		

Reliability Test Data

QTP #:181403

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1061G (7CP171061AO)	9537003	611624393	SB-Thailand	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	96	1636	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1000	120	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157EV30LL (7CP62157FC)	4501549	RFB2171	SB-Thailand	168	80	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1061G (7CP171061AO)	9537003	611624393	SB-Thailand	500	80	0	
CY7C1061G (7CP171061AO)	9537003	611624393	SB-Thailand	1000	80	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	500	9	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1000	3	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1100	3	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	2200	8	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	3300	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, +/-100mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.94V, +/-140mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-140mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-200mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	2	0	

Reliability Test Data

QTP #:190713

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	96	2318	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	500	9	0	
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	1000	3	0	
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	1100	3	0	
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	2200	8	0	
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	3300	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, +/-100mA							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.94V, +/-140mA							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-140mA							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-200mA							
CY62167G30 (7CP182167AO)	9851013	611910418	SB-Thailand	COMP	2	0	

Reliability Test Data

QTP #:191808

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	96	1762	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	500	120	0	
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	1000	118	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	500	9	0	
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	1000	3	0	
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	1100	3	0	
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	2200	8	0	
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	3300	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, +/-100mA							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.94V, +/-140mA							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-140mA							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-200mA							
CY62167EV30LL9 (7CP182167ABO)	9907044	611920146	SB-Thailand	COMP	2	0	

Reliability Test Data

QTP #:193601

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	COMP	22	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	500	9	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	750	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1000	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1250	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1500	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1750	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	2000	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1100	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	2200	8	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	3300	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	4000	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	5000	3	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	6000	3	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	96	30	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	128	30	0	
STRESS: HI-ACCEL SATURATION TEST- UNBIASED (130C, 85%RH), PRE COND 192 HR 30C/60%RH (MSL3)							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	96	80	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	192	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	96	1542	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	500	120	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1000	118	0	

Reliability Test Data

QTP #:193601

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	0	32	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	500	32	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1000	32	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, +/-100mA							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.94V, +/-140mA							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-140mA							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-200mA							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-300mA							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	COMP	3	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	500	80	0	
CY62157G30 (7CP182157ABO)	9938005	611936984	SB-Thailand	1000	80	0	

Document History Page

Document Title: QTP# 193601: 8-MBIT ULTRA LOW POWER ASYNCHRONOUS SRAM FAMILY, ULP65NM (LL65UMP-25ODR) TECHNOLOGY AT UMC FAB 12A
Document Number: 002-29675

Rev.	ECN No.	Orig. of Change	Description of Change
**	6789817	JYF	Initial spec release.

Cypress Semiconductor Corporation
CY62157EVXX Characterization Report

8 Mbit Static RAM

Design Engineering Director or Manager
Prashant Saxena
psc@cypress.com

Product Engineering Director
Shailesh Chauhan
svc@cypress.com

Product Engineer
Mark Lindsey Magboo
qoo@cypress.com

Applications Engineer
Vinay Manikkoth
vini@cypress.com

Marketing Engineer
Karthik Rangarajan
karr@cypress.com

www.cypress.com

198 Champion Ct.
San Jose, CA 95134 USA

Tel: (408) 943 2600
Fax: (408) 943 4730

1.0 Table of Contents

2.0 Introduction

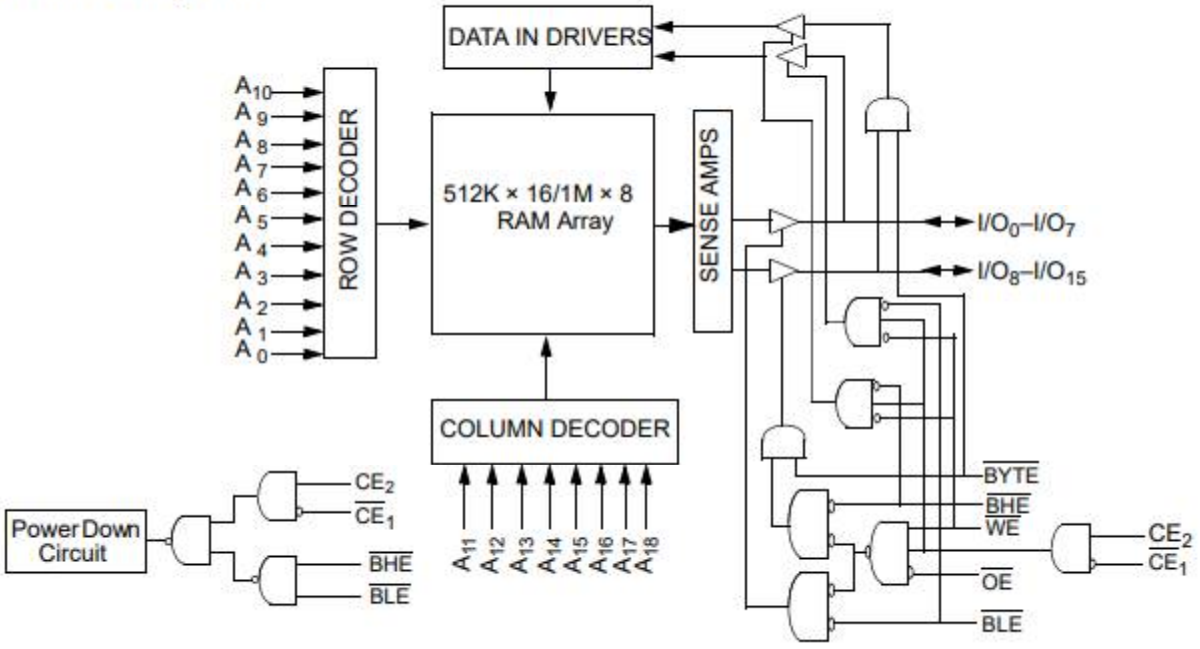
2.1 General Description

The CY62157EV30 is a high-performance CMOS static RAM. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected (CE1 HIGH or CE2 LOW or both BHE and BLE are HIGH). The input or output pins (I/O0 through I/O15) are placed in a high impedance state when the device is deselected (CE1 HIGH or CE2 LOW), the outputs are disabled (OE HIGH), Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is active (CE1 LOW, CE2 HIGH and WE LOW).

To write to the device, take Chip Enable (CE1 LOW and CE2 HIGH) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O0 through I/O7) is written into the location specified on the address pins (A0 through A18). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O8 through I/O15) is written into the location specified on the address pins (A0 through A18).

To read from the device, take Chip Enable (CE1 LOW and CE2 HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appear on I/O0 to I/O7. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O8 to I/O15.

Logic Block Diagram



Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View)

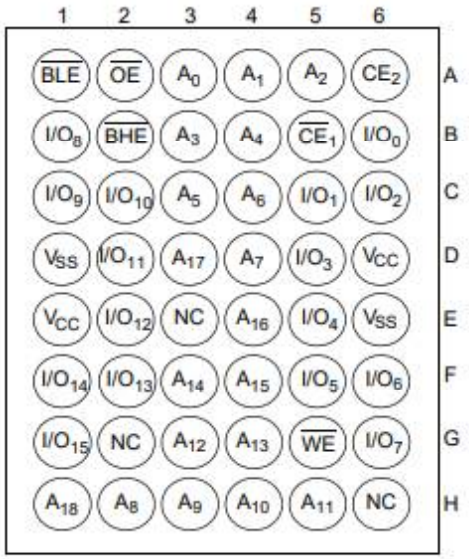


Figure 2. 44-pin TSOP II pinout (Top View)

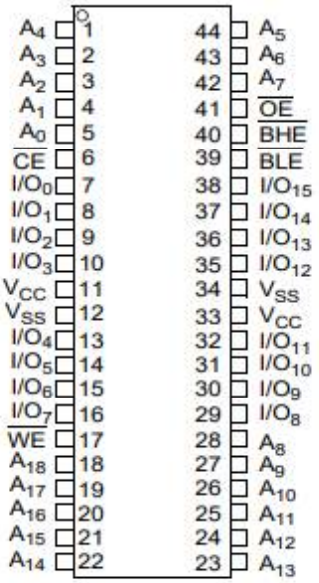
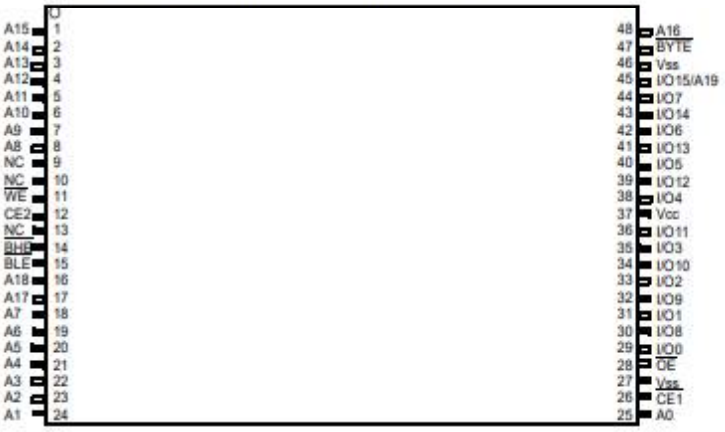


Figure 3. 48-pin TSOP I pinout (Top View)



2.2 Datasheet

The *CY62157EVXX* meets all datasheet specifications. The datasheet is available from the Cypress Website at:

CY62157EV30 Datasheet
CY62157EV18 Datasheet

2.3 Application Notes

The *CY62157EVXX* has the following associated Application Notes at this time. The Application Notes are available from the Cypress website at the URL provided below.

AN44517 - Design Recommendation for Battery-Backed SRAMs Using Cypress MoBL® SRAMs

2.4 White Papers

The *CY62157EVXX* has no associated White Papers at this time.

2.5 Qualification Report

The *CY62157EVXX* is qualified under QTP 193601.

3.0 Characterization Hardware and Setup

3.1 Measurement System and Hardware

The following equipments and hard wares are used for the DC and AC parametric characterization of this device.

3.1.1 Characterization Board

All the DC parameters and the AC parameters were measured using 48TSOP1 package with the D1054 hand test interface board and 48VFBGA package with D84348 board connected to L042 load board. Pin capacitance was measured using the probe card type board.

3.1.2 ATE

Advantest 5581P tester was used for the DC and AC parameter characterization.

3.1.3 Temperature Forcing System

Temptronics TP04310A Precision Temperature Forcing System was used to force ambient temperature.

3.1.4 Frequency LCR Meter

HP4284A LCR Meter was used to measure input and output pin capacitance.

3.1.5 Power Supply

The Kiethley 2400 Source Meter was used to supply power for device for pin capacitance measurement.

3.2 Characterization Conditions and Parameters

Characterization was done on the following device and conditions as listed in Table 1. Units used for characterization are quick builds and chosen randomly unless specified.

Table 1. Characterization Conditions and Parameters

Parameter	Device	Fab Lot	Assy Lot	# of Devices	Voltage Variation (V)	Temperature Variation (ºC)
DC & AC	CY62157EV30-45BVXI	9938005	611936984	64	1.65V-3.7V	-40, 25, 85

The part is qualified for a new technology and fabrication site. The below tables compare the characterization results for the current technology and the new technology.

4.0 DC Characterization

4.1 DC Characterization Summary over V_{DD} and Temperature

Table 2. 3V DC Characterization Results across V_{DD} and Temperature

Parameter	Description		Test Conditions		Datasheet (45ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
					Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V_{OH}	Output HIGH voltage	2.2V to 2.7V	VCC = Min, IOH = –0.1 mA		2.0	-	-	2.16	2.17	2.18	2.15	2.15	2.16	V
		2.7V to 3.6V	VCC = Min, IOH = –1.0 mA		2.4	-	-	2.60	2.61	2.61	2.58	2.58	2.59	
V_{OL}	Output LOW voltage	2.2V to 2.7V	VCC = Min, IOL = 0.1 mA		-	-	0.4	0.028	0.029	0.03	0.038	0.040	0.044	V
		2.7V to 3.6V	VCC = Min, IOL = 2.1 mA		-	-	0.4	0.170	0.175	0.180	0.146	0.149	0.154	
V_{IH}	Input HIGH voltage	2.2V to 2.7V			1.8	-	VCC + 0.3	1.19	1.21	1.25	1.21	1.22	1.24	V
		2.7V to 3.6V			2.0	-	VCC + 0.3	1.47	1.50	1.56	1.69	1.70	1.71	
V_{IL}	Input LOW voltage	2.2V to 2.7V			-0.3	-	0.6	0.87	0.88	0.90	0.96	0.97	0.97	V
		2.7V to 3.6V			-0.3	-	0.8	0.96	0.98	1.00	1.15	1.16	1.17	
I_{IX}	Input leakage current		GND < VIN < VCC		-1.0	-	1.0	-0.020	0.072	0.100	-0.040	0.020	0.140	uA
I_{OZ}	Output leakage current		GND < VOUT < VCC, Output disabled		-1.0	-	1.0	-0.020	0.028	0.040	-0.040	0.024	0.040	uA
I_{CC}	Operating supply current		VCC = Max, IOUT = 0 mA, CMOS levels	f = 1 MHz	-	6	7	1.8	1.99	2.08	3.36	3.64	4.00	mA
				f = 22.22 MHz (55ns)	-	18	25	19.12	20.56	21.52	18.80	19.65	20.80	
I_{sb1}	Automatic Power-down Current – CMOS Inputs; VCC = 2.2 V to 3.6 V		CE1 > VCC – 0.2 V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V, VIN < 0.2 V, f = fmax (address and data only), f = 0 (OE, and WE), VCC = VCC(max)		-	2	8	1.88	3.17	4.26	2.94	3.76	4.64	uA
I_{sb2}	Current – CMOS Inputs VCC = 2.2 V to 3.6 V		CE1 > VCC – 0.2V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V or VIN < 0.2 V, f = 0, VCC = VCC(max)		-	2	8	2.48	3.19	4.32	4.54	4.80	5.16	uA

Table 3. 1.8V DC Characterization Results across V_{DD} and Temperature

Parameter	Description	Test Conditions		Datasheet (55ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
				Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V_{OH}	Output HIGH voltage	Vcc = 1.65V, IOH = –0.1 mA		1.4	-	-	1.61	1.62	1.63	1.59	1.60	1.60	V
V_{OL}	Output LOW voltage	VCC = 1.65V, IOL = 0.1 mA		-	-	0.2	0.024	0.027	0.030	0.040	0.043	0.048	V
V_{IH}	Input HIGH voltage	Vcc = 1.65V to 2.25V		1.4	-	VCC + 0.2	1.06	1.08	1.10	1.24	1.25	1.26	V
V_{IL}	Input LOW voltage	Vcc = 1.65V to 2.25V		-0.2	-	0.4	0.78	0.81	0.83	0.75	0.76	0.76	V
I_{IX}	Input leakage current	GND < VIN < VCC		-1.0	-	1.0	-0.020	0.072	0.100	-0.040	0.020	0.140	uA
I_{OZ}	Output leakage current	GND < VOUT < VCC, Output disabled		-1.0	-	1.0	-0.020	0.028	0.040	-0.040	0.024	0.040	uA
I_{CC}	Operating supply current	VCC = Max, IOUT = 0 mA, CMOS levels	f = 1 MHz	-	6	7	1.61	1.84	2.57	3.08	3.37	3.80	mA
			$f = f_{max}$	-	18	25	18.50	20.18	21.22	14.80	15.88	16.80	
I_{sb1}	Automatic CE power down current – CMOS inputs	CE1 > VCC – 0.2 V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V, VIN < 0.2 V, f = fmax (address and data only), f = 0 (OE, and WE), VCC = VCC(max)		-	2	8	1.80	3.00	3.82	4.06	4.76	5.62	uA
I_{sb2}	Automatic CE power down current – CMOS inputs	CE1 > VCC – 0.2V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V or VIN < 0.2 V, f = 0, VCC = VCC(max)		-	2	8	2.64	3.24	4.00	6.46	6.72	7.06	uA

Capacitance

Parameter	Description	Test Conditions	Datasheet	90nm Skywater fab (current)	65nm UMC fab (New)	Unit
C_{IN}	Input capacitance	TA = 25 °C, f = 1 MHz, VCC = VCC(typ)	10	7.80	7.80	pF
C_{OUT}	Output capacitance		10	6.80	6.80	pF

Data Retention Characteristics

Parameter	Description	Test Conditions	Datasheet (45ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
			Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V_{DR}	VCC for data retention		1.5	-	-	Pass	-	-	Pass	-	-	V
I_{CCDR}	Data retention current	VCC = 1.5 V, CE1 > VCC – 0.2 V or CE2 < 0.2 V, or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V or VIN < 0.2 V	-	3.2	8	1.62	2.59	3.10	4.06	4.51	4.80	uA
t_{CDR}	Chip deselect to data retention time		0	-	-	Pass	-	-	Pass	-	-	V
t_R	Operation recovery time	VCC > 2.2 V	45	-	-	pass	-	-	Pass	-	-	ns

Parameter	Description	Test Conditions	Datasheet (55ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
			Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V_{DR}	VCC for data retention		1.0	-	-	Pass	-	-	Pass	-	-	V
I_{CCDR}	Data retention current	VCC = 1.2 V, CE1 > VCC – 0.2 V or CE2 < 0.2 V, or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V or VIN < 0.2 V	-	5	9	0.40	1.89	2.66	6.32	6.69	7.08	uA
t_{CDR}	Chip deselect to data retention time		0	-	-	Pass	-	-	Pass	-	-	V
t_R	Operation recovery time	VCC > 2.2 V	55	-	-	pass	-	-	Pass	-	-	ns

5.0 AC Characterization

5.1 AC Characterization Summary over V_{DD} and Temperature

Table 4. AC Characterization Results across V_{DD} (2.2V-3.6V) and Temperature

Parameter	Description	Datasheet (45ns)		90nm Skywater fab (current)			65nm UMC fab (New)			
		Min	Max	Min	Mean	Max	Min	Mean	Max	Unit
Read Cycle										
t_{RC}	Read cycle time	45.0	-	Pass	-	-	Pass	-	-	ns
t_{AA}	Address to data valid	-	45.0	28.00	30.16	33.87	15.68	16.29	17.05	ns
t_{OHA}	Data hold from address change	10.0		14.37	15.44	17.19	15.45	15.74	15.94	ns
t_{ACE}	CEB LOW to data valid	-	45.0	30.00	32.28	36.25	28.98	30.34	31.55	ns
t_{DOE}	OEB LOW to data valid	-	22.0	11.44	12.03	12.87	7.30	7.43	7.57	ns
t_{LZOE}	OEB LOW to low-Z	5	-	7.65	7.74	7.75	7.65	7.74	7.75	ns
t_{HZOE}	OEB HIGH to high-Z	-	18.0	5.65	5.80	5.87	5.73	5.87	5.93	ns
t_{LZCE}	CEB LOW to low-Z	10.0	-	27.80	27.83	27.90	27.75	27.82	27.90	ns
t_{HZCE}	CEB LOW to low-Z	-	18.0	6.05	6.10	6.15	6.03	6.15	6.28	ns
t_{PU}	CEB LOW to power-up	0	-	pass	-	-	pass	-	-	ns
t_{pd}	CEB HIGH to power-down	-	45.0	-	-	pass	-	-	pass	ns
t_{DBE}	Byte enable to data valid	-	45.0	30.75	34.02	38.19	29.61	31.02	32.18	ns
t_{LZBE}	Byte enable to low-Z	5	-	28.13	28.20	28.28	27.18	28.09	28.23	ns
t_{HZBE}	Byte disable to high-Z	-	18.0	6.03	6.08	6.15	6.03	6.10	6.18	ns

Parameter	Description	Datasheet (45ns)		90nm Skywater fab (current)			65nm UMC fab (New)			
		Min	Max	Min	Mean	Max	Min	Mean	Max	Unit
Write Cycle										
t_{WC}	Write cycle time	45.0	-	pass	-	-	pass	-	-	ns
t_{SCE}	CE LOW to write end	-	35.0	16.25	17.50	20.19	23.41	24.76	25.98	ns
t_{AW}	Address setup to write end	-	35.0	17.37	19.38	21.62	25.43	26.92	28.22	ns
t_{HA}	Address hold from write end	0	-	-6.44	-6.21	-5.88	-11.32	-10.61	-10.17	ns
t_{SA}	Address setup to write start	0	-	-9.56	-7.75	-8.34	-6.89	-6.67	-6.45	ns
t_{PWE}	WE pulse width	-	35.0	13.75	14.90	17.25	5.85	6.13	6.45	ns
t_{BW}	Byte Enable to write end	-	35.0	17.75	19.16	21.81	25.48	26.90	28.11	ns
t_{SD}	Data setup to write end	-	25.0	10.81	11.56	12.87	6.18	6.43	6.73	ns
t_{HD}	Data hold from write end	0	-	-7.25	-6.64	-6.13	-2.57	-2.38	-2.13	ns
t_{HZWE}	WE LOW to high-Z	-	18.0	6.21	6.22	6.23	6.20	6.22	6.24	ns
t_{LZWE}	WE HIGH to low-Z	10.0	-	15.70	15.78	15.85	15.85	15.89	15.93	ns

Table 5. AC Characterization Results across V_{DD} (1.65V-2.2V) and Temperature

Parameter	Description	Datasheet (55ns)		90nm Skywater fab (current)			65nm UMC fab (New)			
		Min	Max	Min	Mean	Max	Min	Mean	Max	Unit
Read Cycle										
t_{RC}	Read cycle time	55.0	-	Pass	-	-	Pass	-	-	ns
t_{AA}	Address to data valid	-	55.0	33.31	33.70	35.56	16.25	16.81	17.45	ns
t_{OHA}	Data hold from address change	10.0		14.37	15.44	17.19	15.45	15.67	16.00	ns
t_{ACE}	CEB LOW to data valid	-	55.0	36.12	36.89	38.69	31.16	32.51	33.73	ns
t_{DOE}	OEB LOW to data valid	-	25.0	11.31	12.13	13.50	8.45	8.55	8.72	ns
t_{LZOE}	OEB LOW to low-Z	5	-	7.65	7.74	7.75	7.65	7.74	7.75	ns
t_{HZOE}	OEB HIGH to high-Z	-	18.0	5.65	5.80	5.87	5.73	5.87	5.93	ns
t_{LZCE}	CEB LOW to low-Z	10.0	-	27.80	27.83	27.90	27.75	27.82	27.90	ns
t_{HZCE}	CEB LOW to low-Z	-	18.0	6.05	6.10	6.15	6.03	6.15	6.28	ns
t_{PU}	CEB LOW to power-up	0	-	pass	-	-	pass	-	-	ns
t_{pd}	CEB HIGH to power-down	-	55.0	-	-	pass	-	-	pass	ns
t_{DBE}	Byte enable to data valid	-	55.0	36.56	37.73	40.69	32.07	33.49	34.80	ns
t_{LZBE}	Byte enable to low-Z	5.0	-	28.13	28.20	28.28	27.18	28.09	28.23	ns
t_{HZBE}	Byte disable to high-Z	-	18.0	6.03	6.08	6.15	6.03	6.10	6.18	ns

Parameter	Description	Datasheet (55ns)		90nm Skywater fab (current)			65nm UMC fab (New)			
		Min	Max	Min	Mean	Max	Min	Mean	Max	Unit
Write Cycle										
t_{WC}	Write cycle time	55.0	-	pass	-	-	pass	-	-	ns
t_{SCE}	CE LOW to write end	-	40.0	18.00	18.72	20.31	24.77	26.16	27.34	ns
t_{AW}	Address setup to write end	-	40.0	20.87	21.47	22.94	26.91	28.35	29.53	ns
t_{HA}	Address hold from write end	0	-	-6.56	-6.18	-5.69	-11.76	-11.02	-10.66	ns
t_{SA}	Address setup to write start	0	-	-9.94	-8.67	-7.88	-7.44	-7.15	-6.84	ns
t_{PWE}	WE pulse width	-	40.0	13.25	14.60	17.44	5.74	6.09	6.45	ns
t_{BW}	Byte Enable to write end	-	40.0	20.50	21.36	22.94	27.07	28.52	30.02	ns
t_{SD}	Data setup to write end	-	25.0	10.69	11.49	12.81	6.67	6.91	7.33	ns
t_{HD}	Data hold from write end	0	-	-6.69	-6.26	-5.75	-2.84	-2.68	-2.46	ns
t_{HZWE}	WE LOW to high-Z	-	20.0	6.21	6.22	6.23	6.20	6.22	6.24	ns
t_{LZWE}	WE HIGH to low-Z	10.0	-	15.70	15.78	15.85	15.85	15.89	15.93	ns

Document History Page

Rev.	ECN No.	Orig. of Change	Description of Change
**	6807771	ARAV	New Characterization Report

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC psoc.cypress.com
Clocks & Buffers clocks.cypress.com
Wireless wireless.cypress.com
Memories memory.cypress.com
Image Sensors image.cypress.com

PSoC Solutions

General psoc.cypress.com/solutions
Low Power/Low Voltage psoc.cypress.com/low-power
Precision Analog psoc.cypress.com/precision-analog
LCD Drive psoc.cypress.com/lcd-drive
CAN 2.0b psoc.cypress.com/can
USB psoc.cypress.com/usb

CY62157EV18 MoBL

8-Mbit (512K × 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65 V–2.25 V
- Pin compatible with CY62157DV18 and CY62157DV20
- Ultra low standby power
  - Typical Standby current: 2 µA
  - Maximum Standby current: 8 µA
- Ultra low active power
  - Typical active current: 6 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) package

Functional Description

The CY62157EV18 is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

- Deselected ($\overline{CE}_1$ HIGH or CE_2 LOW)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or
- Write operation is active ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

Write to the device by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

Read from the device by taking Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 13 for a complete description of read and write modes.

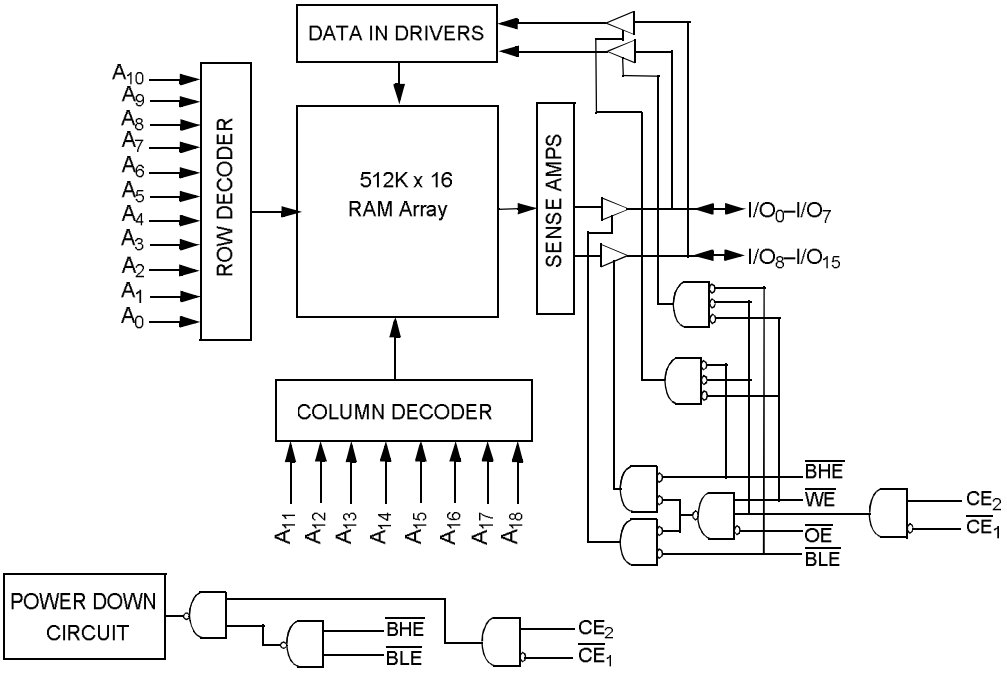
For a complete list of related documentation, click here.

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC}, (mA)				Standby, I_{SB2} (µA)	
					f = 1MHz		f = f_{max}			
	Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62157EV18	1.65	1.8	2.25	55	6	7	18	25	2	8

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

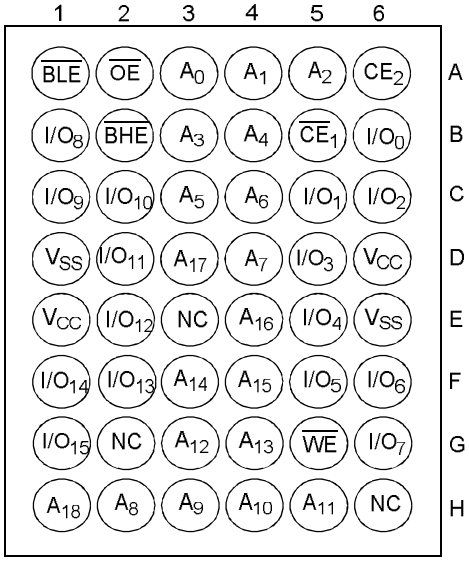
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball VFBGA pinout (Top View) [2]



Note
2. NC pins are not connected on the die.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.2 V to 2.45 V (V_{CCmax} + 0.2 V)

DC voltage applied to outputs in High-Z state [3, 4] ..... –0.2 V to 2.45 V (V_{CCmax} + 0.2 V)

DC input voltage [3, 4] ..... –0.2 V to 2.45 V (V_{CCmax} + 0.2 V)

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (in accordance with MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [5]
CY62157EV18LL	Industrial	–40 °C to +85 °C	1.65 V to 2.25 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA	V_{CC} = 1.65 V	1.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA	V_{CC} = 1.65 V	–	–	0.2	V
V_{IH}	Input HIGH voltage	V_{CC} = 1.65 V to 2.25 V		1.4	–	V_{CC} + 0.2 V	V
V_{IL}	Input LOW voltage	V_{CC} = 1.65 V to 2.25 V		–0.2	–	0.4	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	18	25	mA
		f = 1 MHz		–	6	7	mA
I_{SB1} [7]	Automatic CE power down current – CMOS inputs	$\overline{CE}_1$ ≥ V_{CC}–0.2 V or CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V), f = f_{max} (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC} = $V_{CC(max)}$.		–	2	8	µA
I_{SB2} [7]	Automatic CE power down current – CMOS Inputs	$\overline{CE}_1$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$.		–	2	8	µA

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.5 V for pulse durations less than 20 ns.
5. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB1}/I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

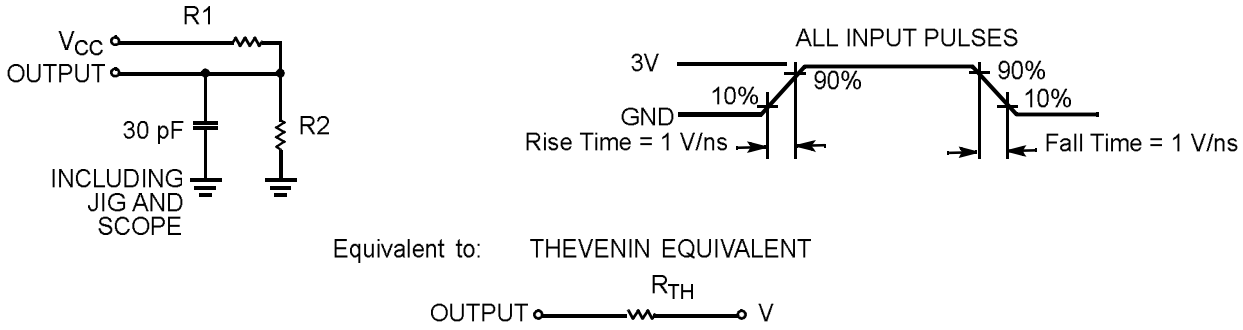
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	BGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	36.92	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.55	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	Value	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.80	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

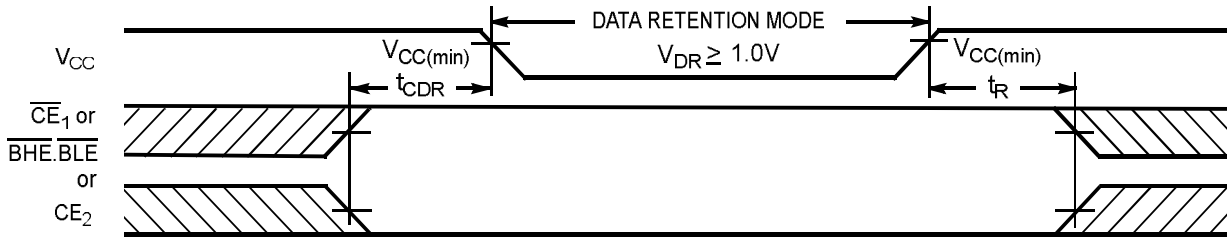
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} [10]	Data retention current	$1.2\ V \le V_{CC} \le V_{CC\ (max)}$, $\overline{CE}_1 \ge V_{CC} - 0.2\ V$, $CE_2 \le 0.2\ V$, $V_{IN} \ge V_{CC} - 0.2\ V$ or $V_{IN} \le 0.2\ V$	–	5	9	µA
t_{CDR} [11]	Chip deselect to data retention time		0	–	–	ns
t_R [12]	Operation recovery time		55	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform [13]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\ °C$.
10. Chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \ge 100\ µs$ or stable at $V_{CC(min)} \ge 100\ µs$.
13. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	55	–	ns
t_{AA}	Address to data valid	–	55	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low-Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High-Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power down	–	55	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to data valid	–	55	ns
t_{LZBE} [18]	$\overline{BLE}/\overline{BHE}$ LOW to Low-Z [16]	10	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to High-Z [16, 17]	–	18	ns
Write Cycle [19, 20]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [16]	10	–	ns

Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 6.
15. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the byte enable and/or chip enable signals as described in the Application Notes AN13842 and AN66311. However, the issue has been fixed and in production now, and hence, these Application Notes are no longer applicable. They are available for download on our website as they contain information on the date code of the parts, beyond which the fix has been in production.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the output enters a high impedance state.
18. If both byte enables are toggled together, this value is 10 ns.
19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
20. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [21, 22]

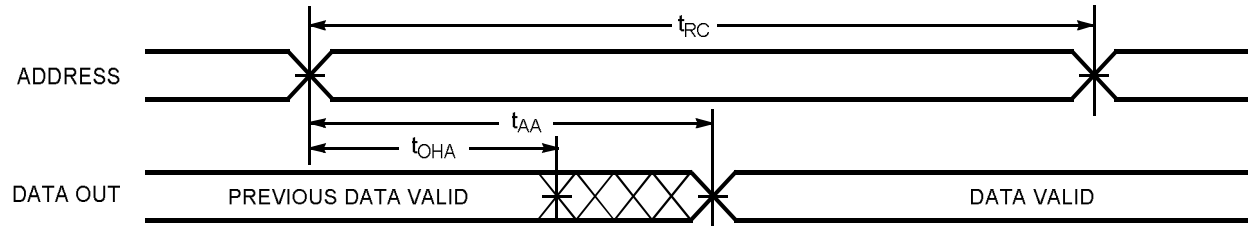
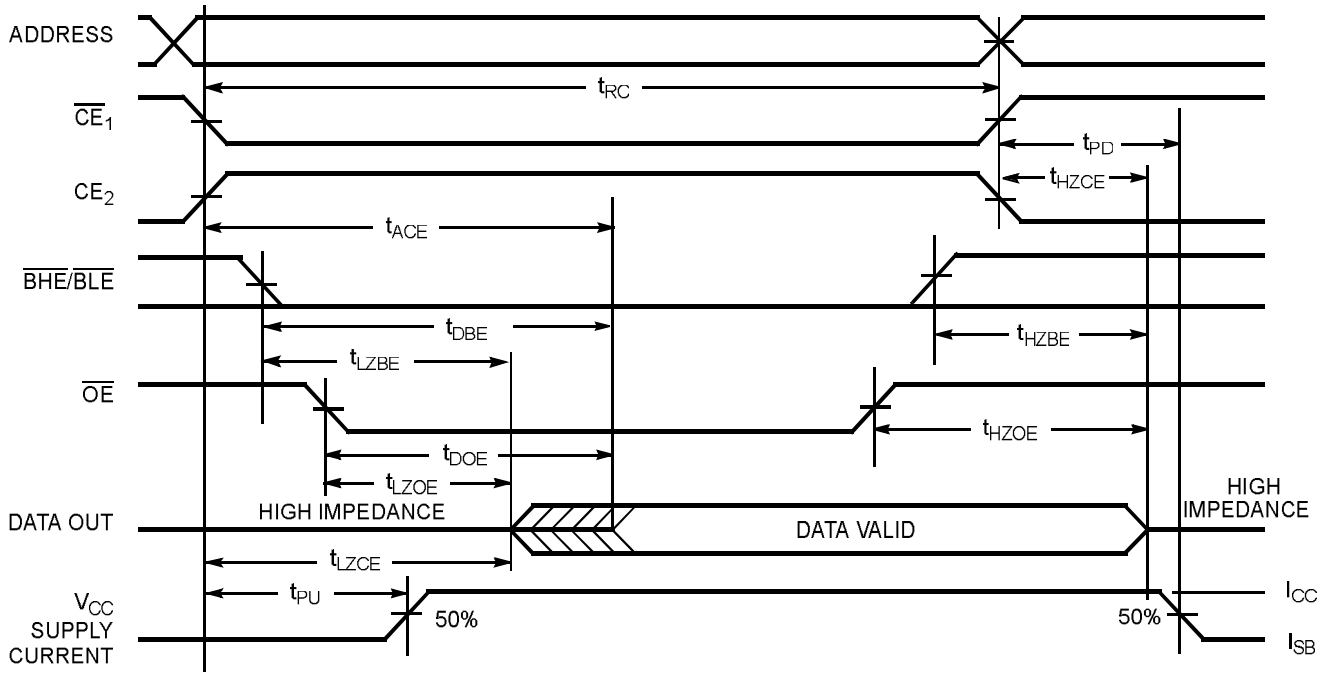


Figure 5. Read Cycle 2 ($\overline{OE}$ Controlled) [22, 23]

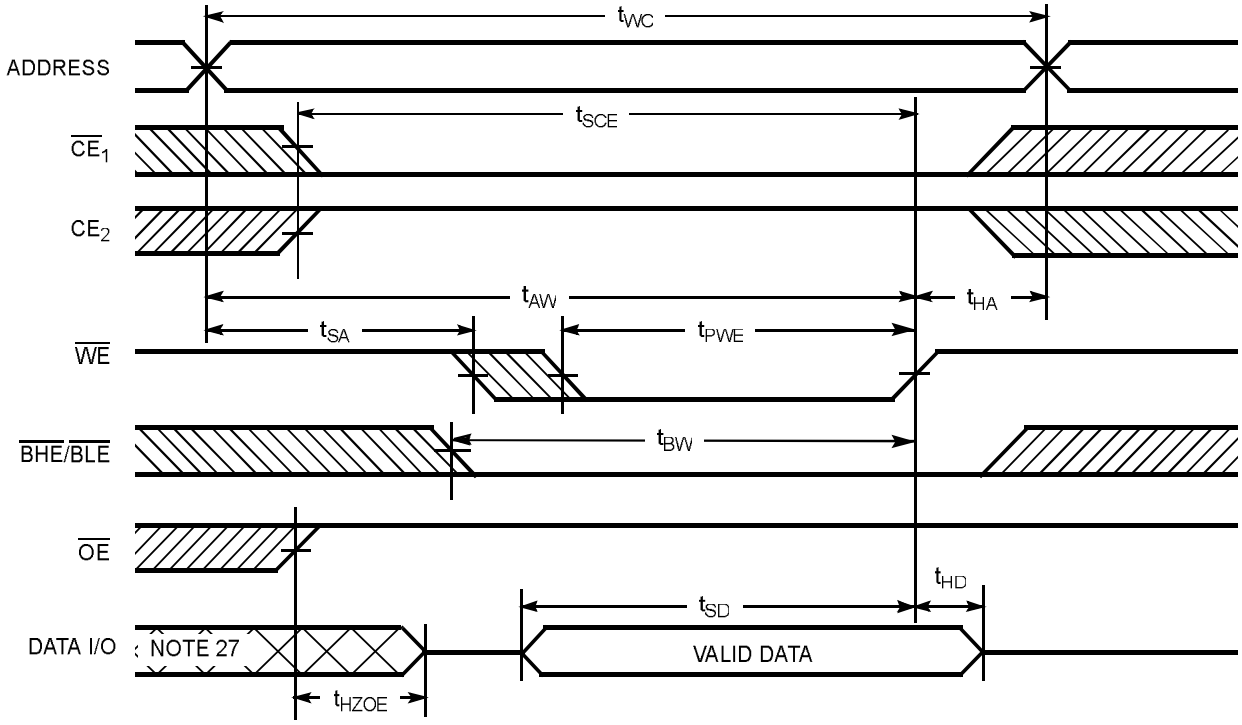


Notes

21. The device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
22. $\overline{WE}$ is HIGH for read cycle.
23. Address valid before or similar to $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 ($\overline{WE}$ Controlled) [24, 25, 26]

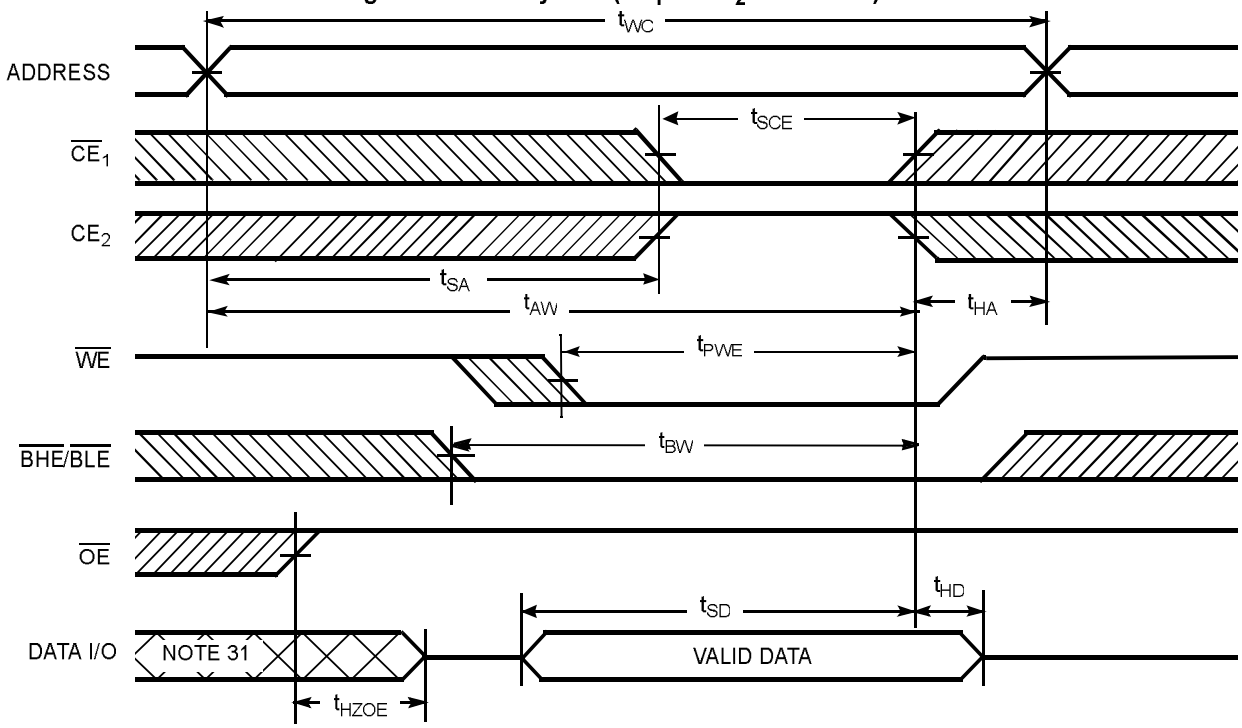


Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
26. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
27. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled) [28, 29, 30]



Notes

28. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
29. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
30. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
31. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [32, 33]

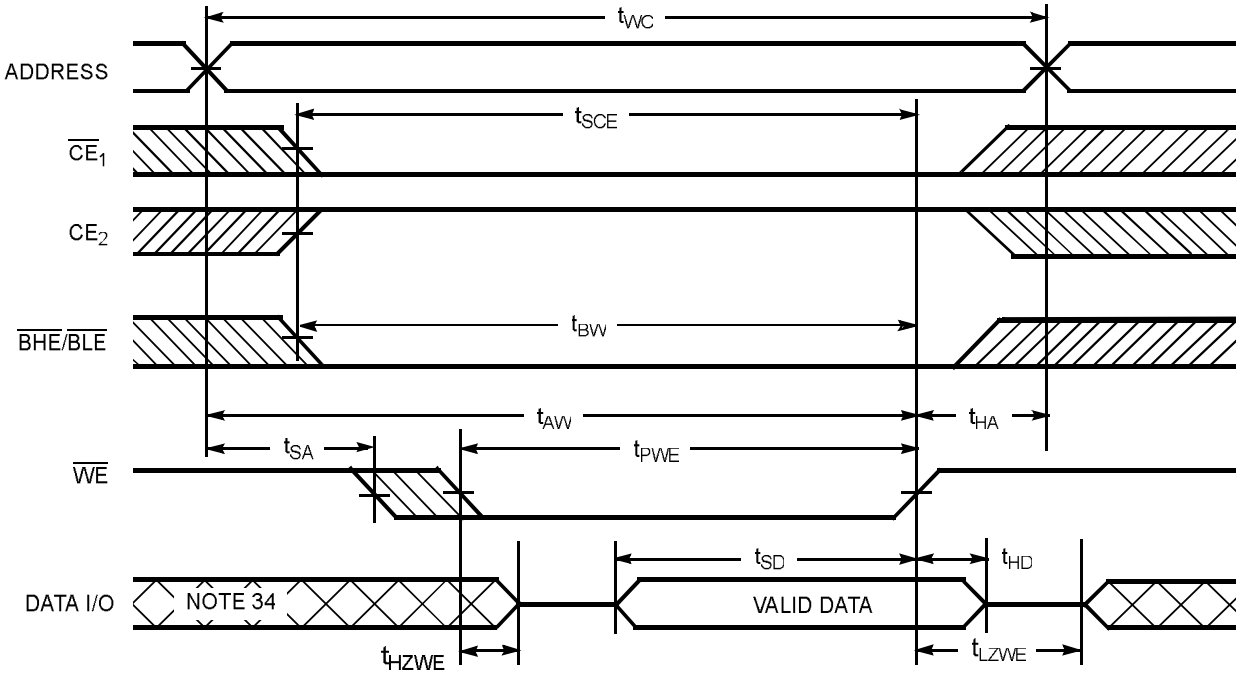
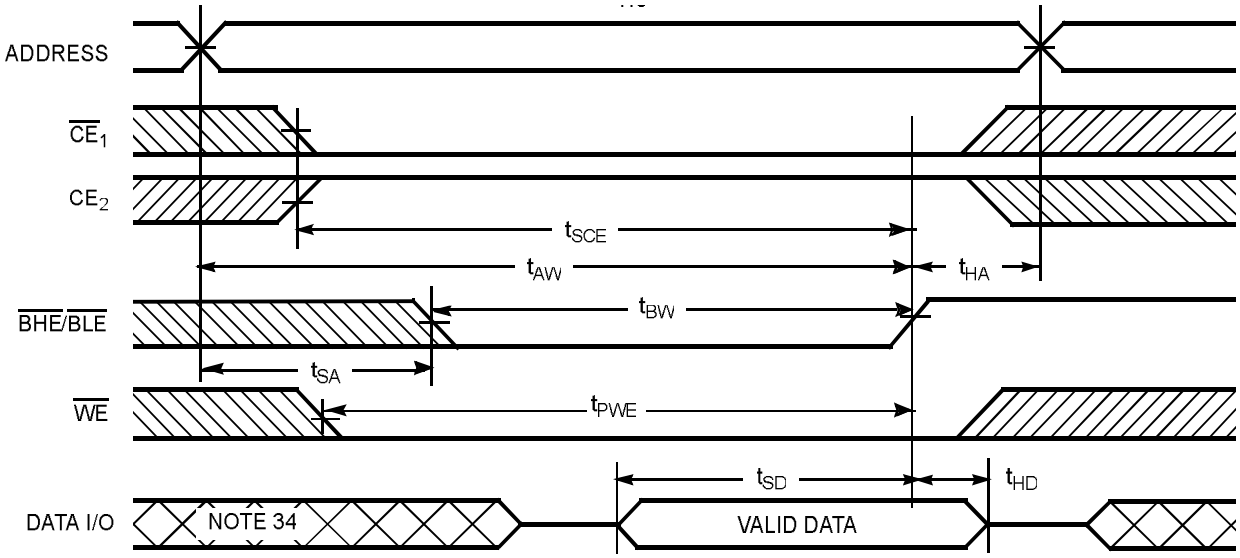


Figure 9. Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW) [32]



Notes

32. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
33. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
34. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X[35]	X	X	X[35]	X[35]	High-Z	Deselect/Power down	Standby (I_{SB})
X[35]	L	X	X	X[35]	X[35]	High-Z	Deselect/Power down	Standby (I_{SB})
X[35]	X[35]	X	X	H	H	High-Z	Deselect/Power down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High-Z (I/O_0–I/O_7); Data out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High-Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High-Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O_0–I/O_7); High-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High-Z (I/O_0–I/O_7); Data in (I/O_8–I/O_{15})	Write	Active (I_{CC})

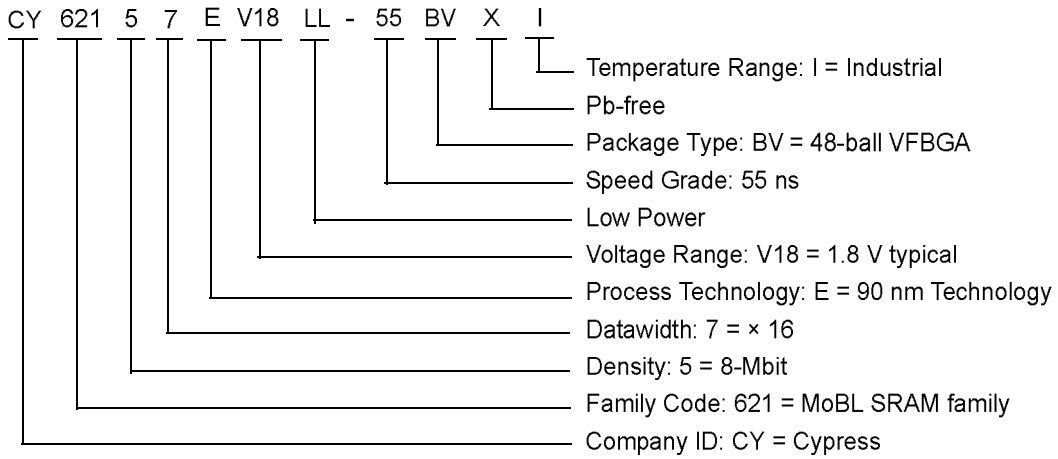
Note
35. The 'X' (Don't care) state for the Chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62157EV18LL-55BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

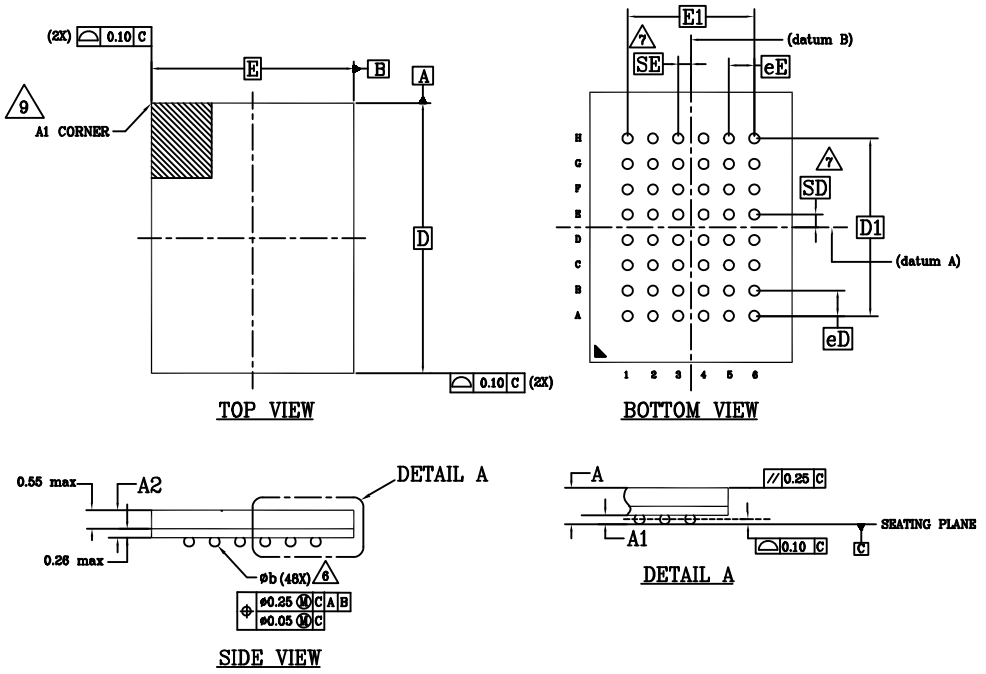
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
µA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05490			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	202862	01/27/2004	New data sheet.
*A	291272	11/19/2004	Changed status from Advance Information to Preliminary. Updated Features: Updated description. Updated Operating Range: Updated Note 5 (Replaced "100 µs wait time" with "200 µs wait time"). Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 4 µA to 4.5 µA. Updated Switching Characteristics: Changed minimum value of t_{OHA} parameter from 6 ns to 10 ns corresponding to both 35 ns and 45 ns speed bins. Changed maximum value of t_{DOE} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZOE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 12 ns to 18 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZCE} parameter from 15 ns to 22 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZBE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZBE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SCE} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin. Changed minimum value of t_{SCE} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{AW} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin. Changed minimum value of t_{AW} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{BW} parameter from 25 ns to 30 ns corresponding to 35 ns speed bin. Changed minimum value of t_{BW} parameter from 40 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 15 ns to 18 ns corresponding to 35 ns speed bin. Changed minimum value of t_{SD} parameter from 20 ns to 22 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZWE} parameter from 12 ns to 15 ns corresponding to 35 ns speed bin. Changed maximum value of t_{HZWE} parameter from 15 ns to 18 ns corresponding to 45 ns speed bin. Updated Ordering Information: Updated part numbers.

Document History Page (continued)

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05490			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*B	444306	04/13/2006	Changed status from Preliminary to Final. Removed 35 ns Speed Bin related information in all instances across the document. Removed "L" from the part numbers across the document. Updated Pin Configuration: Updated Figure 1 (Changed ball E3 from DNU to NC). Removed Note "DNU pins have to be left floating or tied to Vss to ensure proper application." and its reference. Updated Maximum Ratings: Updated ratings corresponding to "Supply Voltage to Ground Potential", "DC Voltage Applied to Outputs in High Z State", "DC Input Voltage" (Replaced "2.4 V" with "2.45 V"). Updated Electrical Characteristics: Changed typical value of I_{CC} parameter from 16 mA to 18 mA corresponding to Test Condition "f = f_{MAX} = 1/t_{RC}". Changed maximum value of I_{CC} parameter from 28 mA to 25 mA corresponding to Test Condition "f = f_{MAX} = 1/t_{RC}". Changed maximum value of I_{CC} parameter from 2.3 mA to 3 mA corresponding to Test Condition "f = 1 MHz". Changed typical value of I_{SB1} parameter from 0.9 µA to 2 µA. Changed maximum value of I_{SB1} parameter from 4.5 µA to 8 µA. Changed typical value of I_{SB2} parameter from 0.9 µA to 2 µA. Changed maximum value of I_{SB2} parameter from 4.5 µA to 8 µA. Updated Thermal Resistance: Updated values of Θ_{JA}, Θ_{JC} parameters corresponding to BGA package. Updated AC Test Loads and Waveforms: Updated Figure 2 (Changed Test Load Capacitance from 50 pF to 30 pF). Updated Data Retention Characteristics: Added 1 µA as typical value for I_{CCDR} parameter. Changed maximum value of I_{CCDR} parameter from 4.5 µA to 3 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns. Changed minimum value of t_{LZBE} parameter from 6 ns to 5 ns. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns. Added Note 18 and referred the same note in t_{LZBE} parameter. Updated Ordering Information: Updated part numbers. Removed "Package Name" column. Added "Package Diagram" column. Updated Package Diagram: spec 51-85150 – Changed revision from *B to *D. Updated to new template.
*C	571786	12/01/2006	Removed 45 ns Speed Bin related information in all instances across the document. Added 55 ns Speed Bin related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*D	908120	04/04/2007	Updated Electrical Characteristics: Added Note 7 and referred the same note in I_{SB2} parameter. Updated Switching Characteristics: Added Note 15 and referred the same note in "Parameter" column.

Document History Page (continued)

Document Title: CY62157EV18 MoBL, 8-Mbit (512K × 16) Static RAM Document Number: 38-05490			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*E	2934396	06/03/2010	Updated Switching Characteristics: Added Note 35 and referred the same note in "X" under $\overline{CE}_1$ and CE_2 columns. Updated Package Diagram: spec 51-85150 – Changed revision from *D to *E. Updated to new template.
*F	3110053	12/14/2010	Changed Table Footnotes to Notes. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagram: spec 51-85150 – Changed revision from *E to *F.
*G	3243545	04/28/2011	Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	3295175	06/29/2011	Updated Electrical Characteristics: Updated Note 7. Referred Note 7 in I_{SB1} parameter. Updated Data Retention Characteristics: Added Note 10 and referred the same note in I_{CCDR} parameter. Updated Truth Table: Updated Note 35.
*I	4102022	08/22/2013	Updated Switching Characteristics: Updated Note 15. Updated Package Diagram: spec 51-85150 – Changed revision from *F to *H. Updated to new template.
*J	4384935	05/20/2014	Updated Switching Characteristics: Added Note 20 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 33 and referred the same note in Figure 8. Completing Sunset Review.
*K	4576526	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*L	5759379	06/01/2017	Updated Thermal Resistance values. Updated to new template. Completing Sunset Review.
*M		02/26/2020	Updated Features: Updated description. Updated Product Portfolio: Updated all values of "Operating I_{CC}" corresponding to "f = 1 MHz". Updated Electrical Characteristics: Updated all values of I_{CC} parameter corresponding to "55 ns" and "f = 1 MHz". Updated Thermal Resistance: Updated values of Θ_{JA}, Θ_{JC} parameters corresponding to BGA package. Updated Data Retention Characteristics: Updated details in "Conditions" column and updated all values of I_{CCDR} parameter. Updated Package Diagram: spec 51-85150 – Changed revision from *H to *I. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

CY62158EV30 MoBL

8-Mbit (1024K × 8) Static RAM

Features

- Very high speed: 45 ns
  - Wide voltage range: 2.20 V–3.60 V
- Pin compatible with CY62158DV30
- Ultra low standby power
  - Typical standby current: 2 µA
  - Maximum standby current: 8 µA
- Ultra low active power
  - Typical active current: 6 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description

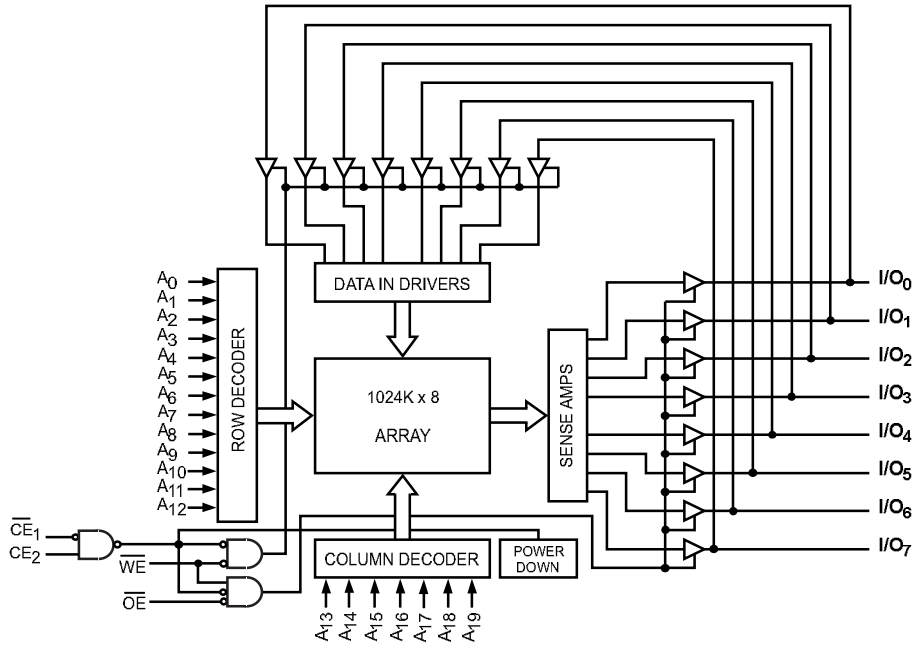
The CY62158EV30 is a high performance CMOS static RAM organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption. Placing the device into standby mode reduces power consumption significantly when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and $\overline{OE}$ LOW while forcing the $\overline{WE}$ HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins. See Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

Logic Block Diagram



Contents

Pin Configurations

Figure 1. 48-ball VFBGA pinout (Top View) [1]

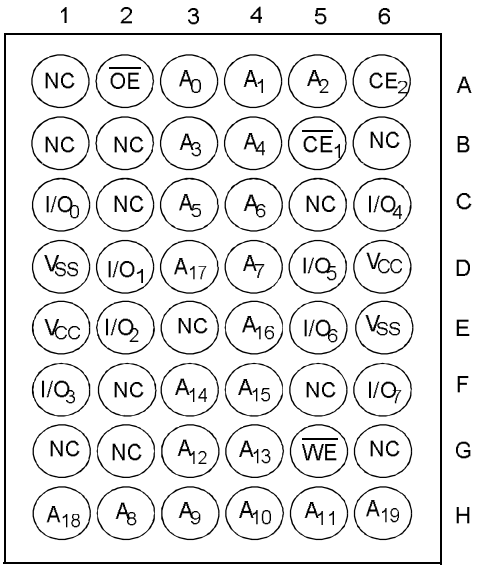
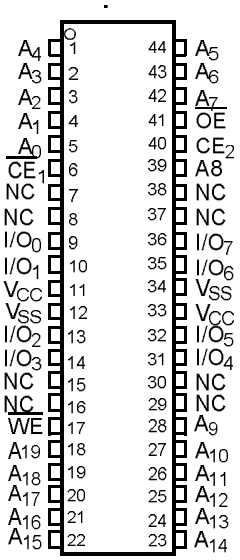


Figure 2. 44-pin TSOP II pinout (Top View) [1]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby, I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62158EV30LL	2.2	3.0	3.6	45	6	7	18	25	2	8

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC Voltage Applied to Outputs in High Z State [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC Input Voltage [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch up Current ..... > 200 mA

Operating Range

Product	Range	Ambient Temperature (T_A)	V_{CC}[5]
CY62158EV30LL	Industrial	–40 °C to +85 °C	2.2 V–3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		V_{CC} = 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3 V	V
V_{IIL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC} = 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	$V_{CC} = V_{CCmax}$, I_{OUT} = 0 mA, CMOS levels	–	18	25	mA
		f = 1 MHz		–	6	7	mA
I_{SB1}	Automatic CE power down current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V, $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$ and $\overline{WE}$), V_{CC} = 3.60 V		–	2	8	µA
I_{SB2}[7]	Automatic CE Power down Current — CMOS inputs	$\overline{CE}_1 \geq V_{CC}$ – 0.2 V or $CE_2 \leq$ 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or $V_{IN} \leq$ 0.2 V, f = 0, V_{CC} = 3.60 V		–	2	8	µA

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse duration less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.

Capacitance

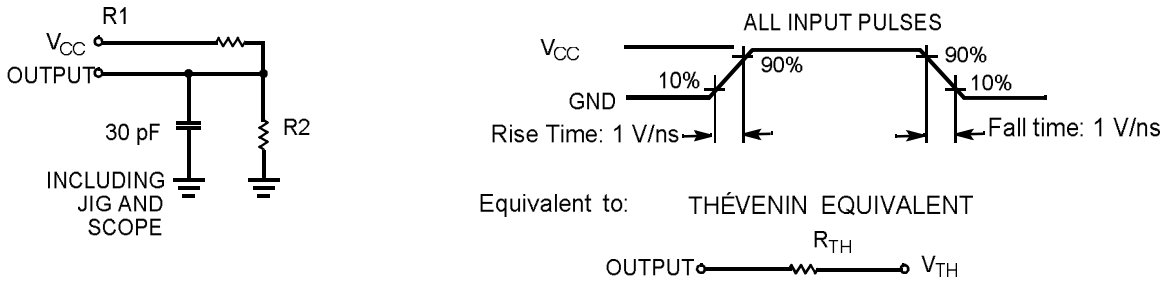
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball BGA	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	36.92	65.91	°C/W
Θ_{JC}	Thermal resistance (junction to case)		13.55	13.96	°C/W

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

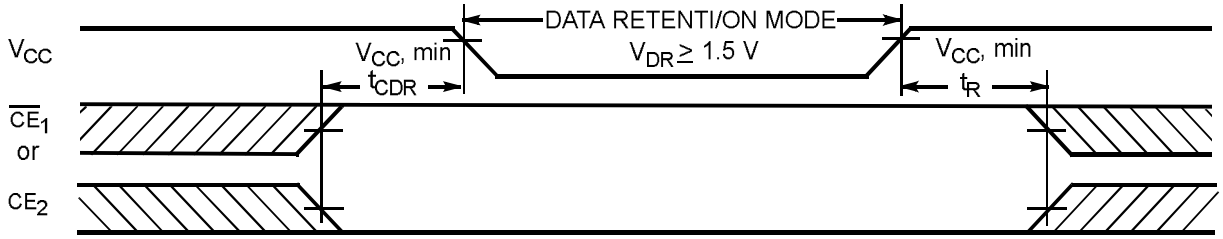
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ[9]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	–	V
I_{CCDR}[10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	3.2	8	µA
t_{CDR}[11]	Chip deselect to data retention time		0	–	–	ns
t_R[12]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2}/I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data Hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[15]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[15, 16]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[15]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to High Z[15, 16]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to Power Down	–	45	ns
Write Cycle [17, 18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	35	–	ns
t_{AW}	Address setup to Write End	35	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to Write End	25	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[15, 16]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[15]	10	–	ns

Notes

13. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 3 on page 5.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled) [19, 20]

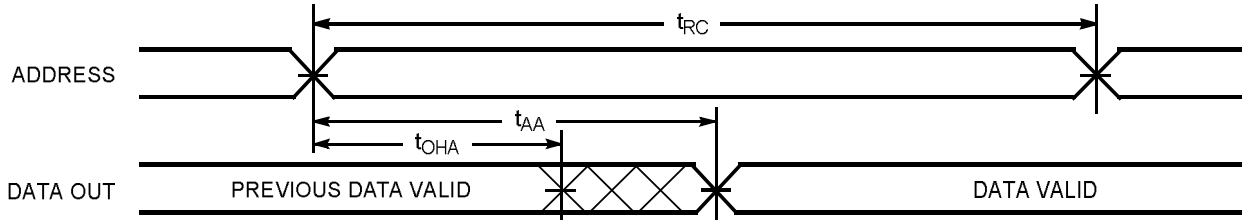
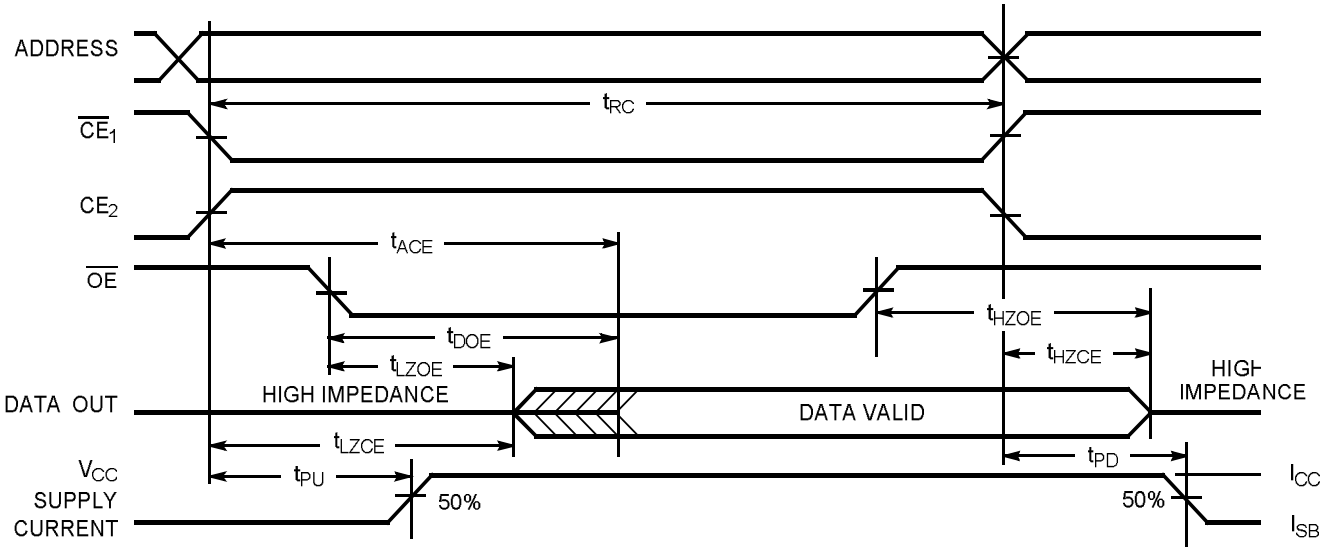


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled) [20, 21]



Notes
19. Device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{WE}$ Controlled) [22, 23, 24]

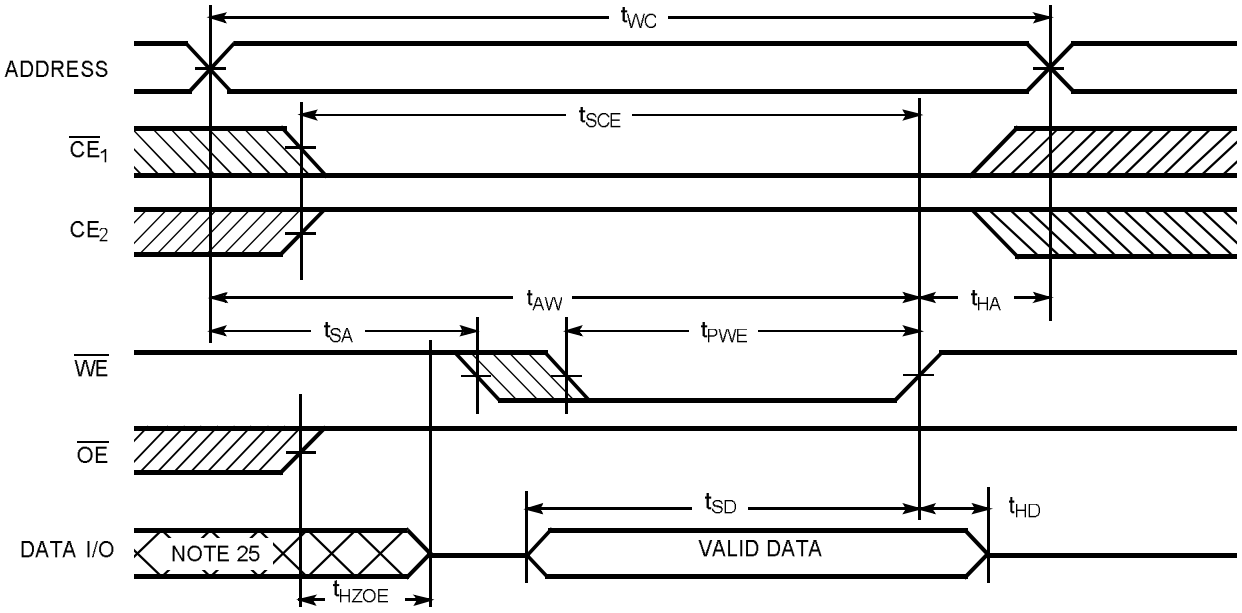
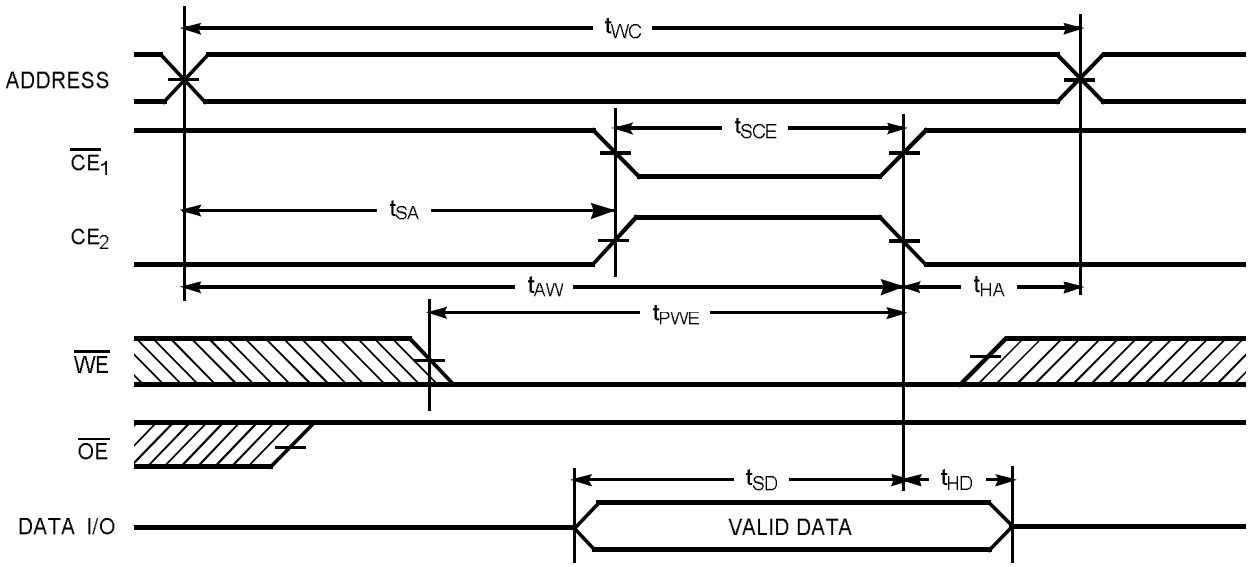


Figure 8. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [22, 23, 24]

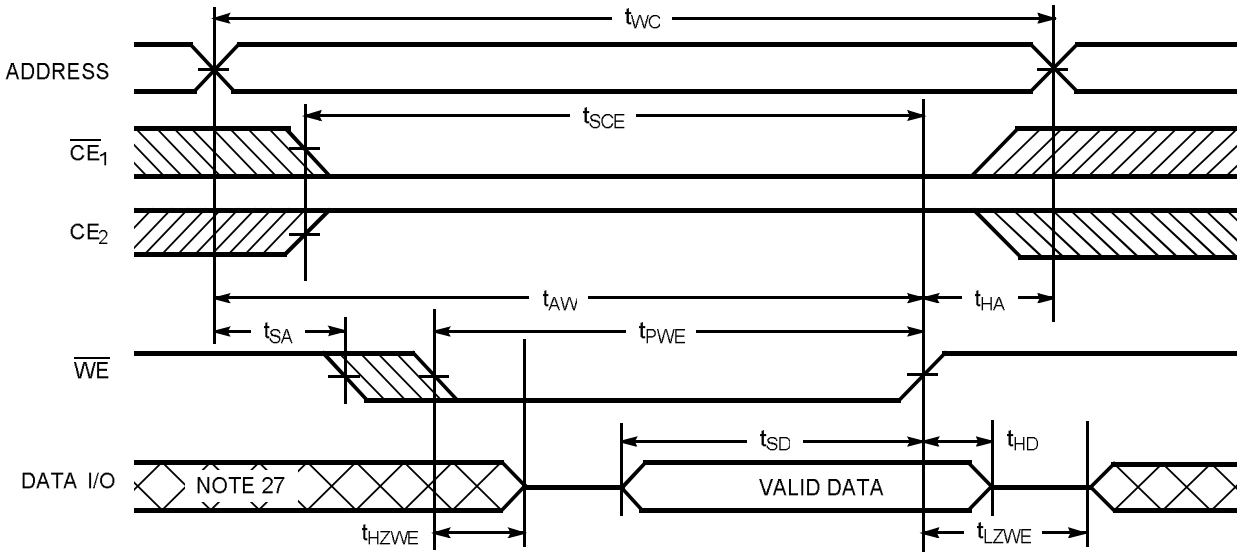


Notes

22. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [26, 28]



Notes
26. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.
28. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X[29]	X	X	High Z	Deselect/Power down	Standby (I_{SB})
X[29]	L	X	X	High Z	Deselect/Power down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

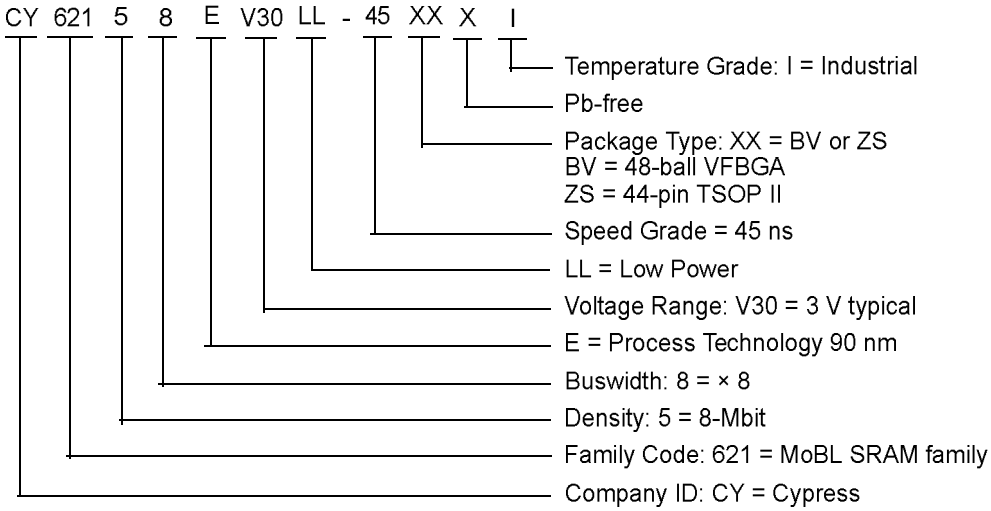
Note
29. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62158EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62158EV30LL-45ZSXI	51-85087	44-pin TSOP Type II (Pb-free)	

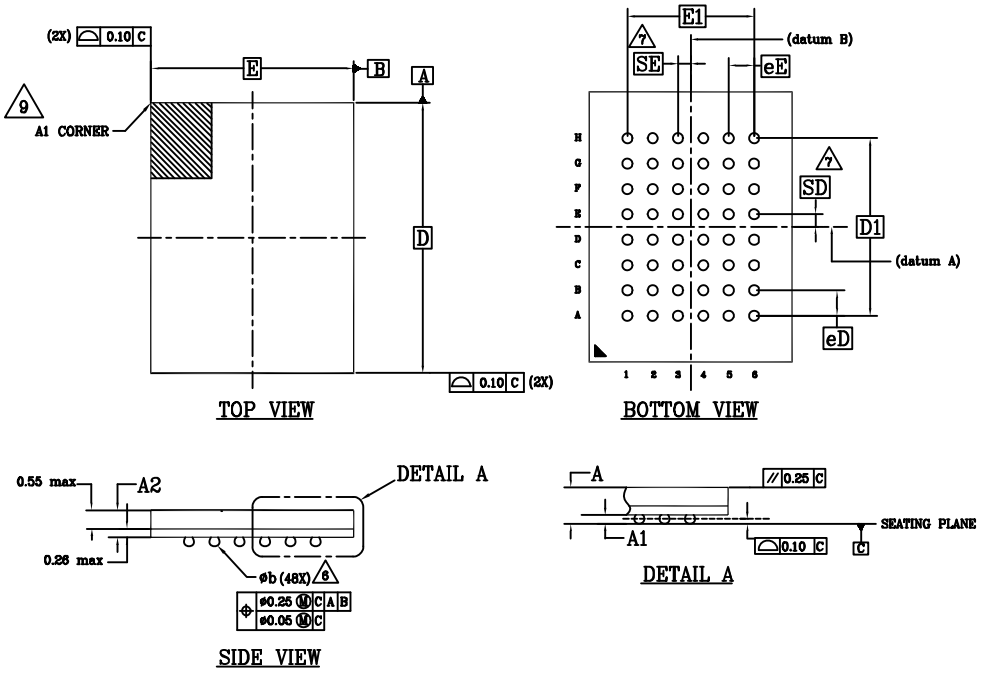
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

Figure 10. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
A2	-	-	0.81
D	8.00 BSC		
E	6.00 BSC		
D1	5.25 BSC		
E1	3.75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

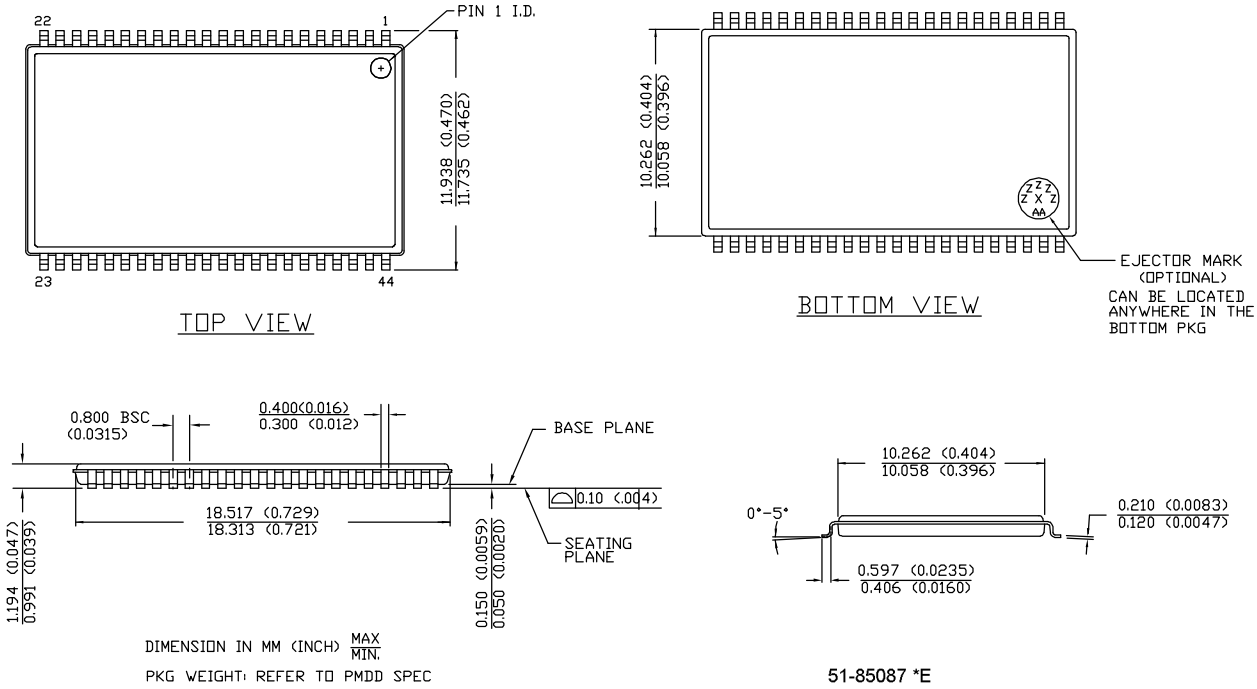
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Package Diagrams (continued)

Figure 11. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62158EV30 MoBL, 8-Mbit (1024K × 8) Static RAM Document Number: 38-05578			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	270329	09/28/2004	New data sheet.
*A	291271	11/19/2004	Changed status from Advance Information to Preliminary. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 4 µA to 4.5 µA.
*B	444306	04/13/2006	Converted from Preliminary to Final. Removed 35 ns Speed Bin related information in all instances across the document. Removed 44-pin TSOP II Package related information in all instances across the document. Included 48-pin TSOP I Package related information in all instances across the document. Removed "L" from the part numbers across the document. Updated Product Portfolio: Changed maximum value of "Operating I_{CC}" from 2.3 mA to 3 mA corresponding to "f = 1 MHz". Changed typical value of "Operating I_{CC}" from 16 mA to 18 mA corresponding to "f = f_{max}". Changed maximum value of "Operating I_{CC}" from 28 mA to 25 mA corresponding to "f = f_{max}". Changed typical value of "Standby I_{SB2}" from 0.9 µA to 2 µA. Changed maximum value of "Standby I_{SB2}" from 4.5 µA to 8 µA. Updated Electrical Characteristics: Changed typical value of I_{SB1} parameter from 0.9 µA to 2 µA. Changed maximum value of I_{SB1} parameter from 4.5 µA to 8 µA. Changed typical value of I_{SB2} parameter from 0.9 µA to 2 µA. Changed maximum value of I_{SB2} parameter from 4.5 µA to 8 µA. Updated AC Test Loads and Waveforms: Updated Figure 3 (Changed Test Load Capacitance from 50 pF to 30 pF). Updated Data Retention Characteristics: Added 2 µA as typical value for I_{CCDR} parameter. Changed maximum value of I_{CCDR} parameter from 4.5 µA to 5 µA. Changed minimum value of t_R parameter from 100 µs to t_{RC} ns. Updated Switching Characteristics: Changed minimum value of t_{LZOE} parameter from 3 ns to 5 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZCE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Changed maximum value of t_{HZCE} parameter from 22 ns to 18 ns corresponding to 45 ns speed bin. Changed minimum value of t_{PWE} parameter from 30 ns to 35 ns corresponding to 45 ns speed bin. Changed minimum value of t_{SD} parameter from 22 ns to 25 ns corresponding to 45 ns speed bin. Changed minimum value of t_{LZWE} parameter from 6 ns to 10 ns corresponding to 45 ns speed bin. Updated Ordering Information: Updated part numbers. Removed "Package Name" column. Added "Package Diagram" column. Updated Package Diagrams: spec 51-85150 – Changed revision from *B to *D. Removed spec 51-85087 *A. Added spec 51-85183 *A. Updated to new template.

Document History Page (continued)

Document Title: CY62158EV30 MoBL, 8-Mbit (1024K × 8) Static RAM Document Number: 38-05578			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*C	467052	06/06/2006	Included 44-pin TSOP II Package related information in all instances across the document. Updated Features: Added Note "For 48-pin TSOP I pin configuration and ordering information, please refer to CY62157EV30 Data sheet." and referred the same note in 48-pin TSOP I package. Updated Ordering Information: Updated part numbers. Updated Package Diagrams: Removed spec 51-85183 *A. Added spec 51-85087 *A,
*D	1015643	04/28/2007	Updated Electrical Characteristics: Added Note 7 and referred the same note in I_{SB2} parameter. Updated Data Retention Characteristics: Added Note 10 and referred the same note in I_{CCDR} parameter.
*E	2934396	06/03/2010	Updated Truth Table: Added Note 29 and referred the same note in "X" under $\overline{CE}_1$ and CE_2 columns. Updated Package Diagrams: spec 51-85150 – Changed revision from *D to *E. spec 51-85087 – Changed revision from *A to *C. Updated to new template.
*F	3110202	12/14/2010	Updated Logic Block Diagram. Updated Ordering Information: No change in part numbers. Added Ordering Code Definitions. Updated Package Diagrams: spec 51-85150 – Changed revision from *E to *F.
*G	3269641	05/30/2011	Removed 48-pin TSOP I Package related information in all instances across the document. Updated Functional Description: Removed the note "For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at http://www.cypress.com." and its reference. Updated Data Retention Characteristics: Changed minimum value of t_R parameter from t_{RC} ns to 45 ns. Added Acronyms and Units of Measure. Updated to new template. Completing Sunset Review.
*H	3598409	04/24/2012	Updated Package Diagrams: spec 51-85150 – Changed revision from *F to *G. spec 51-85087 – Changed revision from *C to *D. Completing Sunset Review.
*I	4100078	08/20/2013	Updated Switching Characteristics: Added Note 13 and referred the same note in "Parameter" column. Updated Package Diagrams: spec 51-85150 – Changed revision from *G to *H. spec 51-85087 – Changed revision from *D to *E. Updated to new template.
*J	4576526	11/21/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end. Updated Switching Characteristics: Added Note 18 and referred the same note in "Write Cycle". Updated Switching Waveforms: Added Note 28 and referred the same note in Figure 9.

Document History Page (continued)

Document Title: CY62158EV30 MoBL, 8-Mbit (1024K × 8) Static RAM Document Number: 38-05578			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*K	4790694	06/08/2015	Updated Maximum Ratings: Referred Notes 3, 4 in "Supply Voltage to Ground Potential". Updated to new template. Completing Sunset Review.
*L	5979591	11/29/2017	Updated Cypress Logo and Copyright.
*M		02/26/2020	Updated Features: Updated description. Updated Product Portfolio: Updated all values of "Operating I_{CC}" corresponding to "f = 1 MHz". Updated Electrical Characteristics: Updated all values of I_{CC} parameter corresponding to "45 ns" and "f = 1 MHz". Updated Thermal Resistance: Updated all values of Θ_{JA}, Θ_{JC} parameters corresponding to all packages. Updated Data Retention Characteristics: Updated all values of I_{CCDR} parameter. Updated Package Diagrams: spec 51-85150 – Changed revision from *H to *I. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Code Examples | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Marketing Part Number	Sample Order Part Number	Sample Availability
CY62157EV18LL-55BVXI	CY62157EV18LL9-55BVXI	Subject to leadtime
CY62157EV18LL-55BVXIT	CY62157EV18LL9-55BVXI	Subject to leadtime
CY62157EV30LL-45BVXI	CY62157EV30LL9-45BVXI	Available
CY62157EV30LL-45BVXIT	CY62157EV30LL9-45BVXI	Available
CY62157EV30LL-45ZSXI	CY62157EV30LL9-45ZSXI	Available
CY62157EV30LL-45ZSXIT	CY62157EV30LL9-45ZSXI	Available
CY62157EV30LL-45ZXI	CY62157EV30LL9-45ZXI	Available
CY62157EV30LL-45ZXIT	CY62157EV30LL9-45ZXI	Available
CY62158EV30LL-45BVXI	CY62158EV30LL9-45BVXI	Available
CY62158EV30LL-45BVXIT	CY62158EV30LL9-45BVXI	Available
CY62158EV30LL-45ZSXI	CY62158EV30LL9-45ZSXI	Available
CY62158EV30LL-45ZSXIT	CY62158EV30LL9-45ZSXI	Available
CG8610AA	CY62157EV30LL9-45BVXI	Available
CG8610AAT	CY62157EV30LL9-45BVXI	Available
CG8237AAT	CY62157EV30LL9-45BVXI	Available
CG8238AA	CY62157EV30LL9-45ZXI	Available
CG8888AM	CY62158EV30LL9-45ZSXI	Available
CG8888AMT	CY62158EV30LL9-45ZSXI	Available
CG8984AM	CY62157EV30LL9-45BVXI	Available
CG8984AMT	CY62157EV30LL9-45BVXI	Available
CG8985AM	CY62157EV30LL9-45ZSXI	Available
CG8985AMT	CY62157EV30LL9-45ZSXI	Available