Product Change Notification - SYST-14ASKF355

Date:

17 Feb 2020

Product Category:

Microprocessors

Affected CPNs:

Notification subject:

Data Sheet - SAMA5D2 Series Datasheet Document Revision

Notification text:

SYST-14ASKF355

Microchip has released a new Product Documents for the SAMA5D2 Series Datasheet of devices. If you are using one of these devices please read the document located at SAMA5D2 Series Datasheet.

Notification Status: Final

Description of Change:

1) Global: In all Register Summary tables, bit order now shown from MSB to LSB.

2) Pinout: Table Pin Description (all packages): modified direction of FLEXCOM3_IO3.

3) Standard Boot Strategies: Supported External Crystal/External Clocks: updated clock frequency. NAND Flash PMECC Register: updated nbSectorPerPage description.

4) Matrix (H64MX/H32MX): Register Summary: added MATRIX_SRTSR0 at offset 0x0280.

5) Reset Controller (RSTC): RSTC_MR: updated reset value.

6) Shutdown Controller (SHDWC): a)Updated Wake-Up Inputs. b) SHDW_SR: added note. c) SHDW_WUIR: added WKUPT1 detail.

7) Real-time Clock (RTC): a) Replaced SLCK by slow clock throughout. b) Updated Reference Clock. c) Updated Alarm, RTC Internal Free-Running Counter Error Checking, Gregorian and Persian Modes, RTC Accurate Clock Calibration d) Updated Time/Calendar Update Timing Diagram, Gregorian and Persian Modes Update Sequence, UTC Time Update Timing Diagram, UTC Mode Update Sequence. e) RTC_CR: updated UPDCAL and UPDTIM bit descriptions. f) RTC_SCCR: updated description.

8) Power Management Controller (PMC): a) Updated the table Clock Assignments with new rows for UART, TWI and SPI. b) PMC_PCKx: modified description of PRES field.

9) AHB Multiport DDR-SDRAM Controller (MPDDRC): a) Block Diagram: updated description. b) DDR2-SDRAM Initialization: added TRFC constraint content c) Corrected Interleaved Mapping DDR-SDRAM Configuration Mapping: 8K Rows, 512/1024/2048 Columns, 4 Banks d) MPDDRC_CR: updated NDQS bit description. e) MPDDRC_LPR: updated CHG_FRQ bit description. f) MPDDRC_TPR1: TRFC field name corrected from Row Cycle Delay to Row Refresh cycle.

10) Static Memory Controller (SMC): In Description, replaced with one-bit error correction capability and supports two-bit error detection. In order to improve the overall system performance, the DATA phase of the transfer can be DMA-assisted. with new text.Scrambling/Unscrambling Function: replaced to prevent recovery with new text.

11) DMA Controller (XDMAC): Updated: a) XDMAC Block Diagram. b) BXKBEN bit description in XDMAC_GCFG.

12) LCD Controller (LCDC): a) Description: replaced AHB with system bus. b) Updated: LCDC PWM Controller, Power Management and Block Diagram c) Modified: 4:2:2 Planar Mode Chrominance Memory Mapping, Little Endian Organization for Byte 0x0, 0x1, 0x2, 0x3, 4:2:0 Planar Mode Chrominance Memory Mapping, Little Endian Organization for Byte 0x0, 0x1, 0x2, 0x3, 4:2:0 Planar

Mode Chrominance Memory Mapping, Little Endian Organization for Byte 0x4, 0x5, 0x6, 0x7, Base Layer with Window Overlay Optimization d) Added figure in Pixel Clock Period Configuration.

13) Ethernet MAC (GMAC): a) Changed all occurrences of GEMAC to GMAC. b) References to MDIO pin modified to GMDIO pin. c) Timestamp Unit: updated paragraph on GTSUCOMP and added figure GTSUCOMP Connection. d) GMAC_RRE.RXRER: modified description. e) GMAC_NSR: added note for the register reset value. f) GMAC_CBSCR: corrected inverted bits. g) GMAC_EFTSH: updated offset. h) Modified base offset and index for registers: GMAC_ISRPQx, GMAC_TBQBAPQx, GMAC_RBQBAPQx, GMAC_RBSRPQx, GMAC_IERPQx, GMAC_IDRPQx, GMAC_IMRPQx

14) Audio Class D Amplifier (CLASSD): a) Description: added a note. b) Embedded Characteristics: modified first item in the list. c) CLASSD Block Diagram: added note.

15) Serial Synchronous Controller (SSC): SSC_TFMR: updated DATDEF bit description

16) Two-wire Interface (TWIHS): a) Updated Master Performs a General Call. b) Updated TWIHS Read Operation with Multiple Data Bytes + Write Operation with Multiple Data Bytes (Sr). c) TWIHS_CWGR: updated CLDIV and CHDIV bit descriptions. d) Added detail: This register reads 0 if the FIFO is disabled (see TWI_CR to enable/disable the internal FIFO) in: TWIHS_FMR, TWIHS_FLR, TWIHS_FSR, TWIHS_FIMR

17) Flexible Serial Communication Controller (FLEXCOM): a) Updated FLEXCOM Block Diagram. b) Updated Master Performs a General Call. c) TWI Compatibility with I2C Standard: updated with Fast Mode Plus and High Speed Mode. d) TWI/SMBus Characteristics: updated for Fast Mode Plus and High-speed mode. e) Modes of Operation: updated for High-speed mode. f) Master Mode: updated Definition, Master Transmitter Mode and Master Receiver Mode. g) Updated TWI Read Operation with Multiple Data Bytes + Write Operation with Multiple Data Bytes (Sr). h) FLEX_US_CR: updated REQCLR description. i) FLEX_TWI_FILTR: removed bit PADFCFG. j) FLEX_US_RTOR: updated TO field description. k) FLEX_US_IDR: corrected OVRE bit description. l) Modified reset values for registers: FLEX_MR, FLEX_US_NER, FLEX_USMR, FLEX_US_MR (SPI_MODE) m) FLEX_TWI_CWGR: updated CLDIV and CHDIV bit descriptions. n) Added note in FLEX_US_FMR, FLEX_US_FLR, FLEX_US_FIMR, FLEX_SPI_SR, FLEX_SPI_FMR, FLEX_SPI_FLR, FLEX_TWI_FMR, FLEX_TWI_FLR, FLEX_TWI_FSR and FLEX_TWI_FMR.

18) Universal Asynchronous Receiver Transmitter (UART): a) UART_SR: changed title. b) UART_IMR: TXRDY description: typo fixed (Disable replaced with Mask).

19) Quad Serial Peripheral Interface (QSPI): a) Instruction Frame Transmission: updated all flowcharts. b) QSPI_MR: updated NBBITS field description.

20) Secure Digital MultiMedia Card Controller (SDMMC): a) SDMMC_CA0R: updated SLTYPE field description and updated note. b) SDMMC_AESR: updated ERRST field description. c) SDMMC_CA1R: updated note. d) SDMMC_NISTR (SD_SDIO): corrected CINT bit description. e) SDMMC_MCCAR: updated note

21) TC_EMRx: updated TRIGSRCB field description.

22) Pulse Width Modulation Controller (PWM): a) Updated Block Diagram. b) Block Diagram and Channel Block Diagram: removed all occurrences of APB. c) Updated Fault Protection. d) Comparator: updated formulae for duty cycle for left-aligned and center-aligned.

23) Secure Fuse Controller (SFC): a) Updated Description. b) Updated Fuse Functions. c) SFC_SR: index 16 now reserved.

24) Integrity Check Monitor (ICM): ICM_SR: updated reset value.

25) Advanced Encryption Standard (AES): a) Embedded Characteristics: added a bullet for new feature. b) Added Temporary Secured Storage for Keys. c) Updated 59.4.2 Operating Modes and added new detail on initialization vectors. d) AES_MR: in OPMOD description, added new detail on initialization vectors. e) AES_IVRx: added new detail on initialization vectors.

26) Secure Hash Algorithm (SHA): a) Updated: Description, Processing Period, Double Input Buffer b) SHA_IDATARx: renamed register from SHA Input Data x Register to SHA Input Data Register x

27) Triple Data Encryption Standard (TDES): a) 61.2 Embedded Characteristics: added bullet for new feature. b) Updated TDES_MR.LOD = 1. c) Added Temporary Secured Storage for Keys. d) TDES_CR: modified SWRST description (removed hardware) e) Corrected field description in TDES_KEYxWRy, TDES_IDATARx, TDES_ODATARx and TDES_IVRx.

28) True Random Number Generator (TRNG): Updated Description.

29) Analog-to-Digital Controller (ADC): a) Updated Last Channel Specific Measurement Trigger. b) Updated Sequence of Consecutive ADC Conversions with TRACKTIM = 15 c) Updated Sequence of Consecutive ADC Conversions with TRACKTIM = 0 d) Updated: ADC Block Diagram, I/O Lines, ADC Reference Voltage, Conversion Triggers, Input-output Transfer Functions, SWRST and START bit descriptions in ADC_CR, TRGMOD field description in ADC_TRGR e) ADC_CHSR: updated CHx bit description

30) Electrical Characteristics: a) DC Characteristics: updated VDDCORE/DC Supply Core. b) Added note to table PLLA Characteristics.

31) Product Identification System: Added SAMA5D26 and SAMA5D27.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 17 Feb 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

SAMA5D2 Series Datasheet

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Affected parts
SYST-14ASKF355
ATSAMA5D21B-CU
ATSAMA5D21B-CUR
ATSAMA5D21C-CU
ATSAMA5D21C-CUR
ATSAMA5D225C-D1M-CU
ATSAMA5D225C-D1M-CUR
ATSAMA5D22A-CU
ATSAMA5D22A-CUR
ATSAMA5D22B-CN
ATSAMA5D22B-CNR
ATSAMA5D22B-CU
ATSAMA5D22B-CUR
ATSAMA5D22C-CN
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ATSAMA5D24B-CU
ATSAMA5D24B-CUR
ATSAMA5D24C-CU
ATSAMA5D24C-CUF01
ATSAMA5D24C-CUR
ATSAMA5D24C-CURF01
ATSAMA5D26B-CN
ATSAMA5D26B-CNR
ATSAMA5D26B-CU
ATSAMA5D26B-CUR
ATSAMA5D26C-CN
ATSAMA5D26C-CNR
ATSAMA5D26C-CNR01
ATSAMA5D26C-CU
ATSAMA5D26C-CUR
ATSAMA5D27-SOM1
ATSAMA5D27-SOM1-EK1
ATSAMA5D27-WLSOM1
ATSAMA5D27A-CU

ATSAMA5D27A-CUR
ATSAMA5D27B-CN
ATSAMA5D27B-CNR
ATSAMA5D27B-CU
ATSAMA5D27B-CUR
ATSAMA5D27C-CN
ATSAMA5D27C-CNR
ATSAMA5D27C-CNRVAO
ATSAMA5D27C-CNVAO
ATSAMA5D27C-CU
ATSAMA5D27C-CUR
ATSAMA5D27C-D1G-CU
ATSAMA5D27C-D1G-CUR
ATSAMA5D27C-D5M-CU
ATSAMA5D27C-D5M-CUR
ATSAMA5D27C-LD1G-CU
ATSAMA5D27C-LD1G-CUR
ATSAMA5D27C-LD2G-CU
ATSAMA5D27C-LD2G-CUR
ATSAMA5D28A-CU
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ATSAMA5D28C-D1G-CU
ATSAMA5D28C-D1G-CUR
ATSAMA5D28C-LD1G-CU
ATSAMA5D28C-LD1G-CUR
ATSAMA5D28C-LD2G-CU
ATSAMA5D28C-LD2G-CUR
ATSAMA5D2C-XULT