Product Change Notification - SYST-03ZZQY339

Date:
04 Feb 2020

Product Category:
32-bit Microcontrollers

Affected CPNs:

📄 📊

Notification subject:

Data Sheet - SAM D21/DA1 Family Data Sheet

Notification text:
SYST-03ZZQY339
Microchip has released a new Product Documents for the SAM D21/DA1 Family Data Sheet of devices. If you are using one of these devices please read the document located at SAM D21/DA1 Family Data Sheet.

Notification Status: Final

Description of Change:

Section	Description
Block Diagram	Added arrow between PORT and AHB-APB BRIDGE B.
Pinout	Updated section titles
Product Mapping	Updated the diagram to show the Internal Flash.
PORT I/O Pin Controller	Corrected the WRCONFIG register to show the DRVSTR bit.
SERCOM	Under Clock Generation - Baud-Rate Generator, the table was updated with a new information and equations.
SERCOM USART	• Information regarding FIFO was removed as it is not supported on this device • The FIFOCLR bit was removed from the CTRLB register • The FIFOSPACE and FIFOPTR registers were removed
SERCOM SPI	• Information on FIFO was removed as it is not supported on this device • The FIFOCLR bit was removed from the CTRLB register • The FIFOSPACE and FIFOPTR registers were removed
SERCOM I2C	• Information on FIFO was removed as it is not supported on this device • The FIFOCLR bit was removed from the CTRLB Slave Register • Bit fields RXFF and TXFE were removed from the INTENCLR, INTENSET, and INTFLAG Slave Registers • The LENERR bit was removed from the STATUS Slave Register • Registers FIFOSPACE and FIFOPTR were removed from the Slave Registers • The FIFOCLR bit was removed from the CTRLB Master Register • Bit fields, RXFF and TXFE, were removed from the INTENCLR, INTENSET, and INTFLAG Master Registers • Registers FIFOSPACE and FIFOPTR were removed from the Master Registers

Timer Counter (TC)	• In Counter Mode, Count32 was updated with new TC numbering • The register summaries for 8-bit Mode, 16-bit Mode, and 32-bit Mode were updated to correctly display
TCC	• FCTRLA and FCTRLB had their naming corrected • In the WEXCTRL register the DTIEN bit had the numbering updated • In the DRVCTRL register the numbering was updated for the INVENx, NRVx, and NREx bits • In the EVCTRL register the numbering was updated for the MCEOx, MCEIx, TCEIx, and TCINVx Registers • In the INTENCLR, INTENSET, and INTFLAG registers the numbering was updated for the MCx bit • In the STATUS register the numbering was updated for the CMPx and FAULTx bits • The PATT register was updated to properly display the PGVx and PGEx bits • The PATTB register was updated to properly display the PGVBx and PGEBx bits
USB	Updated cross references.
ADC	Updated the MUXPOS Bit table in the INPUTCTRL register.
AC	• Updated the STARTx bit numbering in the CTRLB register • Updated the bit numbering for the COMPEIx, COMPEOx, and WINEOx bits in the EVCTRL register • Updated the bit numbering for the WINx, and COMPx bits in the INTENCLR, INTENSET, and INTFLAG registers • Updated the bit numbering for the WSTATEx and STATEx bits in the STATUSA register • Updated the bit numbering for the READYx bit in the STATUSB register • Updated the bit numbering for the WSTATEx and STATEx bits in the STATUSC register • Updated the bit numbering for the WINTSELx and WENx bits in the WINCTRL register
SAM DA1 Electrical Characteristics	This section was migrated into this data sheet from the original SAM DA1 data sheet.
Schematic Checklist	Updated External Reset Circuit with changes to the diagram External Reset Circuit Schematic.
Packaging Information	Updated Package Markings with a new marking diagram.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 04 Feb 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A
Attachment(s):
SAM D21/DA1 Family Data Sheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our PCN home page select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the PCN FAQ section.
If you wish to change your PCN profile, including opt out, please go to the PCN home page select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.