



Product Change Notification - SYST-08AXNW192

Date:

09 Dec 2019

Product Category:

32-bit Microcontrollers

Affected CPNs:



Notification subject:

ERRATA - SAM3S Family Silicon Errata and Data Sheet Clarifications

Notification text:

SYST-08AXNW192

Microchip has released a new Product Documents for the SAM3S Family Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at [SAM3S Family Silicon Errata and Data Sheet Clarifications](#).

Notification Status: Final

Description of Change:

1) This is the initial released version of this document.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 9 December 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

[SAM3S Family Silicon Errata and Data Sheet Clarifications](#)

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SAM3S Family

SAM3S Family Silicon Errata and Data Sheet Clarifications

SAM3S Series Errata

The SAM3S series family of devices that you have received conform functionally to the current device data sheets, *ATARM-SAM-3S4-3S2-3S1-Datasheet (6500F)* and *ATARM-SAM3S8-SAM3SD8-Datasheet (1190B)*, except for the anomalies described in this document.

Note: This document provides information on new errata issues for the SAM3S family of devices. Refer to the current device data sheet for all pre-existing silicon errata issues.

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1. Silicon Errata Summary

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Flash Memory	128-bit Read Access Mode	2.1.1	Default Flash 128-bit, Read Access mode is not supported with a Master Clock Frequency ≥ 60 MHz and $> 50^{\circ}\text{C}$.	X

2. Silicon Errata Issues

The following issues apply to the SAM3S family of devices.

2.1 Flash Memory

2.1.1 128-bit Read Access Mode Reference: M32DOC-1746

Default Flash 128-bit Read Access mode is not supported with a Master Clock Frequency ≥ 60 MHz and $> 50^{\circ}\text{C}$.

This errata effects only the following devices (Chip ID is provided for reference):

SAM3S4C (Revision A) 0x28A00960

SAM3S2C (Revision A) 0x28AA0760

SAM3S4B (Revision A) 0x28900960

SAM3S2B (Revision A) 0x289A0760

SAM3S4A (Revision A) 0x28800960

SAM3S2A (Revision A) 0x288A0760

SAM3S8B (Revision A) 0x289B0A60

SAM3S8C (Revision A) 0x28AB0A60

SAM3SD8B (Revision A) 0x299B0A60

SAM3SD8C (Revision A) 0x29AB0A60

Workaround:

Use the Flash in 64-bit Access Read mode by setting the Flash Access Mode (FAM) bit field of the EEFC Flash Mode Register (EEFC_FMR) to 0x1.

Table 2-1. Affected Silicon Revisions

A							
X							

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheets, (*ATARM-SAM-3S4-3S2-3S1-Datasheet* and *ATARM-SAM3S8-SAM3SD8-Datasheet*):

Note: Corrections in tables, registers, and texts are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no known Data Sheet Clarifications to report.

4. Revision History

Rev A Document 12/2019

This is the initial released version of this document.

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SYST-08AXNW192 - ERRATA - SAM3S Family Silicon Errata and Data Sheet Clarifications

Affected Catalog Part Numbers(CPN)

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ATSAM3S1AB-AUR
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ATSAM3S2BA-MU
ATSAM3S2BA-MUR
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ATSAM3S2CA-AUR
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ATSAM3S2CA-CUR
ATSAM3S4AA-AU
ATSAM3S4AA-AUR
ATSAM3S4AA-MU
ATSAM3S4AA-MUR
ATSAM3S4BA-AU
ATSAM3S4BA-AUR
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