Product Change Notification - SYST-24EBIU654

Date:

25 Oct 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:

Notification subject:

ERRATA - dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-24EBIU654

Microchip has released a new Product Documents for the dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:

1) Updated silicon issue 24 (I/O) and silicon issue 28 (PWM).
2) Removed silicon issue 27 (CPU) which stated that the upper byte of the destination register may not be persistent.
3) Updated reference to current Device Data Sheet revision (DS70005349G).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 25 Oct 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

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dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

The dsPIC33CK256MP508 family devices that you have received conform functionally to the current Device Data Sheet (DS70005349**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CK256MP508 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CK256MP508 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
dsPIC33CK256MP508 Family With CAN FD		
dsPIC33CK256MP508	0x7C74	0x0001
dsPIC33CK256MP506	0x7C73	
dsPIC33CK256MP505	0x7C72	
dsPIC33CK256MP503	0x7C71	
dsPIC33CK256MP502	0x7C70	
dsPIC33CK128MP508	0x7C64	
dsPIC33CK128MP506	0x7C63	
dsPIC33CK128MP505	0x7C62	
dsPIC33CK128MP503	0x7C61	
dsPIC33CK128MP502	0x7C60	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"dsPIC33CK256MP508 Family Flash Programming Specification"* (DS70005300) for detailed information on Device and Revision IDs for your specific device.

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TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]
		A1
dsPIC33CK256MP508 Family With CAN FD (Continued)		
dsPIC33CK64MP508	0x7C54	0x0001
dsPIC33CK64MP506	0x7C53	
dsPIC33CK64MP505	0x7C52	
dsPIC33CK64MP503	0x7C51	
dsPIC33CK64MP502	0x7C50	
dsPIC33CK32MP506	0x7C43	
dsPIC33CK32MP505	0x7C42	
dsPIC33CK32MP503	0x7C41	
dsPIC33CK32MP502	0x7C40	
dsPIC33CK256MP508 Family Without CAN FD		
dsPIC33CK256MP208	0x7C34	0x0001
dsPIC33CK256MP206	0x7C33	
dsPIC33CK256MP205	0x7C32	
dsPIC33CK256MP203	0x7C31	
dsPIC33CK256MP202	0x7C30	
dsPIC33CK128MP208	0x7C24	
dsPIC33CK128MP206	0x7C23	
dsPIC33CK128MP205	0x7C22	
dsPIC33CK128MP203	0x7C21	
dsPIC33CK128MP202	0x7C20	
dsPIC33CK64MP208	0x7C14	
dsPIC33CK64MP206	0x7C13	
dsPIC33CK64MP205	0x7C12	
dsPIC33CK64MP203	0x7C11	
dsPIC33CK64MP202	0x7C10	
dsPIC33CK32MP206	0x7C03	
dsPIC33CK32MP205	0x7C02	
dsPIC33CK32MP203	0x7C01	
dsPIC33CK32MP202	0x7C00	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

2: Refer to the *“dsPIC33CK256MP508 Family Flash Programming Specification”* (DS70005300) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A1
I²C	Interrupt	1.	In Slave mode, incorrect interrupt is generated when DHEN = 1.	X
I²C	Error	2.	Bus collision error cannot be cleared.	X
I²C	Error	3.	False bus collision error generated.	X
I²C	Idle	4.	Address cannot be received in Idle mode.	X
Oscillator	PLL	5.	FRCDIVN drives the PLL instead of the FRC.	X
Oscillator	HS,XT	6.	The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early.	X
PWM	Dead Time	7.	When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.	X
UART	OERR	8.	The OERR bit cannot be cleared by software.	X
UART	FERR	9.	The FERR bit will not get set if one Stop bit is received.	X
UART	OERR	10.	The 9th byte received will not be available to be read.	X
UART	TRMT	11.	The TRMT bit takes time to set on the last transmit completion.	X
UART	TRMT	12.	The TRMT bit is unreliable when there is back-to-back Break character transmission.	X
UART	Idle	13.	The RIDLE bit takes one instruction cycle to get cleared after ABAUD is set.	X
UART	TXWRE	14.	The TXWRE bit (UxSTAH[7]) cannot be cleared once it gets set.	X
UART	Address Detect	15.	When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted.	X
UART	Address Detect	16.	In Address Detect mode, the content of P1 is not transmitted on writing to P1 with UTXBRK = 1.	X
UART	Sleep	17.	When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.	X
UART	Smart Card	18.	The Wait Time Counter Interrupt Flag (WTCIF) is set when the last character transmitted has the bit, LAST = 0.	X
UART	XOFF	19.	XOFF is transmitted when one empty space remains in the RX buffer.	X
MBIST	MBISTDONE	20.	After executing a Reset, the MBISTDONE bit will always be set.	X
CPU	FLIM Instruction	21.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X
SCCP/ MCCP	Clock source	22.	Using FOSC as the clock source may cause synchronization issues.	X
I²C	SMBus 3.0	23.	When Configuration bit, SMBEN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X
I/O	POR	24.	Spike on I/O at POR.	X
CPU	DIV.SD Instruction	25.	Overflow bit is not getting set when an overflow occurs.	X
CPU	MAXAB/MINAB/ MINZAB Instructions	26.	MAXAB, MINAB and MINZAB do not work for different sign operands.	X
DMA	ADC Triggers	27.	DMA is triggered continuously from ADC.	X
PWM	Time Base Capture	28.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A1**).

1. Module: I²C

In Slave mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Slave interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Slave interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

A1							
X							

2. Module: I²C

In Slave mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

A1							
X							

3. Module: I²C

In Slave mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1) and a Stop bit is received.

Work around

Ignore the bus collision. Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

A1							
X							

4. Module: I²C

In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A1							
X							

5. Module: Oscillator

When using the 8 MHz internal FRC Oscillator with Primary PLL as either a system clock or a peripheral source, FRCDIVN drives the PLL instead of the FRC.

This means that the PLL FRC input selection is subject to the FRCDIV[2:0] bits and could lead to a condition where the minimum PLL input requirement of 8 MHz is not maintained.

Work around

Ensure FRCDIV[2:0] bits are maintained as zero when using FRCPLL as either a system clock or a peripheral source.

Affected Silicon Revisions

A1							
X							

6. Module: Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Then, switch to the POSC source.

Affected Silicon Revisions

A1							
X							

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7. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

Work around

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

Affected Silicon Revisions

A1							
X							

8. Module: UART

Once the UART receive buffer overflows and the OERR bit (UxSTA[1]) is set, the OERR bit cannot be cleared by software.

Work around

1. Make sure that the receive buffer never overflows. Do not let the OERR bit get set by reading the received data byte on each byte reception.
2. Disable and enable UART before clearing the OERR bit.

Affected Silicon Revisions

A1							
X							

9. Module: UART

When the UART is operating with STSEL[1:0] = 2 (two Stop bits sent, two checked at receive), the FERR bit will not get set if one Stop bit is received.

Work around

3. Use STSELx = 3 instead of STSELx = 2. When operating with STSELx = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

A1							
X							

10. Module: UART

When the receive buffer overflows, the 9th byte received will get lost and cannot be read.

Work around

Do not allow the OERR bit to get set by reading the received data byte on each byte reception.

Affected Silicon Revisions

A1							
X							

11. Module: UART

At low BRG value, the TRMT bit takes time to set on the last transmit completion, which may result in the transmitted data getting lost.

Work around

1. Use the UTXBE bit to monitor for the next transmit.
2. Provide a delay to stabilize the POSC.

Affected Silicon Revisions

A1							
X							

12. Module: UART

The Transmit Shifter Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.

Work around

Poll the UART Transmit Break bit, UTXBRK (UxMODE[8]), to be cleared instead of the TRMT bit.

Affected Silicon Revisions

A1							
X							

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13. Module: UART

During the UART Auto-Baud Detection sequence, the RIDLE bit takes one instruction cycle to get cleared after ABAUD is set.

Work around

Ignore the RIDLE bit until the Auto-Baud Detection sequence is complete.

Affected Silicon Revisions

A1							
X							

14. Module: UART

Once the TX Write Transmit Error Status bit, TXWRE (UxSTAH[7]), gets set, the TXWRE cannot be cleared by a single clear instruction.

Work around

Use multiple clear instructions in a loop until the TXWRE bit gets cleared.

Affected Silicon Revisions

A1							
X							

15. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

A1							
X							

16. Module: UART

In Address Detect mode, the content of P1 is not transmitted on writing to P1 with UTXBRK = 1.

Work around

Write P1 a second time after waiting for the Break transmission to start.

Affected Silicon Revisions

A1							
X							

17. Module: UART

When waking from Sleep with a UART reception, SLPEN needs to be set in addition to WAKE = 1.

Work around

Set the SPLEN bit in addition to WAKE before entering Sleep.

Affected Silicon Revisions

A1							
X							

18. Module: UART

In Smart Card T = 1 mode, the Wait Time Counter Interrupt Flag (WTCIF) is set when the last character transmitted has the bit, LAST = 0.

Work around

Ignore WTC interrupt events on non-last bytes.

Affected Silicon Revisions

A1							
X							

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19. Module: UART

In Software Flow Control mode, XOFF is transmitted when one empty space remains in the RX buffer. XOFF transmission can get further delayed if the transmitter has already been loaded, resulting in XOFF transmission on a receive buffer full event.

Work around 1

Give a minimum one-byte delay before each byte transmission.

Work around 2

Use the UART RX interrupt with URXISEL[2:0] set to at least two empty slots. This allows the RX buffer to be read in time to prevent RX buffer overflow.

Affected Silicon Revisions

A1							
X							

20. Module: MBIST

After a Reset, the MBISTDONE status bit will be set regardless of a BIST test being executed. If a BIST is requested and executed, the MBISTDONE bit will be set as expected.

Work around

None.

Affected Silicon Revisions

A1							
X							

21. Module: CPU

The `FLIM` instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

A1							
X							

22. Module: SCCP/MCCP

When Fosc is selected as the clock source using the CLKSEL[2:0] bits (CCPxCON1L[10:8]), unexpected operation may occur. For proper SCCP/MCCP input clock synchronization, do not use Fosc as the system clock source.

Work around

Use any of the other available clock sources in CLKSEL[2:0].

Affected Silicon Revisions

A1							
X							

23. Module: I^2C

When selecting SMBus 3.0 operation using Configuration bit, SMBEN (FDEVOPT[10]), the Voltage Input High (V_{IH}) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

Affected Silicon Revisions

A1							
X							

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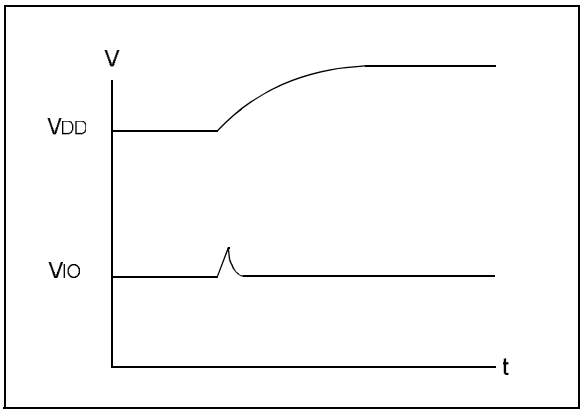
24. Module: I/O

During a fast device power-up when the VDD ramp is less than 4 mS, the I/O pins may drive up to 100 µA current for a duration of up to 10 µS (Figure 1-1).

FIGURE 1-1: I/O RAMP



Work around

1. Slow down the VDD ramp time (greater than 4 mS for VDD to ramp 0V to 3.3V).
2. Ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur. High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® device to avoid the current shoot-through. This behavior is specific to each device and not affected by aging.

Affected Silicon Revisions

A1							
X							

25. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `DIV.SD`, the Overflow bit may not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A1							
X							

26. Module: CPU

When operating on signed operands of different sign values, the output for `MAXAB`, `MINAB` and `MINZAB` instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

A1							
X							

27. Module: DMA

The DMA receives multiple continuous triggers from the ADC until the trigger event from the ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state from '0' to '1', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source (ANxRDY) with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

A1							
X							

28. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status Flag, CAP, will not set again.

Work around

Read the PWM Generator Capture (PGxCAP, x = 1 to 8) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using PWM Generator x (1-8) interrupt or any of the six PWM Event (A-F) interrupts corresponding to the PCI event which triggered the time base capture. Read the PGxCAP value after the CAP bit has set within the interrupt.

Affected Silicon Revisions

A1							
X							

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005349**G**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2018)

Initial release of this document; issued for revision A1.

Rev B Document (9/2018)

Added silicon issues 21 (CPU), 22 (SCCP/MCCP) and 23 (I^2C).

Rev C Document (12/2018)

Added silicon issues 24 (I/O), 25 (CPU), 26 (CPU) and 27 (CPU).

Rev D Document (3/2019)

Added silicon issues 28 (DMA) and 29 (PWM).

Updated reference to current Device Data Sheet revision (DS70005349**F**).

Rev E Document (10/2019)

Updated silicon issue 24 (I/O) and silicon issue 28 (PWM).

Removed silicon issue 27 (CPU) which stated that the upper byte of the destination register may not be persistent.

Updated reference to current Device Data Sheet revision (DS70005349**G**).

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China - Xian
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China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
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SYST-24EBIU654 - ERRATA - dsPIC33CK256MP508 Family Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

DSPIC33CK128MP202-E/2N
DSPIC33CK128MP202-E/SS
DSPIC33CK128MP202-H/2N
DSPIC33CK128MP202-H/SS
DSPIC33CK128MP202-I/2N
DSPIC33CK128MP202-I/SS
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