Cypress Semiconductor Corporation, 198 Champion Court San Jose, CA 95134. Tel: (408) 943-2600

PRODUCT CHANGE NOTIFICATION

PCN: PCN193806 **Date:** September 17, 2019

Subject: Qualification of UMC as an Alternate Wafer Fab Site for Select 16Mb MoBL SRAM Products

To: FUTURE ELECTRONICS
FUTURE ELE
pcn.system@futureelectronics.com

Change Type: Major

Description of Change:
Cypress announces the qualification of UMC's 65nm (No. 3, Li-Hsin 2nd Rd., Hsinchu Science Park, Hsinchu, Taiwan, R.O.C.) as an alternate wafer fab site for select 16Mb Async MoBL SRAM products. The 65nm product is form, fit and function compatible with the 90nm 16Mb Async MoBL SRAM products manufactured at Skywater, Minnesota. There will be no change to the existing marketing part numbers.

Benefit of Change:
Qualification of alternate manufacturing sites and technologies is part of Cypress' ongoing flexible manufacturing initiative. The goal of the flexible manufacturing initiative is to provide the means for Cypress to continue to meet delivery commitments through dynamic, changing market conditions.

Affected Part Numbers: 8
See the attached 'Affected Parts List' file for a list of all part numbers affected by this change. Note that any new parts that are introduced after the publication of this PCN will include all changes outlined in this PCN.

Qualification Status:
LL65 (65nm) technology at UMC was previously qualified through a series of tests identified in the QTP#124902. The new product has been qualified through a series of tests identified in the Qualification Test Plan QTP#181403. The QTP report can be found as attachments to this notification or by visiting www.cypress.com, typing the QTP number in the keyword search window.

Sample Status:
Qualification samples may not be built ahead of time for all part numbers affected by this change. Please review the attached 'Affected Parts List' file for a list of affected part numbers

with their associated UMC sample ordering part numbers. Samples are available now unless there is an indication that the sample ordering part numbers are subject to lead times. If you require qualification samples, please contact your local Cypress sales representative as soon as possible, preferably within 30 days of the date of this PCN, to place any sample orders.

Approximate Implementation Date:
Effective 90 days from the date of this notification, all shipments of the affected part numbers will be fabricated at either SkyWater or UMC.

Anticipated Impact:
Products fabricated at UMC are completely compatible with the existing product from a form, fit, function, quality, performance and parametric perspectives.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration

Cypress Semiconductor Corporation
CY62167EV30 Characterization Report

16-Mbit (1 M words × 16 bit) Static RAM

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1.0 Table of Contents

2.0 Introduction

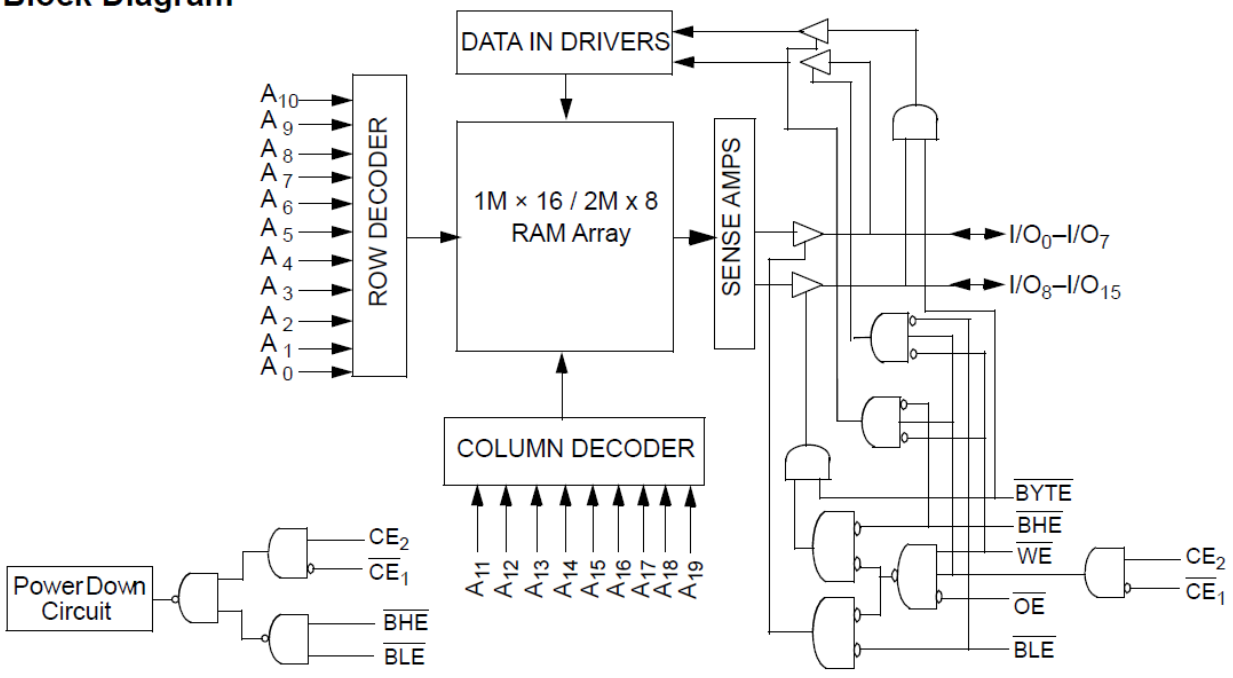
2.1 General Description

The CY62167EV30 is a high-performance CMOS static RAM organized as 1M words by 16 bits or 2M words by 8 bits. This device features an advanced circuit design that provides an ultralow active current. Ultralow active current is ideal for providing More Battery Life in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device in standby mode when deselected (CE1 HIGH or CE2 LOW or both BHE and BLE are HIGH). The input and output pins (I/O0 through I/O15) are placed in a high-impedance state when: the device is deselected (CE1 HIGH or CE2 LOW), outputs are disabled (OE HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is in progress (CE1 LOW, CE2 HIGH and WE LOW).

To write to the device, take Chip Enables (CE1 LOW and CE2 HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O0 through I/O7) is written into the location specified on the address pins (A0 through A19). If Byte High Enable (BHE) is LOW, then data from the I/O pins (I/O8 through I/O15) is written into the location specified on the address pins (A0 through A19).

To read from the device, take Chip Enables (CE1 LOW and CE2 HIGH) and Output Enable (OE) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O0 to I/O7. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O8 to I/O15.

Logic Block Diagram



Pin Configuration

Figure 1. 48-ball VFBGA Pinout (Top View) [1, 2]

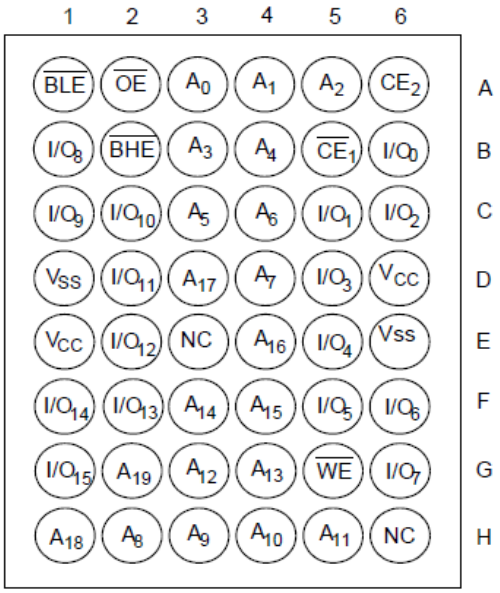
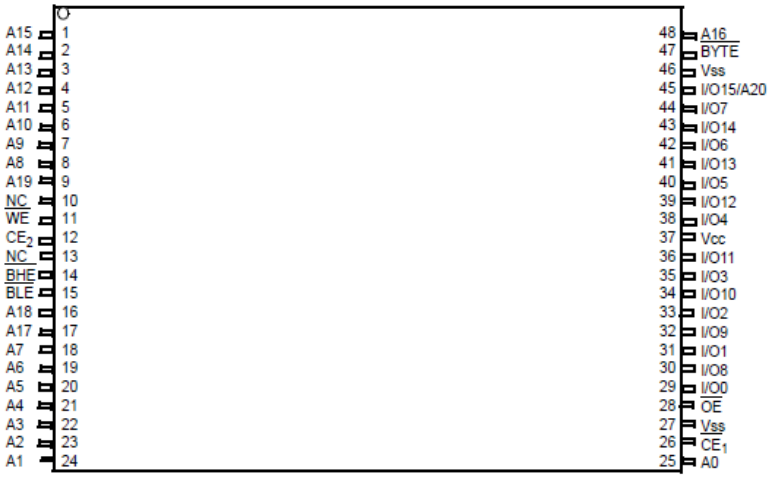


Figure 2. 48-pin TSOP I Pinout (Top View) [2, 3]



2.2 Datasheet

The *CY62167EV30* meets all datasheet specifications. The datasheet is available from the Cypress Website at:

CY62167EV30 Datasheet

2.3 Application Notes

The *CY62167EV30* has not associated Application Notes at this time.

2.4 White Papers

The *CY62167EV30* has no associated White Papers at this time.

2.5 Qualification Report

The *CY62167EV30* is qualified under QTP 181403.

3.0 Characterization Hardware and Setup

3.1 Measurement System and Hardware

The following equipments and hard wares are used for the DC and AC parametric characterization of this device.

3.1.1 Characterization Board

All the DC parameters and the AC parameters were measured using 48TSOP1 package with the D1054 hand test interface board connected to L042 load board. Pin capacitance was measured using the probe card type board.

3.1.2 ATE

Advantest 5581P tester was used for the DC and AC parameter characterization.

3.1.3 Temperature Forcing System

Temptronics TP04310A Precision Temperature Forcing System was used to force ambient temperature.

3.1.4 Frequency LCR Meter

HP4284A LCR Meter was used to measure input and output pin capacitance.

3.1.5 Power Supply

The Kiethley 2400 Source Meter was used to supply power for device for pin capacitance measurement.

3.2 Characterization Conditions and Parameters

Characterization was done on the following device and conditions as listed in Table 1. Units used for characterization are quick builds and chosen randomly unless specified.

Table 1. Characterization Conditions and Parameters

Parameter	Device	Fab Lot	Assy Lot	# of Devices	Voltage Variation (V)	Temperature Variation (°C)
DC & AC	CY62167EV30-45ZXI	9851013	NA (wafer level char)	60	2.1V-3.7V	-40, 25, 85

The part which was originally in 90nm at Skywater fab is now qualified for 65nm technology at UMC's fab in Taiwan. The tables below show the comparison of characterization results between the 90nm technology and 65nm technology.

4.0 DC Characterization

4.1 DC Characterization Summary over V_{DD} and Temperature

Table 2. DC Characterization Results across V_{DD} and Temperature

Parameter	Description		Test Conditions		Datasheet (45ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
					Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V_{OH}	Output HIGH voltage	2.2V to 2.7V	VCC = Min, IOH = –1.0 mA		2.0	-	-	2.162	2.165	2.172	2.150	2.170	2.180	V
		2.7V to 3.6V	VCC = Min, IOH = –1.0 mA		2.4	-	-	2.588	2.596	2.602	2.580	2.600	2.630	
V_{OL}	Output LOW voltage	2.2V to 2.7V	VCC = Min, IOL = 0.1 mA		-	-	0.4	0.080	0.011	0.014	0.010	0.015	0.022	V
		2.7V to 3.6V	VCC = Min, IOL = 2.1 mA		-	-	0.4	0.09	0.112	0.136	0. 096	0.122	0.140	
V_{IH}	Input HIGH voltage	2.2V to 2.7V			1.8	-	VCC + 0.3	1.176	1.208	1.234	1.600	1.630	1.650	V
		2.7V to 3.6V			2.0	-	VCC + 0.3	1.404	1.464	1.520	1.600	1.630	1.650	
V_{IL}	Input LOW voltage	2.2V to 2.7V			-0.3	-	0.6	0.820	0.836	0.856	0.890	0.940	1.010	V
		2.7V to 3.6V			-0.3	-	0.7	0.926	0.949	0.962	1.110	1.150	1.210	
I_{IX}	Input leakage current		GND < VIN < VCC		-1.0	-	1.0	-0.020	0.072	0.100	-0.040	0.020	0.140	uA
I_{OZ}	Output leakage current		GND < VOUT < VCC, Output disabled		-1.0	-	1.0	-0.020	0.028	0.040	-0.040	0.24	0.040	uA
I_{CC}	Operating supply current		VCC = Max, IOUT = 0 mA, CMOS levels	f = 22.22 MHz (45ns)	-	29.0	35	21.36	22.33	23.80	26.40	27.99	29.60	mA
				f = 1 MHz	-	7.0	9.00	2.28	2.36	2.47	3.28	3.81	4.52	
I_{sb1}	Automatic Power-down Current – CMOS Inputs; VCC = 2.2 V to 3.6 V		CE1 > VCC – 0.2 V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V, VIN < 0.2 V, f = fmax (address and data only), f = 0 (OE, and WE), VCC = VCC(max)		-	1.5	12	2.50	3.79	5.70	4.14	5.67	7.28	uA
I_{sb2}	Current – CMOS Inputs VCC = 2.2 V to 3.6 V		CE1 > VCC – 0.2V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC – 0.2 V or VIN < 0.2 V, f = 0, VCC = VCC(max)		-	1.5	12	2.88	4.12	5.88	5.94	6.74	7.80	uA

Capacitance

Parameter	Description	Test Conditions	Datasheet	90nm Skywater fab (current)	65nm UMC fab (New)	Unit
C_{IN}	Input capacitance	TA = 25 °C, f = 1 MHz, VCC = VCC(typ)	10	7.80	7.80	pF
C_{OUT}	Output capacitance		10	6.80	6.80	pF

Data Retention Characteristics

Parameter	Description	Test Conditions	Datasheet (45ns)			90nm Skywater fab (current)			65nm UMC fab (New)			Unit
			Min	Typ	Max	Min	Mean	Max	Min	Mean	Max	
V_{DR}	VCC for data retention		1.0	-	-	Pass	-	-	Pass	-	-	V
I_{CCDR}	Data retention current	1.5 V < VCC < 3.0 V, CE1 > VCC-0.2 V or CE2 < 0.2 V or (BHE and BLE) > VCC – 0.2 V, VIN > VCC-0.2 V or VIN < 0.2 V	-	-	10	2.96	3.57	4.26	6.96	7.86	9.24	V
t_{CDR}	Chip deselect to data retention time		0	-	-	Pass	-	-	Pass	-	-	V
t_R	Operation recovery time	VCC > 2.2 V	45	-	-	pass	-	-	Pass	-	-	ns

5.0 AC Characterization

5.1 AC Characterization Summary over V_{DD} and Temperature

Table 3. AC Characterization Results across V_{DD} (2.2V-3.6V) and Temperature

Parameter	Description	Datasheet (45ns)		90nm Skywater fab (current)			65nm UMC fab (New)			
		Min	Max	Min	Mean	Max	Min	Mean	Max	Unit
Read Cycle										
t_{RC}	Read cycle time	45.0	-	Pass	-	-	Pass	-	-	ns
t_{AA}	Address to data valid	-	45.0	33.31	34.15	35.06	17.95	19.14	20.85	ns
t_{OHA}	Data hold from address change	10.0		12.00	13.02	13.69	15.94	16.33	16.60	ns
t_{ACE}	CEB LOW to data valid	-	45.0	33.31	34.07	35.00	34.83	36.73	38.55	ns
t_{DOE}	OEB LOW to data valid	-	22.0	8.56	9.33	10.25	7.46	7.74	8.06	ns
t_{LZOE}	OEB LOW to low-Z	5	-	7.33	7.57	7.69	7.65	7.74	7.75	ns
t_{HZOE}	OEB HIGH to high-Z	-	18.0	6.33	6.58	6.69	5.73	5.87	5.93	ns
t_{LZCE}	CEB LOW to low-Z	10.0	-	27.10	27.50	27.82	27.75	27.82	27.90	ns
t_{HZCE}	CEB LOW to low-Z	-	18.0	7.74	7.83	7.94	6.03	6.15	6.28	ns
t_{PU}	CEB LOW to power-up	0	-	pass	-	-	pass	-	-	ns
t_{pd}	CEB HIGH to power-down	-	45.0	-	-	pass	-	-	pass	ns
t_{DBE}	Byte enable to data valid	-	45.0	31.56	32.12	33.12	35.35	37.59	39.40	ns
t_{LZBE}	Byte enable to low-Z	5	-	27.50	27.92	28.28	27.18	28.09	28.23	ns
t_{HZBE}	Byte disable to high-Z	-	18.0	6.85	6.97	7.10	6.03	6.10	6.18	ns

Parameter	Description	Datasheet (45ns)		90nm Skywater fab (current)			65nm UMC fab (New)			
		Min	Max	Min	Mean	Max	Min	Mean	Max	Unit
Write Cycle										
t_{WC}	Write cycle time	45.0	-	pass	-	-	pass	-	-	ns
t_{SCE}	CE LOW to write end	-	35.0	17.94	19.64	20.75	29.42	30.64	31.99	ns
t_{AW}	Address setup to write end	-	35.0	18.00	20.39	21.50	31.34	32.71	34.12	ns
t_{HA}	Address hold from write end	0	-	-7.19	-6.76	-6.12	-14.38	-13.77	-13.18	ns
t_{SA}	Address setup to write start	0	-	-8.56	-8.12	-7.50	-9.52	-8.98	-8.48	ns
t_{PWE}	WE pulse width	-	35.0	15.44	16.10	16.87	8.04	8.35	8.86	ns
t_{BW}	Byte Enable to write end	-	35.0	19.38	19.78	20.63	31.39	32.54	32.67	ns
t_{SD}	Data setup to write end	-	25.0	14.31	14.59	15.06	7.27	7.62	7.98	ns
t_{HD}	Data hold from write end	0	-	-6.75	-6.48	-5.86	-3.34	-3.15	-2.84	ns
t_{HZWE}	WE LOW to high-Z	-	18.0	6.19	6.21	6.23	6.20	6.22	6.24	ns
t_{LZWE}	WE HIGH to low-Z	10.0	-	15.60	15.80	15.95	15.85	15.93	15.89	ns

Document History Page

Rev.	ECN No.	Orig. of Change	Description of Change
**	6588482	ARAV	New Characterization Report

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Cypress Semiconductor
Product Qualification Report

QTP# 181403 VERSION**
June 2019

16-MBIT Ultra Low Power Asynchronous SRAM Family, ULP65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	
CY62167G30*	**16-MBIT (1M WORDS X 16 BITS / 2M WORDS X 8 BITS) STATIC RAM WITH ERROR-CORRECTING CODE (ECC), 3V W/ AND W/O ERR PIN (AMAZON EQUIVALENT)**
CY62168G30*	**16-MBIT (2M WORDS X 8 BITS) STATIC RAM WITH ERROR-CORRECTING CODE (ECC), 3V W/ AND W/O ERR PIN (AMAZON EQUIVALENT)**
CY62162G30*	**16-MBIT (512K WORDS X 32 BITS) STATIC RAM WITH ERROR-CORRECTING CODE (ECC), 3V W/ AND W/O ERR PIN (AMAZON EQUIVALENT)**
CY62167EV30LL*	**INDUSTRIAL MoBL® 16-MBIT (1M WORDS X 16 BITS / 2M WORDS X 8 BITS) STATIC RAM (R95 EQUIVALENT)**
CY62168EV30LL*	**INDUSTRIAL MoBL® 16-MBIT (2M WORDS X 8 BITS) STATIC RAM (R95 EQUIVALENT)**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	Aug. 2009
124902	Qualification of 16-MBIT Asynchronous SRAM Family, ULL65nm (LL65UP-25ODR) Technology at UMC Fab 12A	Aug. 2014
144804	Qualification of 16-MBIT Asynchronous SRAM Family Rev.*D Silicon, ULL65nm (LL65UP-25ODR) Technology at UMC Fab 12A	Feb. 2015
181403	Qualification of 16-MBIT Ultra Low Power Asynchronous SRAM Family, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A	June 2019

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify 16-MBIT Ultra Low Power Asynchronous SRAM Family, ULL65nm (LL65UMP-25ODR) Technology at UMC Fab 12A
Marketing Part #:	CY62167G30* / CY62168G30* / CY62162G30* / CY62167EV30LL* / CY62168EV30LL*
Device Description:	16-MBIT Ultra Low Power Asynchronous SRAM Family
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65UMP-25ODR			
Number of Metal Layers:	Proprietary	Metal Composition:	Proprietary
Passivation Type and Materials:		Proprietary	
Number of Transistors in Device		Proprietary	
Number of Logic Gates in Device		Proprietary	
Generic Process Technology/Design Rule (µ-drawn):		Proprietary	
Gate Oxide Material/Thickness (MOS):		Proprietary	
Name/Location of Die Fab (prime) Facility:		UMC Fab 12A	
Die Fab Line ID/Wafer Process ID:		L65LL	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY	QTP REFERENCE
48-Ball VFBGA	Bangkok-Taiwan (SB)	QTP# 152202 / 164305
48L TSOP I	Bangkok-Taiwan (SB)	QTP# 171001

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BZ48A
Package Outline, Type, or Name:	VFBGA (Very Fine Ball Grid Array)
Mold Compound Name/Manufacturer:	KMC-3580LVA/ SHINETSU
Mold Compound Flammability Rating:	V-0 / UL94
Oxygen Rating Index:	> 40%
Substrate Material:	Substrate Cu/BT
Lead Finish, Composition / Thickness:	Sn/Ag/Cu (SAC-105)
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI 546
Bond Diagram Designation:	002-24833
Wire Bond Method:	Thermosonic
Wire Material/Size:	CuPdAu, 0.8 mil (20um)
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-97055
Name/Location of Assembly (prime) facility:	BKK-Thailand (SB)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML - R

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Constructional Analysis	Criteria: Meet external and internal characteristics of Cypress package	P
Dynamic Latch-up	125°C , 8.25V JESD78	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V/1,000V/1,250V JESD22-C101	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V/2,200V/3,300V JESD22-A114	P
Electrostatic Discharge Machine Model (ESD-MM)	200V JESD22-A115	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V 110°C/130°C, 85%RH, 3.65V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 1.37/2.25V, 150°C JESD22-A108	P
High Temperature Storage	JESD22-A103:150°C No bias	P
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 1.44V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 1.44V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core, 1.45V,External 2.05V,125°C /150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 1.62V/2.25V, -30°C JESD22-A108	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at 0 hour/500/1000hrs	P
Static Latch-up	125°C , ± /100mA/140mA, 85°C , ± 140mA/200mA JESD78	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C/ 85% RH , 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron)	JESD89	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life[1] Early Failure Rate	1,636 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[2] Long Term Failure Rate (150°C)	89,000 DHRs	0	0.7	170	13 FIT
High Temperature Operating Life[2] Long Term Failure Rate (125°C)	1,009,840 DHRs	0	0.7	55	

[1]Early Failure Rate was computed from QTP# 181403

[2] Long Term Failure Rate was computed from QTP# 091706 and QTP# 124902 Data

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEMP, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	15	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	170	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	3	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	3	0	
STRESS: CONSTRUCTIONAL ANALYSIS							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	COMP	5	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	5	0	
STRESS: DYNAMIC LATCH-UP TESTING, 125C, 8.25V							
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	500	9	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1000	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1250	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	500	9	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1250	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	500	9	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1000	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1250	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	500	9	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1000	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1250	3	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	500	9	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	750	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	500	9	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1000	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	1100	3	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	2200	8	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	3300	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	1100	3	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	2200	8	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	3300	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	1100	3	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	2200	8	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	3300	3	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	1100	3	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	2200	8	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	3300	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	1100	3	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	2200	8	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	3300	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1100	3	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	2200	8	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	3300	3	0	
STRESS: HI-ACCEL SATURATION TEST, 110C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	264	30	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	128	79	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE – REG-ON, 125C, 6.0V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	96	50	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	96	50	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	96	2107	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	96	1818	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	168	179	0	
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	1000	175	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	168	180	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	1000	180	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	168	179	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	178	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 1.37V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	168	80	0	
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	168	80	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	500	79	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	1000	79	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 1.62V							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	500	83	0	
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9312001	611414530	CML-RA	1000	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	1000	10+2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	0	10+2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	1000	10+2	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRE/POST LTOL CRITICAL PARAMETERS							
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	0	10+2	0	
CY7C1061G30 (7CC171061A)	9313001	611333269	CML-RA	500	10+2	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	168	79	0	
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	288	79	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	168	78	0	
CY7C1061G30 (7CC171061A)	9313001	611333088	CML-RA	288	78	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V/9.1V, +/-140mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	6	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	6	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	6	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	6	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	6	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	6	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V/9.1V, +/-140mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	2	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	2	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V/9.1V, +/-180mA							
CY7C1062G30 (7CC171062A)	9302002	611321701	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9302002	611320002	G-TAIWAN	COMP	2	0	
CY7C1069G30 (7CC171069A)	9302002	611320107	G-TAIWAN	COMP	2	0	
CY7C1061GE30(7CC1710613A)	9308001	611340082	G-TAIWAN	COMP	2	0	
CY7C1061G30 (7CC171061A)	9312001	611328720	CML-RA	COMP	2	0	
CY7C1061G30 (7CC171061A)	9324001	611342911	G-TAIWAN	COMP	2	0	

Reliability Test Data

QTP #: 124902

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE SEL, 25C/85C/120C, 1.65V/3.3V/5.5V							
7C1710614GE	0	0	UMC	COMP	3	0	
STRESS: SER – NEUTRON SEL, 85C/125C, 5.25V							
7C17165A	0	0	UMC	COMP	3	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348183	CML-RA	1000	79	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348182	CML-RA	1000	78	0	
CY7C1061G30 (7CP1710612A)	9313001	611420263	CML-RA	500	80	0	
CY7C1061G30 (7CP1710612A)	9313001	611420263	CML-RA	1000	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	500	80	0	
CY7C1061G30 (7CC171061A)	9313001	611348184	CML-RA	1000	80	0	
STRESS: X-SECTION/STEM XY AUDIT							
7C17165A	9302002	0	UMC	COMP	1WF	0	

Reliability Test Data

QTP #: 144804

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	500	9	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1000	3	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	1100	3	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	2200	8	0	
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	3300	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	96	927	0	
CY62167G30 (7CC172167A)	9438001	611503292	G-Taiwan	96	695	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 8.25V, +/-140mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 9.1V, +/-200mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.25V, +/-140mA							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	3	0	
YIELD: CLASS							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		
YIELD: E-TEST							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		
YIELD: SORT							
CY62167GE30 (7CC1721673A)	9423005	611500929	CML-RA	COMP	EQUIVALENT		

Reliability Test Data

QTP #: 181403

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1061G (7CP171061AO)	9537003	611624393	SB-Thailand	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE , 125C, 1.44V							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	48	1636	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.44V							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1000	120	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157EV30LL (7CP62157FC)	4501549	RFB2171	SB-Thailand	168	80	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1061G (7CP171061AO)	9537003	611624393	SB-Thailand	500	80	0	
CY7C1061G (7CP171061AO)	9537003	611624393	SB-Thailand	1000	80	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	500	9	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1000	3	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1250	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	1100	3	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	2200	8	0	
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	3300	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, +/-100mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.94V, +/-140mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-140mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	2	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-200mA							
CY62167EV30LL (7CP182167A)	9851013	611908715	SB-Thailand	COMP	2	0	

Document History Page

Document Title: QTP# 181403: 16-MBIT Ultra Low Power Asynchronous SRAM Family, ULP65nm (LL65UMP-25ODR) Technology at UMC Fab 12A
Document Number: 002-27556

Rev.	ECN No.	Orig. of Change	Description of Change
**	6591691	JYF	Initial spec release.

Marketing Part Number	Sample Order Part Number	Sample Availability
CY62167EV30LL-45BVXI	CY62167EV30LL9-45BVXI	Available
CY62167EV30LL-45BVXIT	CY62167EV30LL9-45BVXI	Available
CY62167EV30LL-45 XI	CY62167EV30LL9-45 XI	Available
CY62167EV30LL-45 XIT	CY62167EV30LL9-45 XI	Available
CY62168EV30LL-45BVXI	CY62168EV30LL9-45BVXI	Subject to leadtime
CY62168EV30LL-45BVXIT	CY62168EV30LL9-45BVXI	Subject to leadtime
CG7424AF	CG7424 F	Subject to leadtime
CG7424AFT	CG7424 F	Subject to leadtime