Product Change Notification - SYST-10GTDD251

Date:

14 May 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:

Notification subject:

ERRATA - dsPIC33EVXXXGM00X/10X Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-10GTDD251

Microchip has released a new DeviceDoc for the dsPIC33EVXXXGM00X/10X Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33EVXXXGM00X/10X Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: 1) Adds silicon revision AE. 2) Removes all Data Sheet Clarifications as they were addressed in the new revision of the data sheet.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 06 June 2019
NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachment(s):

dsPIC33EVXXXGM00X/10X Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33EV128GM102-E/WMV01
DSPIC33EV128GM002-E/MM
DSPIC33EV128GM102-E/MM
DSPIC33EV64GM002-E/MM
DSPIC33EV64GM102-E/MM
DSPIC33EV32GM002-E/MM
DSPIC33EV32GM102-E/MM
DSPIC33EV128GM102-E/MMVAO
DSPIC33EV64GM002-E/MMVAO
DSPIC33EV32GM002-E/MMVAO
DSPIC33EV128GM002-E/SP
DSPIC33EV128GM102-E/SP
DSPIC33EV64GM002-E/SP
DSPIC33EV64GM102-E/SP
DSPIC33EV32GM002-E/SP
DSPIC33EV32GM102-E/SP
DSPIC33EV128GM002-E/SS
DSPIC33EV128GM102-E/SS
DSPIC33EV64GM002-E/SS
DSPIC33EV64GM102-E/SS
DSPIC33EV32GM002-E/SS
DSPIC33EV32GM102-E/SS
DSPIC33EV64GM102-E/SSVAO
DSPIC33EV32GM102-E/SSVAO
DSPIC33EV128GM002-E/SO
DSPIC33EV128GM102-E/SO
DSPIC33EV64GM002-E/SO
DSPIC33EV64GM102-E/SO
DSPIC33EV32GM002-E/SO
DSPIC33EV32GM102-E/SO
DSPIC33EV64GM002-E/SOVAO
DSPIC33EV128GM006-E/MR
DSPIC33EV128GM106-E/MR
DSPIC33EV64GM006-E/MR
DSPIC33EV64GM106-E/MR
DSPIC33EV32GM006-E/MR
DSPIC33EV32GM106-E/MR
DSPIC33EV64GM006-E/MRVAO
DSPIC33EV128GM003-E/M5
DSPIC33EV128GM103-E/M5
DSPIC33EV64GM003-E/M5
DSPIC33EV64GM103-E/M5
DSPIC33EV32GM003-E/M5
DSPIC33EV32GM103-E/M5
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DSPIC33EV128GM104-E/ML

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DSPIC33EV64GM104-E/PT
DSPIC33EV32GM004-E/PT
DSPIC33EV32GM104-E/PT
DSPIC33EV128GM104-E/PTVAO
DSPIC33EV64GM104-E/PTVAO
DSPIC33EV128GM006-E/PT
DSPIC33EV128GM106-E/PT
DSPIC33EV64GM006-E/PT
DSPIC33EV64GM106-E/PT
DSPIC33EV32GM006-E/PT
DSPIC33EV32GM106-E/PT
DSPIC33EV128GM106-E/PTVAO
DSPIC33EV64GM106-E/PTVAO
DSPIC33EV32GM106-E/PTVAO
DSPIC33EV128GM004-E/P8
DSPIC33EV128GM104-E/P8
DSPIC33EV64GM004-E/P8
DSPIC33EV64GM104-E/P8
DSPIC33EV32GM004-E/P8
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DSPIC33EV32GM002-I/MM
DSPIC33EV32GM102-I/MM
DSPIC33EV128GM002-I/SP
DSPIC33EV128GM102-I/SP
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DSPIC33EV32GM002-I/SP
DSPIC33EV32GM102-I/SP
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DSPIC33EV32GM102-I/SSVAO

DSPIC33EV128GM002-I/SO
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DSPIC33EV32GM002-I/SO
DSPIC33EV32GM102-I/SO
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DSPIC33EV64GM006-I/MR
DSPIC33EV64GM106-I/MR
DSPIC33EV32GM006-I/MR
DSPIC33EV32GM106-I/MR
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DSPIC33EV64GM003-I/M5
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DSPIC33EV32GM106-I/PT
DSPIC33EV64GM006-I/PTVAO
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DSPIC33EV32GM002-H/MMVAO
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DSPIC33EV128GM102-H/SP
DSPIC33EV64GM002-H/SP
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DSPIC33EV32GM004-H/P8
DSPIC33EV32GM104-H/P8
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DSPIC33EV256GM102-E/MM
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DSPIC33EV256GM102-E/MMVAO
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DSPIC33EV256GM006-H/MR
DSPIC33EV256GM106-H/MR
DSPIC33EV256GM003-H/M5
DSPIC33EV256GM103-H/M5
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DSPIC33EV256GM004-H/PT
DSPIC33EV256GM104-H/PT
DSPIC33EV256GM006-H/PT
DSPIC33EV256GM106-H/PT
DSPIC33EV256GM004-H/P8
DSPIC33EV256GM104-H/P8

dsPIC33EVXXXGM00X/10X Family Silicon Errata and Data Sheet Clarification

The dsPIC33EVXXXGM00X/10X family devices that you have received conform functionally to the current Device Data Sheet (DS70005144**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of dsPIC33EVXXXGM00X/10X family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**AE**).

Data Sheet clarifications and corrections start on Page 27, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various silicon revisions of the dsPIC33EVXXXGM00X/10X family are shown in Table 1.

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TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)						
		A4	A6	A7	AC	AB	AD	AE
dsPIC33EV32GM002	0x5D01	—	—	0x4107	—	0x410B	0x410D	—
dsPIC33EV32GM102	0x5D09							
dsPIC33EV32GM003	0x5D02							
dsPIC33EV32GM103	0x5D0A							
dsPIC33EV32GM004	0x5D00							
dsPIC33EV32GM104	0x5D08							
dsPIC33EV32GM006	0x5D03							
dsPIC33EV32GM106	0x5D0B							
dsPIC33EV64GM002	0x5D11	0x4004	0x4006	0x4107	—	0x410B	0x410D	—
dsPIC33EV64GM102	0x5D19							
dsPIC33EV64GM003	0x5D12							
dsPIC33EV64GM103	0x5D1A							
dsPIC33EV64GM004	0x5D10							
dsPIC33EV64GM104	0x5D18							
dsPIC33EV64GM006	0x5D13							
dsPIC33EV64GM106	0x5D1B							
dsPIC33EV128GM002	0x5D21	0x4004	0x4006	0x4107	—	0x410B	0x410D	—
dsPIC33EV128GM102	0x5D29							
dsPIC33EV128GM003	0x5D22							
dsPIC33EV128GM103	0x5D2A							
dsPIC33EV128GM004	0x5D20							
dsPIC33EV128GM104	0x5D28							
dsPIC33EV128GM006	0x5D23							
dsPIC33EV128GM106	0x5D2B							
dsPIC33EV256GM002	0x5D31	0x4004	0x4006	—	0x400C	—	—	0x400E
dsPIC33EV256GM102	0x5D39							
dsPIC33EV256GM003	0x5D32							
dsPIC33EV256GM103	0x5D3A							
dsPIC33EV256GM004	0x5D30							
dsPIC33EV256GM104	0x5D38							
dsPIC33EV256GM006	0x5D33							
dsPIC33EV256GM106	0x5D3B							

Note1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]						
				A4	A6	A7	AC	AB	AD	AE
CPU	div.sd	1.	When using the signed 32-by-16-bit division instruction, div.sd, the Overflow bit is not getting set when an overflow occurs.	X	X	X	X	X	X	X
CPU	DO Loop	2.	PSV access, including Table Reads or Writes in the last instruction of a DO loop, is not allowed.	X	X	X	X	X	X	X
CPU	Program Memory	3.	The address error trap may occur while accessing certain program memory locations.	X	X	X	X	X	X	X
UART	Break Character Transmission	4.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.	X	X	X	X	X	X	X
SPI	Frame Sync Pulse	5.	When the SPIx module is configured as the SPI slave, the frame slave standard buffer with CKP = 0, the data are not transmitted in both 8-bit and 16-bit modes, but the data are being received correctly.	X	X	X	X	X	X	X
Input Capture	Synchronous Cascade mode	6.	Even numbered timer does not reset on a source clock rollover in a synchronous cascaded operation.	X	X	X	X	X	X	X
Output Compare	PWM mode	7.	In the scaled down timer source for the output compare module, the first PWM pulse may not appear on the OCx pin.	X	X	X	X	X	X	X
Output Compare	Interrupt	8.	Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin.	X	X	X	X	X	X	X
PWM	Immediate Update	9.	Dead time is not asserted when PDCx is updated to cause an immediate transition on the PWMxH and PWMxL outputs.	X	X	X	X	X	X	X
PWM	Complementary mode	10.	With dead time greater than zero, 0% and 100% duty cycle cannot be obtained on the PWMxL and PWMxH outputs.	X	X	X	X	X	X	X
PWM	Current Reset mode	11.	PWM Resets only occur in alternate cycles in Current Reset mode.	X	X	X	X	X	X	X
PWM	PWM Override	12.	Glitch on PWMxH and PWMxL pins when the override is turned off.	X	X	X	X	X	X	X
PWM	Complementary mode	13.	If PWM override is turned off during dead time, then the PWM generator may not provide dead time on the corresponding PWMxH/PWMxL edge transition.	X	X	X	X	X	X	X
PWM	Master Time Base mode	14.	When Immediate Update is disabled, certain changes to the PHASEx register may result in missing dead time.	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A4	A6	A7	AC	AB	AD	AE
ADC	DONE bit	15.	The Analog-to-Digital Conversion (ADC) Status (DONE) bit does not work when an external interrupt is selected as the ADC trigger source.	X	X	X	X	X	X	X
ADC	1.1 Msps Sampling	16.	Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.	X	X	X	X	X	X	X
CAN	DMA	17.	Write collisions on a DMA-enabled CAN module do not generate DMAC error traps.	X	X	X	X	X	X	X
I^2C	Overrun Interrupt	18.	Slave interrupt is not generated during an overrun condition.	X	X	X	X	X	X	X
CAN	Receive Buffer	19.	Read-Modify-Write operation on a CxRXFULx register may not update correctly.	X	X	X	X	X	X	X
ADC	AC/DC Electrical Characteristics	20.	The AC/DC electrical characteristic, integral nonlinearity error in the ADC module, is not within the specifications published in the data sheet.	X	X					
Core	DC Electrical Characteristics (IPD)	21.	The DC electrical characteristics for IPD are not within the specification published in the data sheet for the low-temperature range.	X						
PWM	Redundant/ Push-Pull Output mode	22.	When Immediate Update is disabled, changing the duty cycle value from a non-zero value to zero will produce a glitch pulse equal to one PWM clock.	X	X	X	X	X	X	X
Reset	Flash Standby during Sleep	23.	Functionality of the VREGSF bit (RCON[11]) = 0 is not functioning.	X						
Flash	ECC Error Trap	24.	When the system clock is above 60 MHz (30 MIPS), an unexpected ECC error trap may be generated.	X						
Comparator	Offset	25.	Comparator may not work under certain voltage and temperature conditions.	X	X		X			X
Reset	Voltage Regulator (Standby mode)	26.	Standby mode may not work at high temperatures.	X	X	X	X	X	X	X
SPI	Enhanced Buffer mode	27.	Received data of SPI are sampled one clock cycle late.	X	X	X	X	X	X	X
Input Capture	Cascade mode	28.	When ICx is used in Cascaded mode, even timer does not increment immediately when odd timer rolls over, but increments one cycle after the rollover.	X	X	X	X	X	X	X
I^2C	Slave mode	29.	Bus data corruption with multiple slaves on bus.	X	X	X	X	X	X	X
I^2C	Slave mode	30.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X	X	X	X	X	X
CTMU	Edge mode	31.	In Time Generation mode (TGEN), the EDG1STAT bit does not get set.	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]						
				A4	A6	A7	AC	AB	AD	AE
PWM	Push-Pull mode	32.	Push-pull output logic to produce back-to-back pulses when writing to the Period register occurs on the PWMx cycle boundaries.	X	X	X	X	X	X	X
PWM	Push-Pull mode	33.	Push-pull output logic to produce back-to-back pulses when writing to the Period register that coincides with the period rollover event.	X	X	X	X	X	X	X
PWM	Trigger mode	34.	Primary Trigger Compare Value register (TRIGx) will not trigger at the point defined by the TRIGx register values on the first instance.	X	X	X	X	X	X	X
PWM	Center-Aligned Complementary mode	35.	Dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP is disabled.	X	X	X	X	X	X	X
Reset	INTCON4	36.	ECCDBE bit is always read as '0'.	X	X	X	X	X	X	X
SPI	DMA Data Transfer	37.	The data transferred from DMA to the SPI buffer may get corrupted if the CPU accesses any Special Function Registers (SFRs).	X	X	X				
Power-Saving Mode	Doze mode	38.	Stack error trap may occur under certain circumstances, when the processor speed is switched between normal Run mode and Doze mode.	X	X	X	X	X	X	X
Core	Variable Interrupt Latency	39.	Address error trap may occur under certain circumstances if Variable Interrupt Latency mode is enabled.	X	X	X	X	X	X	X
Core	DO Loop	40.	DO loops may work incorrectly if nested interrupts are enabled and interrupts occur during the last two instructions of the DO loop.	X	X	X	X	X	X	X
I^2C	Address Hold	41.	When AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X	X	X	X	X	X	X
I^2C	Data Hold	42.	When DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.	X	X	X	X	X	X	X
SPI	SPIx Enable	43.	When the SPIx module is enabled for the first time, there may be a spurious clock on the SCKx pin, which causes a mismatch between the clock and data lines.	X	X	X	X	X	X	X
SPI	Master mode	44.	Received data are shifted by one bit when CKP = 1 and CKE = 0.	X	X	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)						
				A4	A6	A7	AC	AB	AD	AE
Output Compare (OC)	Cascade mode	45.	In Edge-Aligned Cascade mode, if the OCxR and OCxRS values are less than 0x0000FFFF, then the OC output will remain high.	X	X	X	X	X	X	X
Output Compare (OC)	Edge-Aligned mode	46.	When the OCx is configured in Edge-Aligned mode and the OCx pin is initialized to high, the OCxR is set to non-zero and a non-peripheral clock is set as the OCx clock. Then, the OCx output misses the first pulse.	X	X	X	X	X	X	X
CPU	Data Flash Reads	47.	Given a specific set of preconditions, when two or more data Flash read instructions (via Program Space Visibility (PSV) read or Table Read) are executed back-to-back, one or more subsequent instructions will be misexecuted.	X	X	X	X	X	X	X
I/O	POR	48.	During specific start-up conditions, a voltage spike may be observed on the I/O pins.	X	X	X	X	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**AE**).

1. Module: CPU

When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit does not always get set when an overflow occurs.

This erratum only affects operations in which at least one of the following conditions is true:

a) Dividend and divisor differ in sign,
b) Dividend > 0x3FFFFFFF or
c) Dividend ≤ 0xC0000000.

Work around

The application software must perform both the following actions in order to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.
b) If the dividend and divisor differ in sign (e.g., dividend is negative and divisor is positive), then after executing the `div.sd` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient.

If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

2. Module: CPU

Table Write (`TBLWTx`), Table Read (`TBLRDx`) and PSV Flash read instructions should not be used in the first or last instruction locations of a `DO` loop.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

3. Module: CPU

An unexpected address error trap may occur during accesses to program memory addresses, 0x001 through 0x200. This has been observed when one or more interrupt requests are asserted while reading or writing program memory addresses using `TBLRDx`, `TBLWTx` or PSV-based instructions.

Work around

Before executing the instructions that read or write the program memory addresses, 0x001 through 0x200, disable the interrupts using the `DISI` instruction.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

4. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA[11]), to be cleared instead of the TRMT bit (UxSTA[8]) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

5. Module: SPI

When the SPIx module is configured in SPIx Slave mode (MSTEN bit (SPIxCON1[5]) = 0), the frame slave (FRMEN bit (SPIxCON2[15]) = 1) and the SPIFSD bit (SPIxCON2[14] = 1), in Standard Buffer mode with the Clock Polarity Select bit, CKP = 0, the data are not transmitted in both 8-bit and 16-bit mode, but the data are being received correctly.

Work around

Adding a capacitance on the signal, as shown in Figure 1, will help the data to be received properly.

FIGURE 1:

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

6. Module: Input Capture

The even numbered timer does not reset on a source clock rollover in Synchronous Cascaded mode operation.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules), ICy and ICx form a single 32-bit module. In Synchronous Cascaded mode (IC32 = 1, ICTRIG = 0 and the SYNCSEL[4:0] bits are not equal to 0h), both timers, ICyTMR:ICxTMR, must reset on a Sync_trig input from the 32-bit source timers, but only the odd timer (ICxTMR) is getting reset on a Sync Trigger input.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

7. Module: Output Compare

The first PWM pulse may not appear on the OCx pin if the timer source of the Output Compare x module is scaled down.

The first pulse on the OCx pin is missed in PWM mode when the timer source for the Output Compare x module is scaled down (1:8, 1:64 or 1:256) using the Timerx Input Clock Prescale Select bits, TCKPS[1:0] (TxCON[5:4]).

Work around

Configure the prescaler for the source timer to 1:1 for output compare.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

8. Module: Output Compare

Under certain circumstances, an output compare match may cause the Output Compare x Interrupt Flag (OCxIF) bit to become set prior to the Change-of-State (COS) of the OCx pin. This has been observed when all of the following are true:

- The module is in One-Shot mode (OCM[2:0] = 001, 010 or 100);
- One of the timer modules is being used as the time base; and
- A timer prescaler other than 1:1 is selected

If the module is re-initialized by clearing the OCM[2:0] bits after the One-Shot mode compare, the OCx pin may not be driven as expected.

Work around

After OCxIF is set, allow an interval (in CPU cycles) of at least twice the prescaler factor to elapse before clearing the OCM[2:0] bits. For example, for a prescaler value of 1:8, allow 16 CPU cycles to elapse after the interrupt.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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9. Module: PWM

The PWM generator may not assert dead time on the edges of transitions. This has been observed when all of the following conditions are present:

- The PWM generator is configured to operate in Complementary mode with Independent Time Base (ITB) or master time base;
- Immediate update is enabled; and
- The value in the PDCx register is updated in such a manner that the PWMxH and PWMxL outputs make an immediate transition.

The current duty cycle, PDCOLD, newly calculated duty cycle, PDCNEW, and the point at which a write to the Duty Cycle register occurs within the PWM time base, will determine if the PWMxH and PWMxL outputs make an immediate transition. PWMxH and PWMxL outputs make an immediate transition if the Duty Cycle register is written with a new value, PDCNEW, at a point of time when the PWM time base is counting a value that is in between PDCNEW and PDCOLD. Additionally, writing to the Duty Cycle register, close to the instant of time where dead time is being applied, may result in a reduced dead time effective on the PWMxH and PWMxL transition edges.

In Figure 2, if the duty cycle write occurred in the shaded box, then PWMxH and PWMxL will make an immediate transition without dead time.

FIGURE 2: TIMING DIAGRAMS FOR CENTER-ALIGNED AND EDGE-ALIGNED MODES

Work around

None.

However, in most applications, the duty cycle update timing can be controlled using the TRIGx trigger or Special Event Trigger, such that the above mentioned conditions are avoided altogether.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

10. Module: PWM

This issue is applicable when a PWM generator is configured to operate in an Independent Time Base mode with either Center-Aligned Complementary mode or Edge-Aligned Complementary mode. When dead time is non-zero, the PWMxL is not asserted for 100% of the time when the Programmed Generator Duty Cycle x (PDCx) is zero. Similarly, when dead time is non-zero, the PWMxH is not asserted for 100% of the time when PDCx is equal to the Primary Phase-Shift register (PHASEx). This issue also applies to Master Time Base mode.

Work around

In Center-Aligned mode:

- To obtain 0% duty cycle, zero out the ALTDTRx register and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the ALTDTRx register, and then write (PHASEx + 2) to the PDCx register.

In Edge-Aligned mode:

- To obtain 0% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write zero to the PDCx register.
- To obtain 100% duty cycle, zero out the registers, DTRx and ALTDTRx, and then write (PHASEx + 1) to the PDCx register.

Alternatively, in both Center-Aligned and Edge-Aligned PWM modes, 0% and 100% duty cycle can be obtained by enabling the PWM override (IOCONx = `0b11`) with the Output Override Synchronization bit (OSYNC) set as '`1`':

- For 0% duty cycle, set the Override Data bits (OVRDAT[1:0]) for PWMxH and PWMxL as '`0b01`'
- For 100% duty cycle, set the Override Data bits (OVRDAT[1:0]) for PWMxH and PWMxL as '`0b10`'

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

11. Module: PWM

The PWM Reset may only occur on alternate PWM cycles when both of the following conditions are met:

- The PWM generator is configured to operate in a Current Reset mode (PWMCONx[1] = `1`).
- Independent Time Base mode is selected (PWMCONx[9] = `1`).

Work around

There are two proposed solutions; others may exist.

1. **Software Solution**: Generate an interrupt when the comparator state changes. The interrupt can either be a comparator or a PWM Fault interrupt and must be a high priority. During this interrupt's service routine, update the PHASEx register with a value less than the PDCx; then, immediately update the PHASEx with the PWM period required by the application. Example 1 shows a possible implementation.

EXAMPLE 1:

```
PWMx ISR:
{           PHASEx = PDCx-100;
            PHASEx = PWM_PERIOD;
            PWMxIF = 0;
}
```

2. **Hardware Solution**: When the current Reset signal is coming from an external comparator selected by FCLCONx[14:10], limit the pulse width of the external trigger to less than the maximum value specified in Table 3. The maximum pulse width is determined by the PWM resolution, as selected by the PCLKDIV[2:0] bits (PTCON2[2:0]).

TABLE 3: MAXIMUM PULSE WIDTH FOR CURRENT-LIMIT SIGNAL

PCLKDIV[2:0]	Maximum Pulse Width (ns)
000	20
001	40
010	80
011	160
100	320
101	640
110	1280

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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12. Module: PWM

In Complementary mode after the PWM module is enabled (PTEN = 1), if the PWM override is turned off, a one Tosc glitch will be present on the rising edge of either the PWMxH or PWMxL pins, whichever occurs first, as shown in Figure 3.

The glitch will be present on PWMxH/PWMxL every time the override state is changed from override enabled to override disabled. The width of this glitch is equal to one Tosc when PCLKDIV[2:0] (PTCON2[2:0]) = 000. Increasing the PWMx input clock prescaler setting will increase the width of the glitch accordingly.

Since the width of the glitch is just one Tosc at higher values of Fosc, the glitch may not be visible on the PWMxH/PWMxL pins due to pin and PCB trace capacitances.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

FIGURE 3: ILLUSTRATION OF 1 Tosc GLITCH WHEN PWM OVERRIDE IS TURNED OFF

13. Module: PWM

In Complementary Output mode, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when the following occurs:

- Output override synchronization is configured to occur on the CPU clock boundary (IOCONx[0] = 0);
- Both PWMxH and PWMxL overrides are enabled prior to the event (OVRENH and OVRENL are both '1'), and
- Both overrides are disabled (OVRENH and OVRENL are both '0') at the instant the dead time should be asserted (Figure 4). This has been observed in both Center-Aligned and Edge-Aligned modes.

FIGURE 4:

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

14. Module: PWM

In Edge-Aligned PWM mode with Master Time Base (PWMCONx[9] = 0) and Immediate Update disabled (PWMCONx[0] = 0), after enabling the PWM module (PTCON[15] = 1), changes to the PHASEx register, such that PHASEx is less than DTRx or PHASEx is greater than PDCx, will result in missing dead time at the PWMxH-PWMxL transition that will occur at the next master period boundary.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

15. Module: ADC

The ADC Conversion Status (DONE) bit (AD1CON1[0]) does not indicate completion of a conversion when an external interrupt is selected as the ADC trigger source (SSRC[2:0] (AD1CON1[7:5]) = 0x1).

Work around

Use an ADC interrupt or poll the AD1IF bit in the IFS0 register to determine the completion of the conversion.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

16. Module: ADC

Selecting the same ANx input (AN0 or AN3) for CH0 and CH1 to achieve a 1.1 Msps sampling rate results in erroneous readings for CH1.

Work around

Bring the analog signal into the device using both AN0 and AN3, connect externally, and then assign one input to CH0 and the other to CH1.

If selecting AN0 on CH1 (CH123Sx = 0), select AN3 on CH0 (CH0Sx = 3). Conversely, if selecting AN3 on CH1 (CH123Sx = 1), select AN0 on CH0 (CH0Sx = 0).

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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17. Module: CAN

When DMA is used with the CAN module, and the CPU and DMA write to a CAN Special Function Register (SFR) at the same time, the DMAC error trap is not occurring. In addition, neither the PWCOL[3:0] bits of the DMAPWC SFR or the DMACERR bit of the INTCON1 SFR are being set. Since the PWCOLx bits are not set, subsequent DMA requests to that channel are not ignored.

Work around

There is no work around; however, under normal circumstances, this situation must not arise. When DMA is used with the CAN module, the application should not be writing to the CAN SFRs.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

18. Module: I^2C

When operating in Slave mode, the I^2C module does not trigger an interrupt when an overrun condition occurs.

Work around

Monitor the I2COV bit (I2CxSTAT[6]) using the software.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

19. Module: CAN

When the DMA controller is copying the received CAN message into an appropriate message buffer in the user-defined device RAM area, any Read-Modify-Write operation on a CxRXFULx (C1RXFUL1, C1RXFUL2, C2RXFUL1 and C2RXFUL2) register may not update the CxRXFULx register properly. The CPU can only clear a bit in the CxRXFULx register. A Read-Modify-Write operation successfully clears the intended bit, but it may incorrectly clear the bit set by the CAN module after a successful transfer of a message into RAM by the DMA.

Work around

Avoid Read-Modify-Write operations on the C1RXFUL1, C1RXFUL2, C2RXFUL1 and C2RXFUL2 registers. See Example 2 to clear any bit in the C1RXFUL1, C1RXFUL2, C2RXFUL1 and C2RXFUL2 registers while developing code in C.

EXAMPLE 2: WORK AROUND CODE

```
if (C1FIFObits.FNRB <= 15)
{
   C1RXFUL1 = ~(0x001 << C1FIFObits.FNRB);
}
else
{
   C1RXFUL2 = ~(0x001 << (C1FIFObits.FNRB - 16));

}
```

The CPU can only clear a bit in the CxRXFULx registers, but the CPU cannot set any bit in any of the CxRXFULx registers. Therefore, in the work around (Example 2):

- If the FNRB[5:0] (C1FIFO[5:0]) bits value is less than or equal to 15, only one bit of the C1RXFUL1 register will be cleared depending on the FNRB[5:0] bits value.
- If the FNRB[5:0] bits value is greater than 15, only one bit of the C1RXFUL2 register will be cleared depending on the FNRB[5:0] bits value.

This same method should be adopted for the C2RXFUL1 and C2RXFUL2 registers.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

20. Module: ADC

The AC/DC electrical characteristics, Integral Nonlinearity (INL), offset and gain error in the ADC module, differ for the first 200 codes in the 12-Bit ADC mode from the specifications in the published data sheet. Refer to Table 4 (below) for details.

Work around

None.

Table 4 shows the offset/gain error for the first 200 codes in the12-bit ADC.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X						

TABLE 4: ADC ACCURACY (12-BIT MODE) – MEASUREMENTS WITH INTERNAL VREF+/VREF-

Param No.	Symbol	Characteristic	Min.	Typ.	Max.			Units	Conditions
					+85°C	+125°C	+150°C		
AD20a	Nr	Resolution	12 data bits					bits	
AD21a	INL	Integral Nonlinearity	-2	—	+2	+2.5	+3.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 4.5V
AD21a	INL	Integral Nonlinearity	-2	—	+2.5	+5.5	+7.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.0V
AD21a	INL	Integral Nonlinearity	-2	—	+5.5	+9.5	+14	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V

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21. Module: Core

The DC electrical characteristics for the I_{PD} (Sleep Current) are in the higher range for temperatures at -40°C, +25°C and +85°C. Refer to Table 5 (below) for details.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X							

TABLE 5: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	**Typ.**	**Max.**	**Units**	**Conditions**		
Power-Down Current (I_{PD})						
DC60d	315	360	μA	-40°C	5.0V	Base Power-Down Current
DC60a	315	360	μA	+25°C		
DC60b	450	640	μA	+85°C		

Note: All measurements were taken with the VREGSF bit (RCON[11]) set as '1'.

22. Module: PWM

In the Redundant Output mode (IOCONx[11:10] = 10) and Push-Pull Output mode (IOCONx[11:10] = 01) with Immediate Update disabled (PWMCONx[0] = 0), when the Duty Cycle register is updated from a non-zero value to zero, a glitch pulse of a width equal to one PWM clock will appear at the next PWM period boundary, as shown in Figure 5, for the Redundant Output mode. Here, the Duty Cycle register refers to the PDCx register if PWMCONx[8] = 0 or the MDC register if PWMCONx[8] = 1.

FIGURE 5:

Work around

If the application requires a zero duty cycle output, there are two possible work around methods:

1. Use the PWM override feature to override the PWM output to a low state instead of writing to the Duty Cycle register. In order to switch back to a non-zero duty cycle output, turn off the PWM override. The override-on and override-off events must be timed close to the PWM period boundary if the IOCONx register has been configured with IOCON[0] = 0 (i.e., output overrides via the OVDDAT[1:0] bits occur on the next CPU clock boundary).
2. Enable the Immediate Update (PWMCONx[0] = 1) while configuring the PWM module, i.e., before enabling the PWM module (PTCON[15] = 1). With Immediate Update enabled, writes to the Duty Cycle register can have an immediate effect on the PWM output. Hence, duty cycle write operations must be timed close to the PWM period boundary in order to avoid distortions in the PWM output.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

23. Module: Reset

When using the functionality of the Flash regulator voltage during Sleep mode, the VREGSF bit (RCON[11]) = 0 is not functioning, thereby burning high IPD currents.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X							

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24. Module: Flash

When the system clock is above 60 MHz (30 MIPS), an unexpected ECC error trap may be generated. There are three scenarios which display this behavior:

Scenario 1: (see Example 3)

a) If the PSV Pointer is set right before the PSV access; or

b) If the Flash data are read using the `TBLRDL` or `TBLRDH` instructions and the Flash offset is set right before the access.

Scenario 2: (see Example 5)

a) If the `REPEAT` instruction is used to access PSV; or

b) If the `REPEAT` instruction is used with `TBLRDL` or `TBLRDH` instructions to access the Flash memory.

Scenario 3:

a) If a `DO` loop instruction is used to access PSV; or

b) If a `DO` loop instruction is used with `TBLRDL` or `TBLRDH` instructions to access the Flash memory.

Work around

For Scenario 1: A `NOP` instruction should be inserted after setting the PSV Pointer or the data offset to separate the address load and memory access (see Example 5).

For Scenario 2: None. Do not use the `REPEAT` instruction for PSV access, or with `TBLRDL` or `TBLRDH` instructions.

For Scenario 3: None. Do not use the `DO` loop instruction for PSV access, or with `TBLRDL` or `TBLRDH` instructions.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X							

EXAMPLE 3: SCENARIO 1 CASES FOR ECC TRAP ERRORS

```
// ECC Error Trap with PSV access (Scenario 1a):
mov     #psvoffset(MyPSVData), w4            ;move PSV pointer to w4
mov     [w4], w5                             ;read from PSV, ECC trap is generated here

// ECC Error Trap with tabble offset (Scenario 1b):
mov     #tbloffset(MyFlashData), w4          ;move the data offset to w4
tblrdl  [w4], w5                             ;read from flash, ECC trap is generated here
```

EXAMPLE 4: WORK AROUNDS FOR SCENARIO 1

```
// Work around for PSV access(Scenario 1a):
mov     #psvoffset(MyPSVData), w4        ;move PSV pointer to w4
nop                                      ;WORK AROUND
mov     [w4], w5                         ;read from PSV

// Work around for Table Read instructions(Scenario 1b):
mov     #tbloffset(MyPSVData), w4        ;move PSV pointer to w4
nop                                      ;WORK AROUND
tblrdl  [w4], w5                         ;read from Flash
```

EXAMPLE 5: SCENARIO 2 CASES

```
// ECC Error Trap with REPEAT instruction and PSV access(Scenario 2a):
mov     #psvoffset(MyPSVData), w4            ;move source PSV address to w4
mov     #0x1800, w6                          ;move destination address to w6
repeat  #10
mov     [w4++], [w5++]                       ;move data from PSV to RAM, ECC trap is generated here

// ECC Error Trap with REPEAT instruction and Table Read instructions(Scenario 2b):
mov     #tbloffset(MyFlashData), w4          ;move source data address to w4
mov     #0x1800, w6                          ;move destination address to w6
repeat  #10
tblrdl  [w4++], [w5++]                       ;move data from flash to RAM, ECC trap is generated here
```

25. Module: Comparator

Over the lifetime of the device, the comparators may, at some point, fail to function when both of the following conditions are true:

- The comparator input voltage is below 4.5V
- Ambient temperature is below +55°C

The comparators will still function when the ambient temperature exceeds +55°C.

Work around

If comparators will be needed under these circumstances, design the application to use the on-chip op amps in Comparator mode instead. Alternatively, external comparators may be used.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X		X			X	

26. Module: Reset

Note: This issue only applies to High-Temperature rated dsPIC33EVXXXGM00X/10X family devices (temperature designator of 'H' in the catalog part number.)

When operating at ambient temperatures above +130°C, Standby mode for the on-chip voltage regulator may not function properly. This makes the device susceptible to unexpected wake-ups from Sleep mode.

Work around

If Sleep mode operation is required at high temperatures, keep the VREGS bit (RCON[8]) set.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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27. Module: SPI

Received data of the SPI are sampled one clock cycle late for the following conditions:

1. When the SPI is configured as master (MSTEN = 1), frame sync pulse input (SPIFSD = 1), enhanced buffer (SPIBEN = 1), CKP = 1, SMP = 1, FRMPOL = 1, FRMDLY = 1.
2. When the SPI is configured as master (MSTEN = 1), frame sync pulse input (SPIFSD = 1), enhanced buffer (SPIBEN = 1), CKP = 1, SMP = 1, FRMPOL = 0, FRMDLY = 0.

For example, the correct data that should be received are 0x9191, 0x9292, 0x9393, 0x9494, 0x9595, 0x9696, 0x9797, 0x9898, but the actual data received are 0x2323, 0x2525, 0x2727, 0x2929, 0x2B2B, 0x2D2D, 0x2F2F, 0x3130 (Figure 6).

FIGURE 6:

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

28. Module: Input Capture

When the ICx is used in Cascaded mode, the even timer does not increment immediately when the odd timer rolls over but increments one cycle after the rollover.

In the cascaded configuration, ICy:ICx (ICy represents the even numbered modules and ICx represents the odd numbered modules) form a single 32-bit module. In such a configuration, when ICx counts for a 16-bit value (65535 cycles), and rolls over to '0' during the next clock cycle (65536th cycle), ICy should immediately increment by '1'; but the ICy timer remains at '0', and during the next clock cycle (65537th cycle), both the ICx and ICy timers increment by '1'.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

29. Module: I²C

In applications with multiple I²C slaves, bus data can become corrupted when the data payload sent to an addressed slave device matches the bus address of another (unaddressed) slave device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other slave devices) until a Stop bit is received.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

30. Module: I²C

In I²C Slave 10-Bit Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during an Acknowledgment sequence. The issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes.

The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on the upper address byte reception. When AHEN = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a very short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

31. Module: CTMU

When the CTMU is configured in Edge mode, with the Edge Delay Generation bit (TGEN (CTMUCON1[12]) = 1) enabled, the ED1STAT bit does not get set.

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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32. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx[11:10] = 10) with the Enable Immediate Period Update bit (PTCON[10] = 0), a write to the Period register occurs on the PWMx cycle boundaries. This may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins.

Work around

Workaround #1: Ensure that the Enable Immediate Period Update bit (PTCON [10] = 1) is set.

Workaround #2: Configure the PWM phase-shift value (PHASEx[15:0]) with a value more than '0x0007'. When multiple PWM generators are configured in Push-Pull mode, configure the PWM phase-shift value with a value more than '0x0007' for respective PWM generators.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

33. Module: PWM

When the PWM module is configured for Push-Pull mode (IOCONx[11:10] = 10) with the Enable Immediate Period Update bit enabled (PTCON [10] = 1), a write to the Period register that coincides with the period rollover event may cause the push-pull output logic to produce back-to-back pulses on the PWMx pins.

Work around

Ensure that the update to the PWMx Period register occurs away from the PWM rollover event by setting the EIPU bit (PTCON[10] = 1). Use either the PWMx Special Event Trigger register (SEVTCMP) or the PWMx Primary Trigger Compare Value register (TRIGx) to generate a PWM Interrupt Service Routine (ISR) near the start of the PWM cycle. This ISR will ensure that period writes do not occur near the PWM period rollover event.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

34. Module: PWM

The triggers generated by the PWMx Primary Trigger Compare Value register (TRIGx) will not trigger at the point defined by the TRIGx register values on the first instance for the configurations listed below. Subsequent trigger instances are not affected.

- Trigger compare values for TRIGx are less than 8 counts.
- Trigger Output Divider bits, TRGDIV[3:0] (TRGCONx[15:12]), are greater than '0'.
- Trigger Postscaler Start Enable Select bits (TRGSTRT[5:0]) are equal to '0'.

Work around

Configure the PWMx Primary Trigger Compare Value register (TRIGx) values to be equal to, or greater than, eight.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

35. Module: PWM

In Center-Aligned Complementary mode with Independent Time Base, the expected dead time between transitions of the PWMxH and PWMxL outputs may not be asserted when SWAP is disabled under the following conditions:

- PWMx module is enabled (PTEN = 1)
- SWAP is enabled prior to this event

Work around

None.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

36. Module: Reset

When an ECC double-bit error occurs, the code is switched to the trap routine; the ECCDBE bit (INTCON4[1]) is writable, but always read as '0'.

Work around

Clear the ECCDBE bit (INTCON4[1]) in the trap routine for it to come out of the trap.

Affected Silicon Revisions

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

37. Module: SPI

The data transferred from DMA to the SPI buffer may get corrupted if the CPU accesses any Special Function Registers (SFRs) during the data transfer.

Work around

None.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X					

38. Module: Power-Saving Mode

Stack error trap may be generated, when all of the following conditions are met:

- Device operates in Doze mode with Processor Clock Reduction Select bits (Doze Ratio) in CLKDIV set as '0b011' or '0b1xx'.
- Multiple interrupts are enabled.
- In user function, the processor speed is switched between normal Run mode and Doze mode.

Work around

Use the Doze mode with CLKDIV = 0b010, 0b001 or 0b000.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

39. Module: Core

An address error trap or incorrect application behavior may occur if the variable exception processing latency is enabled by setting the VAR bit (CORCON[15]) = 1).

Work around

Enable the Fixed Interrupt Latency mode by clearing the VAR bit (VAR (CORCON[15]) = 0).

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

40. Module: Core

When interrupt nesting is enabled by clearing the NSTDIS bit (INTCON1[15] = 0), an interrupt that occurs during the last two instructions of the DO loop can end it prematurely. The DCOUNT is incorrectly decremented twice when:

- An interrupt occurs during the last two instructions of a DO loop, and
- The second higher priority interrupt occurs exactly four instruction cycles later.

Work around

Disable interrupt nesting by setting the NSTDIS bit (INTCON1[15] = 1). Alternatively, for interrupts of priority levels up to 6, use the DISI instruction to disable the nested interrupts while executing the last two instructions of the DO loop.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

41. Module: I^2C

When AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, the user software should clear ACKDT (Acknowledge Data) on receiving the Start bit.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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42. Module: I²C

When DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, the user software should clear ACKDT (Acknowledge Data) on receiving the Start bit.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

43. Module: SPI

When the SPIx module is enabled for the first time, there may be a spurious clock on the SCKx pin. This may result in one bit of data getting shifted out on the data line, resulting in a mismatch between the clock and data lines. This issue may also occur when the SPIx module is disabled during data transmission and subsequently enabled.

Work around

1. Disable the SPIx module after two SPIx cycles and then re-enable SPIx; this will synchronize the clock and data.
2. If the SPIx module is configured on the PPS pins, first enable the SPIx without configuring the PPS, then allow the two SPIx clocks to pass. At that time, configure the PPS to connect to the SPIx module. This will prevent the spurious SPIx clock going out on the pin. If the SPIx module is turned off periodically, ensure that the PPS is turned off as well.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

44. Module: SPI

In Master mode, the SPI device reads the data on the SDIx line incorrectly. Data are shifted by one bit; for example, if 0x37 is transmitted, it is read as 0x1B.

This issue occurs for the following configurations:

- SMP = x
- CKE = 0
- CKP = 1
- Master MIPS ≤ Slave MIPS

This issue is seen over a range of SPI clock frequencies (1 MHz to 16 MHz).

Work around

When CKE = 0 and CKP = 1, execute the following sequence to initiate an SPI communication:

a) Set the Slave Select line to the Idle state
b) Set the SCKx pin high
c) Enable Master mode
d) Enable the module
e) Assert the Slave Select line

Note: If the SPI slave device does not use the $\overline{SSx}$ line, then the SPI slave should be enabled only after the master clock line is set to high.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

45. Module: Output Compare (OC)

In the cascaded configuration, OCy:OCx (where OCy represents the even numbered Output Compare modules and OCx represents the odd numbered modules) form a single 32-bit module. If the cascaded OCy:OCx modules are configured in Edge-Aligned mode, and the values of the cascaded OCyR:OCxR and OCyRS:OCxRS are less than 0x0000FFFF, then the cascaded OC output will remain high, even when the OCyTMR:OCxTMR matches the OCyR:OCxR values.

Work around

None.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

46. Module: Output Compare (OC)

Whenever an OCx is configured in Edge-Aligned mode:

- The OCxR value is set to non-zero
- A non-peripheral clock is set as the OCx clock (OCTSEL[2:0] bits are not equal to '`0b111`')
- The OCx pin is initialized to high

The OCx output is immediately pulled low and continues to remain low during the entire cycle. Normal operations will resume from the second cycle.

Work around

None.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

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47. Module: CPU

> **Note:** This issue is deterministic based on the instruction sequence executed, and is not sensitive to manufacturing process, temperature, voltage or other application operating conditions that do not affect the instruction sequence.

When two or more data Flash read instructions (via Program Space Visibility (PSV) read or table read) are executed back-to-back, one or more subsequent instructions can be misexecuted when all of the conditions in Table 6 occur.

TABLE 6: REQUIRED CONDITIONS

1.	A PSV `MOV.D` instruction is executed with opcode at address ending in 0x0, 0x4, 0x8 or 0xC; and
2.	Some "connecting code" is executed (following the `MOV.D` of condition 1), with the properties: a) The connecting code does not include any program flow changes, including: taken branch instructions (including all versions of `BRA`, `CPBEQ`, `CPBGT`, `CPBLT`, `CPBNE`), `CALL`, `CALL.L`, `GOTO`, `GOTO.L`, `RCALL`, `RETLW`, `RETURN`, vectoring to an ISR, returning from an interrupt (`RETFIE`) and certain debug operations, such as Break and one-step; and b) The connecting code does not include a `TBLRDx` or non-`MOV.D` PSV instruction, located at a Flash memory address ending in 0x0, 0x4, 0x8 or 0xC; and c) The connecting code is at least two instruction words in length; and d) The connecting code does not end with a `REPEAT` instruction, with count > `0`; and
3.	≥ 2 back-to-back PSV or `TBLRDx` instructions are executed (following the code of condition 2), where the first of the back-to-back instructions is located at an address ending in 0x2, 0x6, 0xA or 0xE.

Figure 7 provides an example of the effective behavior.

FIGURE 7: SIMPLIFIED BEHAVIOR

Work around

The issue can be avoided by ensuring any one or more of the requirements are not met. For example:

1. All instances of PSV `MOV.D` can be replaced with two PSV `MOV` instructions instead. Non-PSV `MOV.D` instructions acting on RAM/SFRs do not need to be modified; or
2. If not already present, a program flow change instruction (such as `BRA $+2`) can be inserted above back-to-back data Flash read sequences; or
3. Back-to-back data Flash read instruction sequences can be broken up by inserting a non-Flash read instruction (such as a `NOP`), in between the Flash read instructions; or
4. The alignment of the code can be shifted to avoid the required opcode location addresses.

C code built with MPLAB® XC16 Compiler Version 1.32, or later, implements the work around by default. However, if the application uses Assembly language routines, these should be manually modified to implement the work around. Additionally, if precompiled libraries are used, these should be built with XC16 Version 1.32 or later. For additional information, please visit: **www.microchip.com/erratum_psrd_psrd**

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X	X	X	

48. Module: I/O

During device power-up, the I/O pins may drive a pulse up to 1.6V for a duration of up to 300 µSec at temperatures of 0ºC or below.

Work around

Ensure the circuitry that is connected to the pins can endure this active duration.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur. High-voltage applications with complementary switches should power the high voltage 500 µSec later than powering the dsPIC® device to avoid the issue. The behavior is specific to each part and not affected by aging.

Affected Silicon Revisions.

A4	A6	A7	AC	AB	AD	AE	
X	X	X	X	X			

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005144**H**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2014)

Initial version of this document; issued for silicon revision A4.

Includes silicon issues 1 (CPU), 2, (CPU) 3 (CPU), 4 (UART), 5 (SPI), 6 (Input Capture), 7 (Output Compare), 8 (Output Compare), 9 (PWM), 10 (PWM), 11 (PWM), 12 (PWM), 13 (PWM), 14 (PWM), 15 (ADC), 16 (ADC), 17 (CAN), 18 (I^2C), 19 (CAN), 20 (ADC), 21 (IPD), 22 (PWM) and 23 (Reset).

Rev B Document (8/2014)

This revision includes silicon issue 24 (Flash). Updated issues 9 (PWM),11 (PWM) and 23 (Reset). Updated Table 2.

Rev C Document (11/2014)

Adds silicon revision A6; includes all current silicon issues through the previous document revision, except for issues 21 (Core), 23 (Reset) and 24 (Flash).

Adds new silicon issues 25 (Comparator) to silicon revisions A4 and A6.

Adds new silicon issue 26 (Reset) to silicon revision A6 only.

Changes the title of issue 21 to “Core” from “IPD”, to be consistent with current nomenclature practice; the issue itself is unchanged.

Updates the Work Around for issue 7 (Output Compare).

Amends issue 21 (Core) to add Parameter DC60b (IPD, +85°C).

Changes the layout of issue 24 (Flash) to consolidate the text and code examples on a single page, and to enhance readability. The issue itself is unchanged.

Rev D Document (4/2015)

Adds silicon revision A7.

Adds new silicon issues 27 (SPI), 28 (Input Capture), 29-30 (I^2C), 31 (CTMU), 32-35 (PWM) and 36 (Reset).

Updates Table 1 and Table 2, and silicon issue 10 (PWM) and 13 (PWM).

Rev E Document (5/2015)

Updates the notes on Page 1 and Page 7, where the current silicon revision is shown as A6; it should be A7.

Revision F Document (8/2015)

Updates silicon issues 27 (SPI) and 36 (Reset).

Adds data sheet clarifications 1 (Qualification and Class B Support), 2-3 (Special Features), 4 (Memory Organization) and 5 (Electrical Characteristics).

Revision G Document (10/2015)

Adds new silicon issues 37 (SPI) and 38 (Power-Saving Mode).

Revision H Document (4/2016)

Modified silicon issue 7 (Output Compare).

Adds new silicon issues 39 (Core), 40 (Core), 41 (I^2C), 42 (I^2C) and 43 (SPI).

Adds new Data Sheet Clarifications 6 (Table 1: dsPIC33EVXXXGM00X/10X Family Devices), 7 (SCK1 Minimum Clock Period), 8 (Register 25-2: CMxCON: Comparator x Control Register) and 9 (Referenced Sources).

Revision J Document (9/2016)

Adds silicon revision AC.

Removes all Data Sheet Clarifications as they were addressed in the new revision of the data sheet.

Revision K Document (1/2017)

Adds silicon revision AB.

Adds silicon issues 44 (SPI), 45 (Output Compare (OC)) and 46 (Output Compare (OC)).

Adds Data Sheet Clarifications 1 (Special Features), 2 (Instruction Set Summary), 3 (10-Bit/12-Bit Analog-to-Digital Converter (ADC)), 4 (Memory Organization) and 5 (Electrical Characteristics).

Revision L Document (8/2017)

Updates silicon issues 1 (CPU) and 2 (CPU).

Adds silicon issue 47 (CPU).

Revision M Document (3/2018)

Updates to Table 1 for 36 pin UQFN devices.

Removes all Data Sheet Clarifications as they are addressed in the new revision of the data sheet.

Revision N Document (7/2018)

Adds data sheet clarifications 1 (Electrical Characteristics).

Revision P Document (10/2018)

Adds silicon issue 48 (I/O).

Revision Q Document (2/2019)

Updates the document for silicon revision **AD.**

Adds data sheet clarification 2 (Electrical Characteristics).

Revision R Document (5/2019)

Adds silicon revision AE.

Removes all Data Sheet Clarifications as they were addressed in the new revision of the data sheet.

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