Product Change Notification - SYST-10NANE953

Date:

14 May 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:



Notification subject:

Data Sheet - dsPIC33EVXXXGM00X/10X Family Data Sheet

Notification text:

SYST-10NANE953

Microchip has released a new DeviceDoc for the dsPIC33EVXXXGM00X/10X Family Data Sheet of devices. If you are using one of these devices please read the document located at dsPIC33EVXXXGM00X/10X Family Data Sheet.

Notification Status: Final

Description of Change: This revision incorporates the following updates: 1) Sections: a) Updated Section 17.1 PWM Faults, Section 34.2 Package Details and Section 29.0 Development Support. 2) Registers: a) Updated Register 21-2 and Register 22-10. 3) Tables: a) Updated Table 1, Table 30-3, Table 30-8, Table 30-11, Table 30-22, Table 31-4 and Table 31-9. 4) Figures: a) Updated Figure 26-1. 5) Added 48-Pin package marking information.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 14 May 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

dsPIC33EVXXXGM00X/10X Family Data Sheet

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Affected Catalog Part Numbers (CPN)

DSPIC33EV128GM102-E/WMV01
DSPIC33EV128GM002-E/MM
DSPIC33EV128GM102-E/MM
DSPIC33EV64GM002-E/MM
DSPIC33EV64GM102-E/MM
DSPIC33EV32GM002-E/MM
DSPIC33EV32GM102-E/MM
DSPIC33EV128GM102-E/MMVAO
DSPIC33EV64GM002-E/MMVAO
DSPIC33EV32GM002-E/MMVAO
DSPIC33EV128GM002-E/SP
DSPIC33EV128GM102-E/SP
DSPIC33EV64GM002-E/SP
DSPIC33EV64GM102-E/SP
DSPIC33EV32GM002-E/SP
DSPIC33EV32GM102-E/SP
DSPIC33EV128GM002-E/SS
DSPIC33EV128GM102-E/SS
DSPIC33EV64GM002-E/SS
DSPIC33EV64GM102-E/SS
DSPIC33EV32GM002-E/SS
DSPIC33EV32GM102-E/SS
DSPIC33EV64GM102-E/SSVAO
DSPIC33EV32GM102-E/SSVAO
DSPIC33EV128GM002-E/SO
DSPIC33EV128GM102-E/SO
DSPIC33EV64GM002-E/SO
DSPIC33EV64GM102-E/SO
DSPIC33EV32GM002-E/SO
DSPIC33EV32GM102-E/SO
DSPIC33EV64GM002-E/SOVAO
DSPIC33EV128GM006-E/MR
DSPIC33EV128GM106-E/MR
DSPIC33EV64GM006-E/MR
DSPIC33EV64GM106-E/MR
DSPIC33EV32GM006-E/MR
DSPIC33EV32GM106-E/MR
DSPIC33EV64GM006-E/MRVAO
DSPIC33EV128GM003-E/M5
DSPIC33EV128GM103-E/M5
DSPIC33EV64GM003-E/M5
DSPIC33EV64GM103-E/M5
DSPIC33EV32GM003-E/M5
DSPIC33EV32GM103-E/M5
DSPIC33EV128GM004-E/ML
DSPIC33EV128GM104-E/ML

DSPIC33EV64GM004-E/ML
DSPIC33EV64GM104-E/ML
DSPIC33EV32GM004-E/ML
DSPIC33EV32GM104-E/ML
DSPIC33EV64GM004-E/MLV02
DSPIC33EV128GM004-E/MLVAO
DSPIC33EV128GM004-E/PT
DSPIC33EV128GM104-E/PT
DSPIC33EV64GM004-E/PT
DSPIC33EV64GM104-E/PT
DSPIC33EV32GM004-E/PT
DSPIC33EV32GM104-E/PT
DSPIC33EV128GM104-E/PTVAO
DSPIC33EV64GM104-E/PTVAO
DSPIC33EV128GM006-E/PT
DSPIC33EV128GM106-E/PT
DSPIC33EV64GM006-E/PT
DSPIC33EV64GM106-E/PT
DSPIC33EV32GM006-E/PT
DSPIC33EV32GM106-E/PT
DSPIC33EV128GM106-E/PTVAO
DSPIC33EV64GM106-E/PTVAO
DSPIC33EV32GM106-E/PTVAO
DSPIC33EV128GM004-E/P8
DSPIC33EV128GM104-E/P8
DSPIC33EV64GM004-E/P8
DSPIC33EV64GM104-E/P8
DSPIC33EV32GM004-E/P8
DSPIC33EV32GM104-E/P8
DSPIC33EV128GM002-I/MM
DSPIC33EV128GM102-I/MM
DSPIC33EV64GM002-I/MM
DSPIC33EV64GM102-I/MM
DSPIC33EV32GM002-I/MM
DSPIC33EV32GM102-I/MM
DSPIC33EV128GM002-I/SP
DSPIC33EV128GM102-I/SP
DSPIC33EV64GM002-I/SP
DSPIC33EV64GM102-I/SP
DSPIC33EV32GM002-I/SP
DSPIC33EV32GM102-I/SP
DSPIC33EV128GM002-I/SS
DSPIC33EV128GM102-I/SS
DSPIC33EV64GM002-I/SS
DSPIC33EV64GM102-I/SS
DSPIC33EV32GM002-I/SS
DSPIC33EV32GM102-I/SS
DSPIC33EV32GM002-I/SSVAO
DSPIC33EV32GM102-I/SSVAO

DSPIC33EV128GM002-I/SO
DSPIC33EV128GM102-I/SO
DSPIC33EV64GM002-I/SO
DSPIC33EV64GM102-I/SO
DSPIC33EV32GM002-I/SO
DSPIC33EV32GM102-I/SO
DSPIC33EV128GM006-I/MR
DSPIC33EV128GM106-I/MR
DSPIC33EV64GM006-I/MR
DSPIC33EV64GM106-I/MR
DSPIC33EV32GM006-I/MR
DSPIC33EV32GM106-I/MR
DSPIC33EV64GM006-I/MRVAO
DSPIC33EV128GM003-I/M5
DSPIC33EV128GM103-I/M5
DSPIC33EV64GM003-I/M5
DSPIC33EV64GM103-I/M5
DSPIC33EV32GM003-I/M5
DSPIC33EV32GM103-I/M5
DSPIC33EV128GM004-I/ML
DSPIC33EV128GM104-I/ML
DSPIC33EV64GM004-I/ML
DSPIC33EV64GM104-I/ML
DSPIC33EV32GM004-I/ML
DSPIC33EV32GM104-I/ML
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DSPIC33EV64GM104-I/PT
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DSPIC33EV64GM004-I/PTVAO
DSPIC33EV64GM104-I/PTVAO
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DSPIC33EV128GM106-I/PT
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DSPIC33EV64GM106-I/PT
DSPIC33EV32GM006-I/PT
DSPIC33EV32GM106-I/PT
DSPIC33EV64GM006-I/PTVAO
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DSPIC33EV64GM104-I/P8
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DSPIC33EV128GM102-H/MM
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DSPIC33EV128GM102-H/SP
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DSPIC33EV32GM006-H/PT
DSPIC33EV32GM106-H/PT
DSPIC33EV128GM004-H/P8
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DSPIC33EV64GM004-H/P8
DSPIC33EV64GM104-H/P8
DSPIC33EV32GM004-H/P8
DSPIC33EV32GM104-H/P8
DSPIC33EV256GM002-E/MM
DSPIC33EV256GM102-E/MM
DSPIC33EV256GM002-E/MMVAO
DSPIC33EV256GM102-E/MMVAO
DSPIC33EV256GM002-E/SP
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DSPIC33EV256GM002-E/SS
DSPIC33EV256GM102-E/SS
DSPIC33EV256GM002-E/SO
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DSPIC33EV256GM102-I/MM
DSPIC33EV256GM002-I/SP
DSPIC33EV256GM102-I/SP
DSPIC33EV256GM102-I/SPREL

DSPIC33EV256GM002-I/SS
DSPIC33EV256GM102-I/SS
DSPIC33EV256GM002-I/SO
DSPIC33EV256GM102-I/SO
DSPIC33EV256GM006-I/MR
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DSPIC33EV256GM003-I/M5
DSPIC33EV256GM103-I/M5
DSPIC33EV256GM004-I/ML
DSPIC33EV256GM104-I/ML
DSPIC33EV256GM104-I/MLVAO
DSPIC33EV256GM004-I/PT
DSPIC33EV256GM104-I/PT
DSPIC33EV256GM006-I/PT
DSPIC33EV256GM106-I/PT
DSPIC33EV256GM106-I/PTREL
DSPIC33EV256GM106-I/PTVAO
DSPIC33EV256GM004-I/P8
DSPIC33EV256GM104-I/P8
DSPIC33EV256GM002-H/MM
DSPIC33EV256GM102-H/MM
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DSPIC33EV256GM102-H/SP
DSPIC33EV256GM002-H/SS
DSPIC33EV256GM102-H/SS
DSPIC33EV256GM102-H/SSVAO
DSPIC33EV256GM002-H/SO
DSPIC33EV256GM102-H/SO
DSPIC33EV256GM006-H/MR
DSPIC33EV256GM106-H/MR
DSPIC33EV256GM003-H/M5
DSPIC33EV256GM103-H/M5
DSPIC33EV256GM004-H/ML
DSPIC33EV256GM104-H/ML
DSPIC33EV256GM004-H/PT
DSPIC33EV256GM104-H/PT
DSPIC33EV256GM006-H/PT
DSPIC33EV256GM106-H/PT
DSPIC33EV256GM004-H/P8
DSPIC33EV256GM104-H/P8

dsPIC33EVXXXGM00X/10X FAMILY

16-Bit, 5V Digital Signal Controllers with PWM, SENT, Op Amps and Advanced Analog Features

Operating Conditions

- 4.5V to 5.5V, 0°C to +85°C, DC to 70 MIPS
- 4.5V to 5.5V, -40°C to +125°C, DC to 60 MIPS
- 4.5V to 5.5V, -40°C to +150°C, DC to 40 MIPS

Core: 16-Bit dsPIC33E CPU

- Code-Efficient (C and Assembly) Architecture
- 16-Bit Wide Data Path
- Two 40-Bit Wide Accumulators
- Single-Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support
- Intermediate Security for Memory:
  - Provides a Boot Flash Segment in addition to the existing General Flash Segment
- Error Code Correction (ECC) for Flash
- Added Two Alternate Register Sets for Fast Context Switching

Clock Management

- Internal, 15% Low-Power RC (LPRC) – 32 kHz
- Internal, 1% Fast RC (FRC) – 7.37 MHz
- Internal, 10% Backup FRC (BFRC) – 7.37 MHz
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Additional FSCM Source (BFRC), Intended to Provide a Clock Fail Switch Source for the System Clock
- Independent Watchdog Timer (WDT)
- System Windowed Watchdog Timer (DMT)
- Fast Wake-up and Start-up

Power Management

- Low-Power Management modes (Sleep, Idle and Doze)
- Power Consumption Minimized Executing `NOP` String
- Integrated Power-on Reset (POR) and Brown-out Reset (BOR)
- 0.5 mA/MHz Dynamic Current (typical)
- 50 µA at +25°C I_{PD} Current (typical)

PWM

- Up to Six Pulse-Width Modulation (PWM) Outputs (three generators)
- Primary Master Time Base Inputs allow Time Base Synchronization from Internal/External Sources
- Dead Time for Rising and Falling Edges
- 7.14 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, inverters, Power Factor Correction (PFC) and lighting
  - Brushless Direct Current (BLDC), Permanent Magnet Synchronous Motor (PMSM), AC Induction Motor (ACIM), Switched Reluctance Motor (SRM)
  - Programmable Fault inputs
  - Flexible trigger configurations for Analog-to-Digital conversion
  - Supports PWM lock, PWM output chopping and dynamic phase shifting

Advanced Analog Features

- ADC module:
  - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - Up to 36 analog inputs
- Flexible and Independent ADC Trigger Sources
- Up to Four Op Amp/Comparators with Direct Connection to the ADC module:
  - Additional dedicated comparator and 7-bit Digital-to-Analog Converter (DAC)
  - Two comparator voltage reference outputs
  - Programmable references with 128 voltage points
  - Programmable blanking and filtering
- Charge Time Measurement Unit (CTMU):
  - Supports mTouch® capacitive touch sensing
  - Provides high-resolution time measurement (1 ns)
  - On-chip temperature measurement
  - Temperature sensor diode
  - Nine sources of edge input triggers (CTED1, CTED2, OCPWM, TMR1, SYSCLK, OSCLK, FRC, BFRC and LPRC)

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Timers/Output Compare/Input Capture

- Nine General Purpose Timers:
  - Five 16-bit and up to two 32-bit timers/counters; Timer3 can provide ADC trigger
- Four Output Compare modules Configurable as Timers/Counters
- Four Input Capture modules

Communication Interfaces

- Two Enhanced Addressable Universal Asynchronous Receiver/Transmitter (UART) modules (6.25 Mbps):
  - With support for LIN/J2602 bus and IrDA®
  - High and low speed (SCI)
- Two SPI modules (15 MHz):
  - 25 MHz data rate without using PPS
- One I^2C module (up to 1 Mbaud) with SMBus Support
- Two SENT J2716 (Single-Edge Nibble Transmission-Transmit/Receive) module for Automotive Applications
- One CAN module:
  - 32 buffers, 16 filters and 3 masks

Direct Memory Access (DMA)

- Four-Channel DMA with User-Selectable Priority Arbitration
- UART, Serial Peripheral Interface (SPI), ADC, Input Capture, Output Compare and Controller Area Network (CAN)

Input/Output

- GPIO Registers to Support Selectable Slew Rate I/Os
- Peripheral Pin Select (PPS) to allow Function Remap
- Sink/Source: 8 mA or 12 mA, Pin-Specific for Standard V_{OH}/V_{OL}
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Change Notice Interrupts on All I/O Pins

Qualification and Class B Support

- AEC-Q100 REVG (Grade 1: -40°C to +125°C) Compliant
- AEC-Q100 REVG (Grade 0: -40°C to +150°C) Compliant
- Class B Safety Library, IEC 60730

Class B Fault Handling Support

- Backup FRC
- Windowed WDT uses LPRC
- Windowed Deadman Timer (DMT) uses System Clock (System Windowed Watchdog Timer)
- H/W Clock Monitor Circuit
- Oscillator Frequency Monitoring through CTMU (OSCI, SYSCLK, FRC, BFRC, LPRC)
- Dedicated PWM Fault Pin
- Lockable Clock Configuration

Debugger Development Support

- In-Circuit and In-Application Programming
- Three Complex and Five Simple Breakpoints
- Trace and Run-Time Watch

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dsPIC33EVXXXGM00X/10X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1. The following pages show the devices' pinout diagrams.

TABLE 1: dsPIC33EVXXXGM00X/10X FAMILY DEVICES

Device	Program Memory Bytes	SRAM Bytes	CAN	DMA Channels	16-Bit Timers (T1)	32-Bit Timers	Input Capture	Output Compare	PWM	UART	SPI	I^2C	SENT	10/12-Bit ADC	ADC Inputs	Op Amp/Comparators	CTMU	Security	Peripheral Pin Select (PPS)	General Purpose I/O (GPIO)	External Interrupts	Pins
dsPIC33EV32GM002	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	11	3/4	1	Intermediate	Y	21	3	28
dsPIC33EV32GM102			1																			
dsPIC33EV64GM002	64K	8K	0																			
dsPIC33EV64GM102			1																			
dsPIC33EV128GM002	128K	8K	0																			
dsPIC33EV128GM102			1																			
dsPIC33EV256GM002	256K	16K	0																			
dsPIC33EV256GM102			1																			
dsPIC33EV32GM003	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	13	3/4	1	Intermediate	Y	25	3	36
dsPIC33EV32GM103			1																			
dsPIC33EV64GM003	64K	8K	0																			
dsPIC33EV64GM103			1																			
dsPIC33EV128GM003	128K	8K	0																			
dsPIC33EV128GM103			1																			
dsPIC33EV256GM003	256K	16K	0																			
dsPIC33EV256GM103			1																			
dsPIC33EV32GM004	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	24	4/5	1	Intermediate	Y	35	3	44, 48
dsPIC33EV32GM104			1																			
dsPIC33EV64GM004	64K	8K	0																			
dsPIC33EV64GM104			1																			
dsPIC33EV128GM004	128K	8K	0																			
dsPIC33EV128GM104			1																			
dsPIC33EV256GM004	256K	16K	0																			
dsPIC33EV256GM104			1																			

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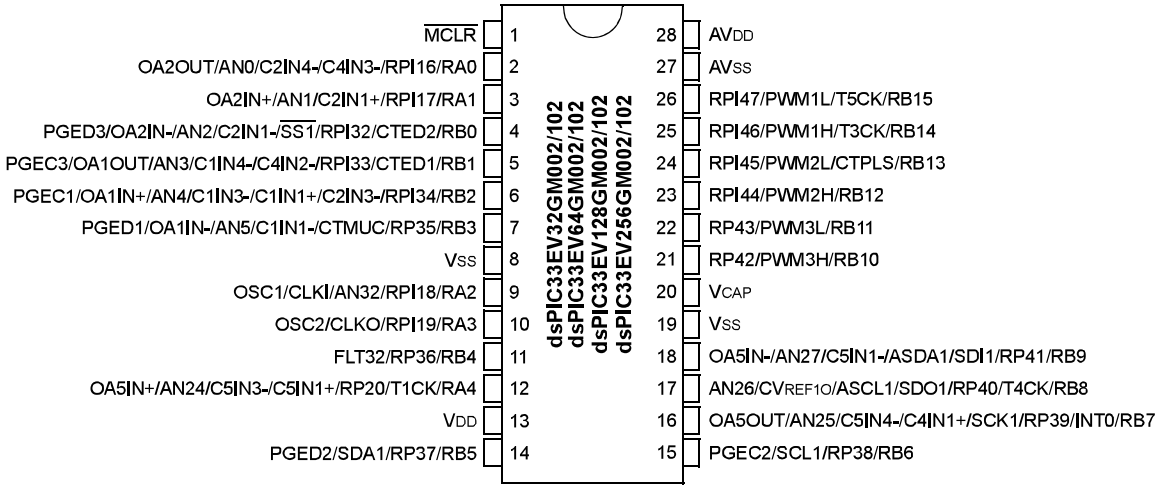
TABLE 1: dsPIC33EVXXXGM00X/10X FAMILY DEVICES (CONTINUED)

Device	Program Memory Bytes	SRAM Bytes	CAN	DMA Channels	16-Bit Timers (T1)	32-Bit Timers	Input Capture	Output Compare	PWM	UART	SPI	I^2C	SENT	10/12-Bit ADC	ADC Inputs	Op Amp/Comparators	CTMU	Security	Peripheral Pin Select (PPS)	General Purpose I/O (GPIO)	External Interrupts	Pins
dsPIC33EV32GM006	32K	4K	0	4	5	2	4	4	3x2	2	2	1	2	1	36	4/5	1	Intermediate	Y	53	3	64
dsPIC33EV32GM106			1																			
dsPIC33EV64GM006	64K	8K	0																			
dsPIC33EV64GM106			1																			
dsPIC33EV128GM006	128K	8K	0																			
dsPIC33EV128GM106			1																			
dsPIC33EV256GM006	256K	16K	0																			
dsPIC33EV256GM106			1																			

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Pin Diagrams

28-Pin SPDIP/SOIC/SSOP(1,2,3)



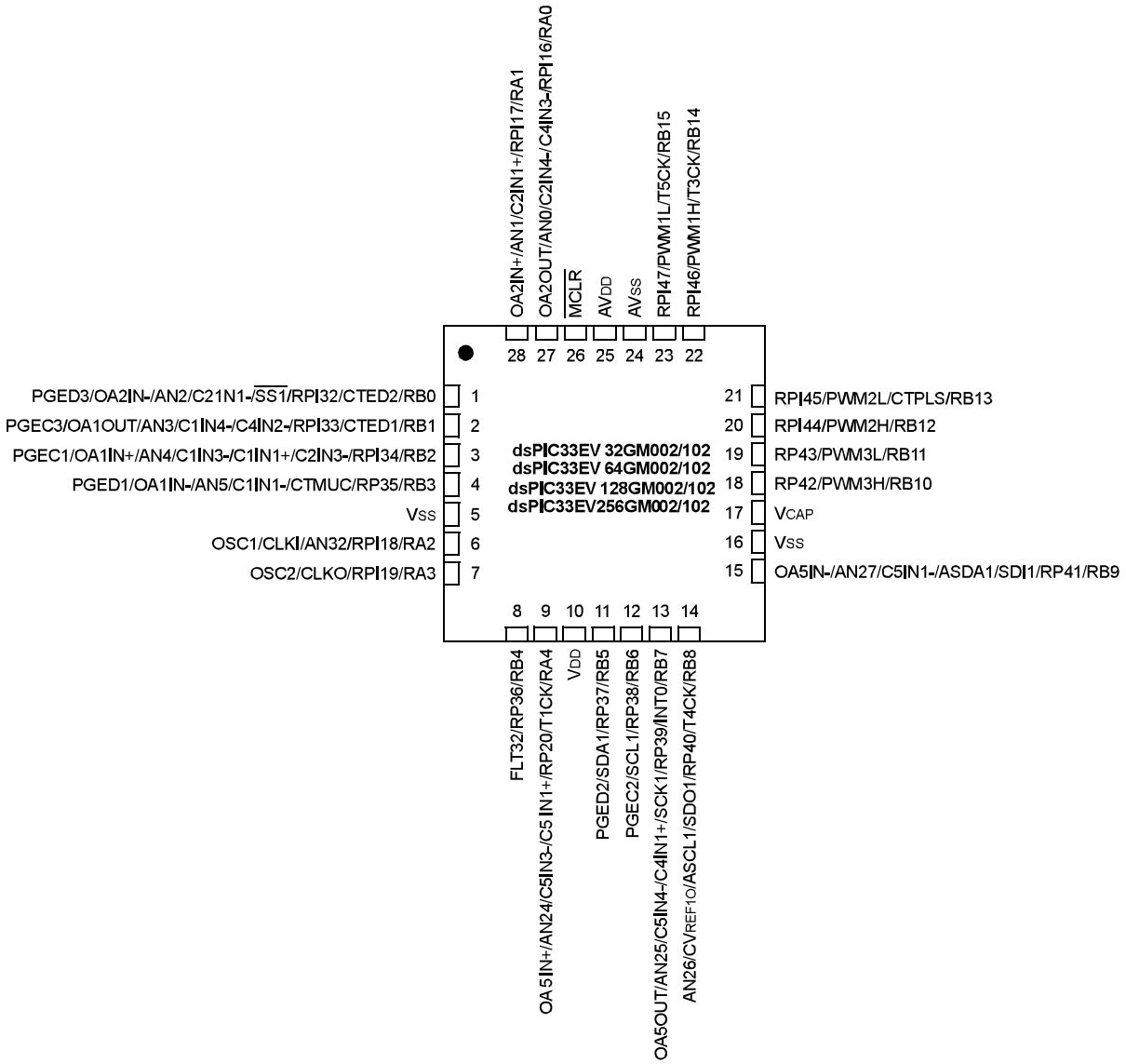
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

Pin Diagrams (Continued)

28-Pin QFN-S(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

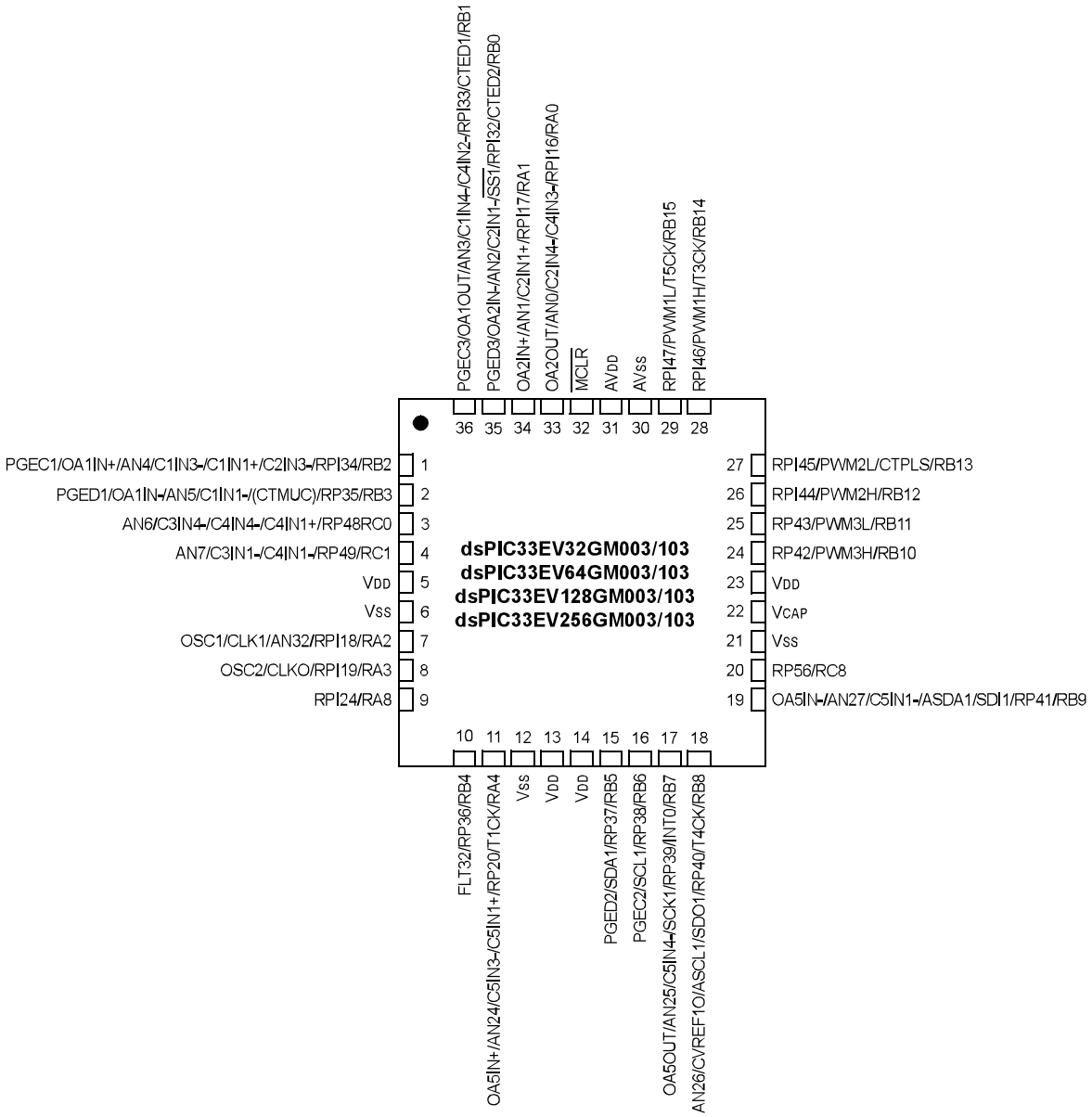
3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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Pin Diagrams (Continued)

36-Pin UQFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

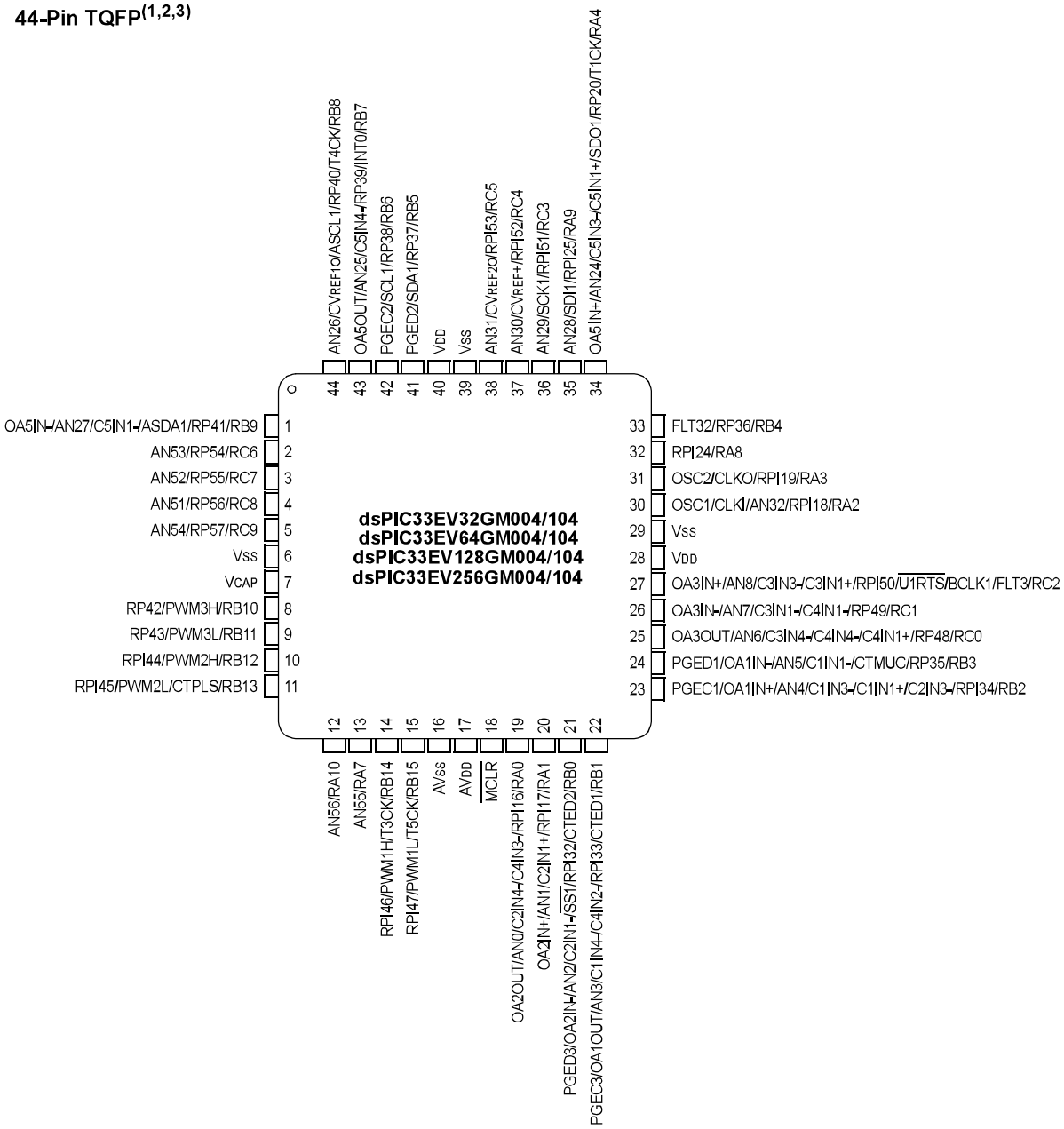
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

44-Pin TQFP(1,2,3)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

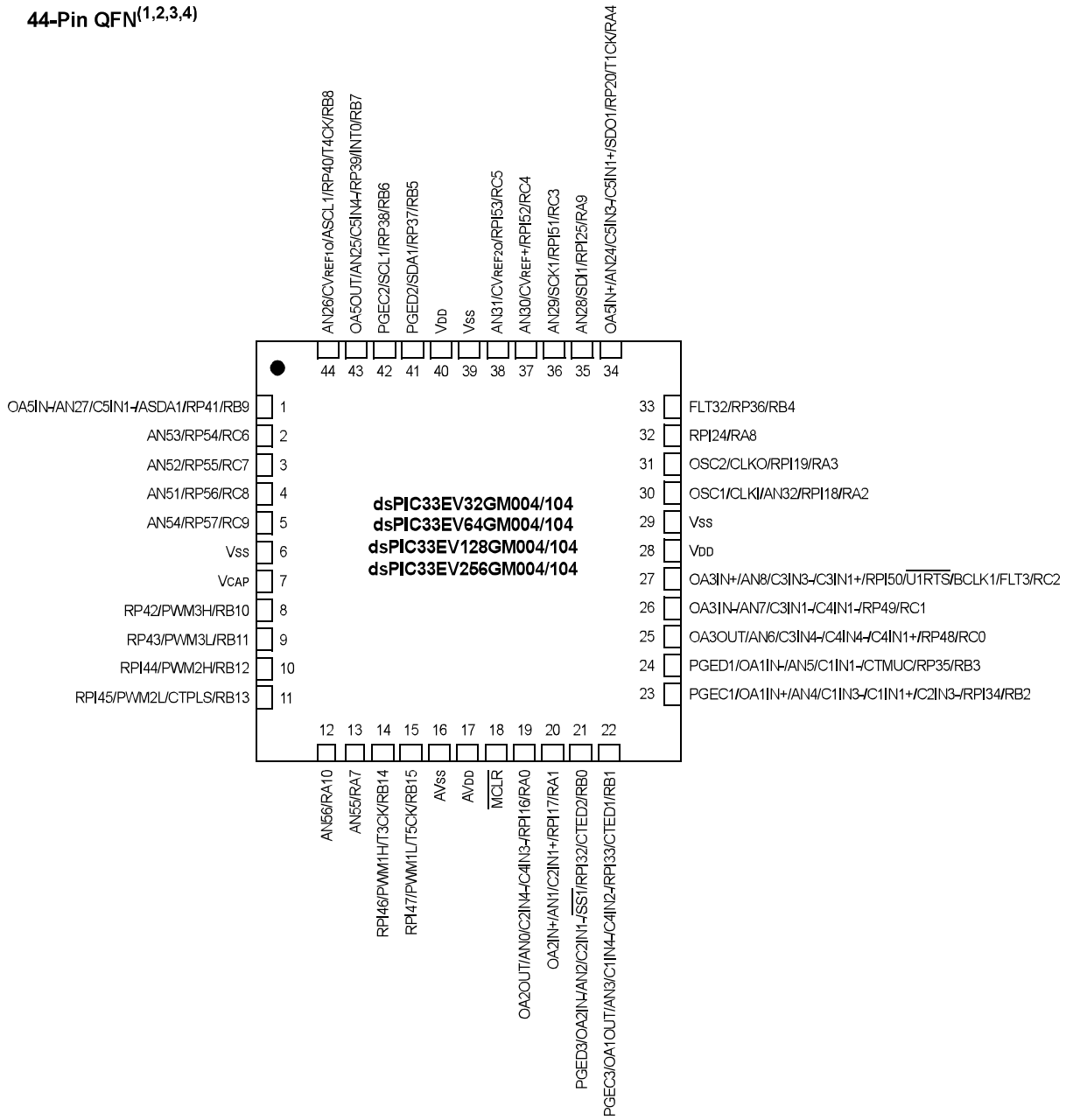
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

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Pin Diagrams (Continued)

44-Pin QFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

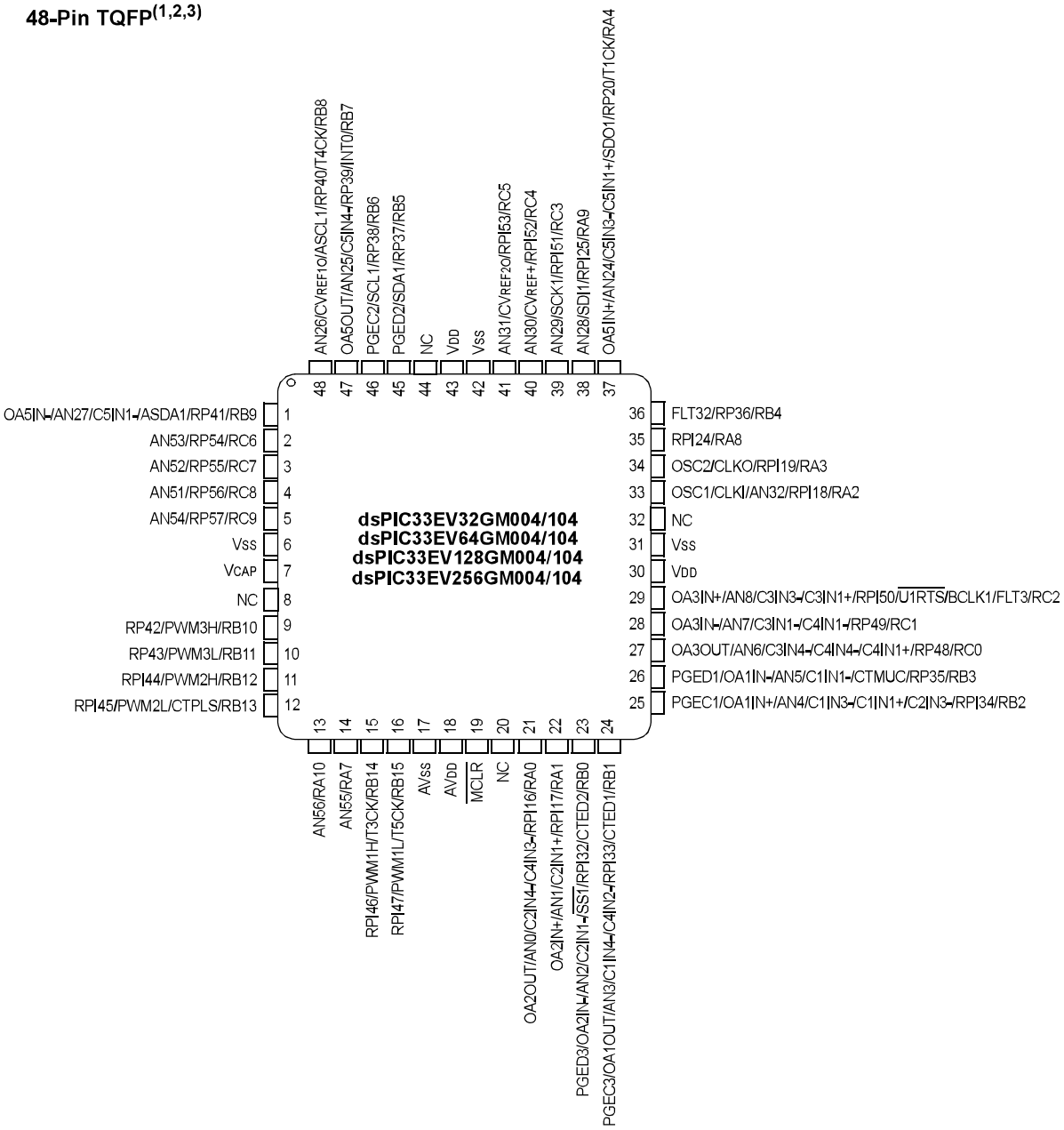
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

Pin Diagrams (Continued)

48-Pin TQFP(1,2,3)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

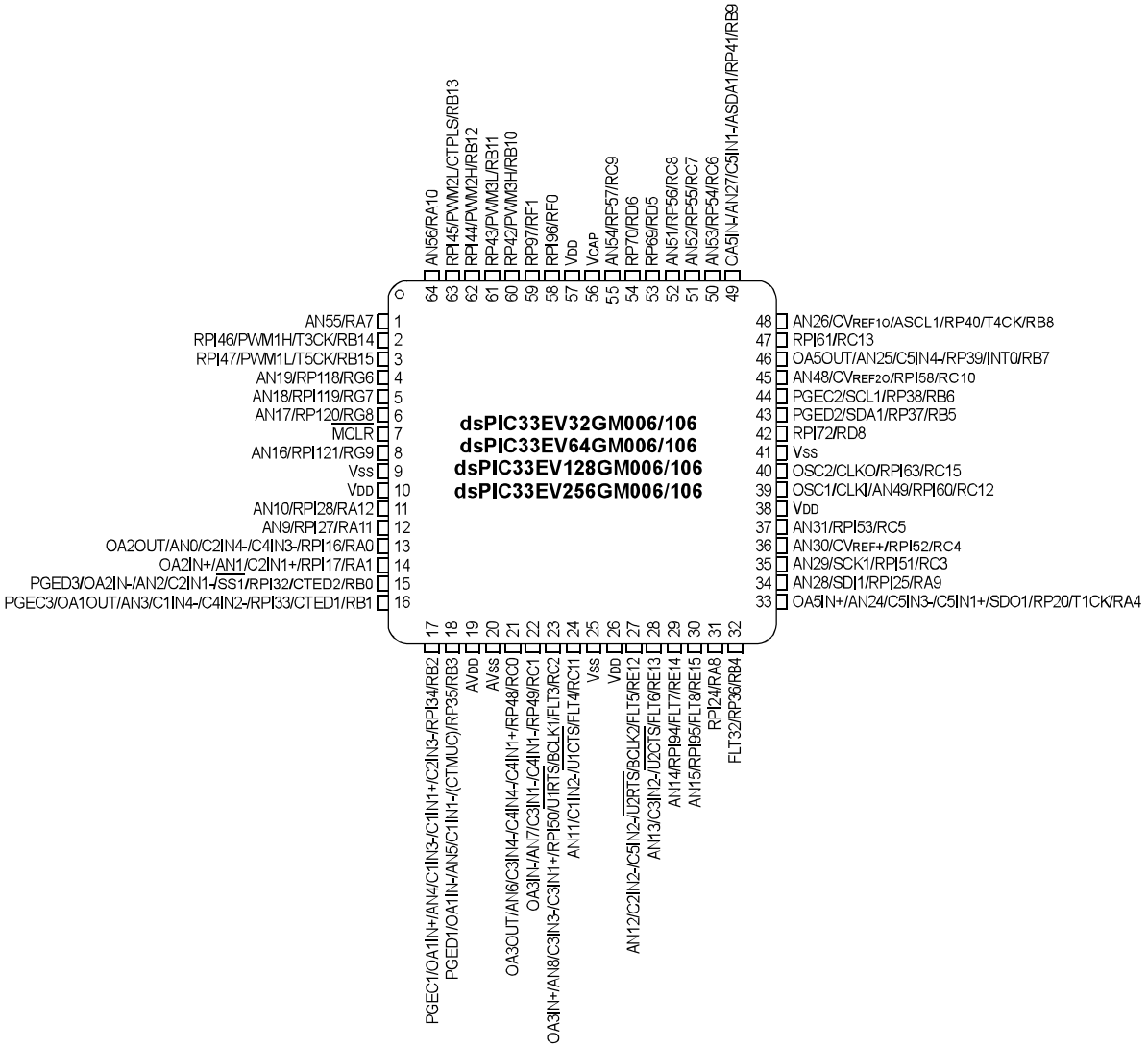
2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

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Pin Diagrams (Continued)

64-Pin TQFP(1,2,3)



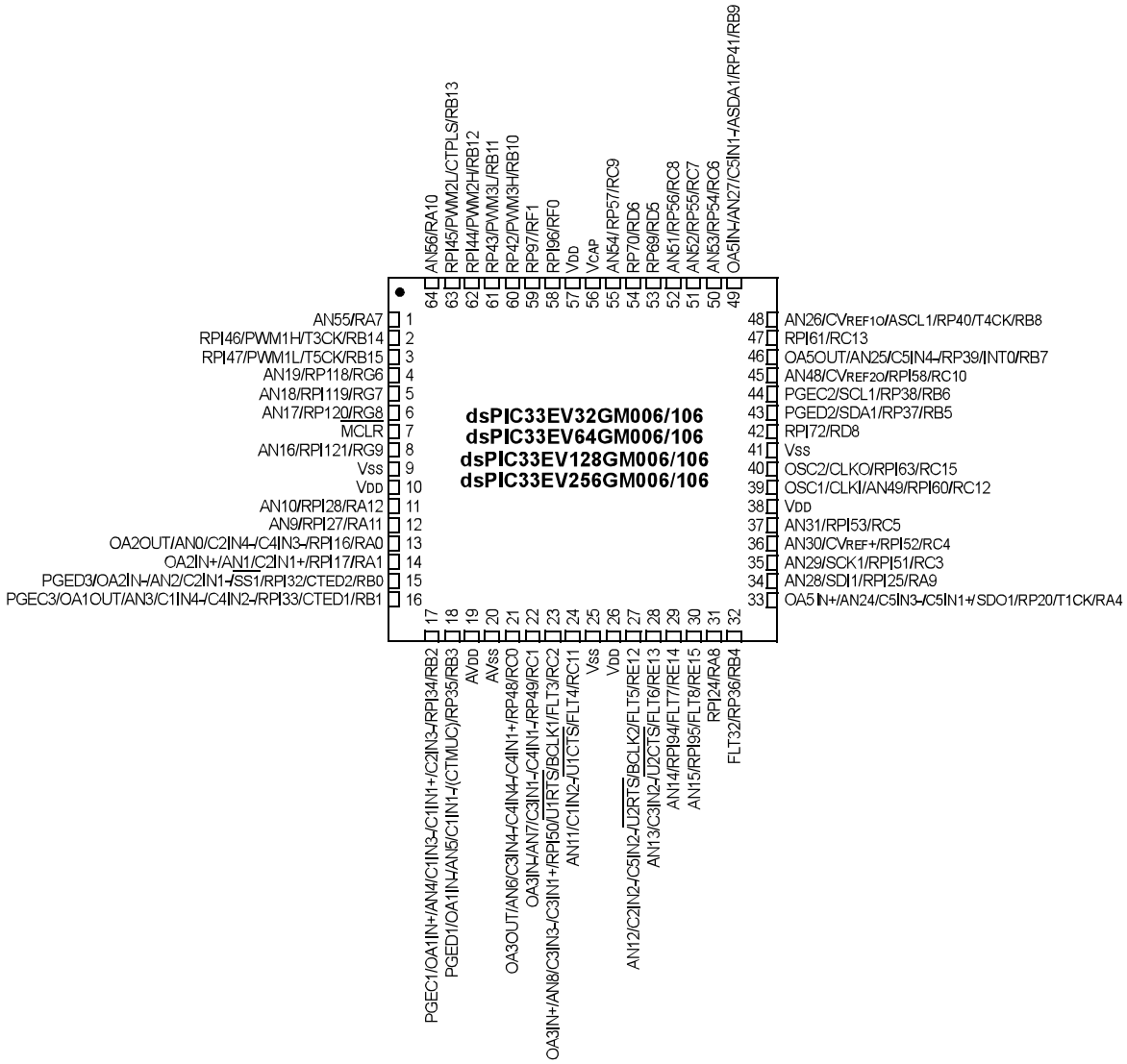
Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

Pin Diagrams (Continued)

64-Pin QFN(1,2,3,4)



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.5 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: If the op amp is selected when OPAEN (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

4: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*, which are available from the Microchip website (www.microchip.com). The following documents should be considered as the general reference for the operation of a particular module or device feature:

- **"Introduction"** (www.microchip.com/DS70573)
- **"CPU"** (www.microchip.com/DS70359)
- **"Data Memory"** (www.microchip.com/DS70595)
- **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613)
- **"Flash Programming"** (www.microchip.com/DS70000609)
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- **"Timers"** (www.microchip.com/DS70362)
- **"CodeGuard™ Intermediate Security"** (www.microchip.com/DS70005182)
- **"Deadman Timer"** (www.microchip.com/DS70005155)
- **"Input Capture with Dedicated Timer"** (www.microchip.com/DS70000352)
- **"Output Compare with Dedicated Timer"** (www.microchip.com/DS70005159)
- **"High-Speed PWM"** (www.microchip.com/DS70645)
- **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621)
- **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582)
- **"Serial Peripheral Interface (SPI)"** (www.microchip.com/DS70005185)
- **"Inter-Integrated Circuit (I^2C)"** (www.microchip.com/DS70000195)
- **"Enhanced Controller Area Network (ECAN™)"** (www.microchip.com/DS70353)
- **"Direct Memory Access (DMA)"** (www.microchip.com/DS70348)
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- **"Op Amp/Comparator"** (www.microchip.com/DS70000357)
- **"Device Configuration"** (www.microchip.com/DS70000618)
- **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (www.microchip.com/DS30009743)
- **"Single-Edge Nibble Transmission (SENT) Module"** (www.microchip.com/DS70005145)

NOTES:

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1.0 DEVICE OVERVIEW

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).

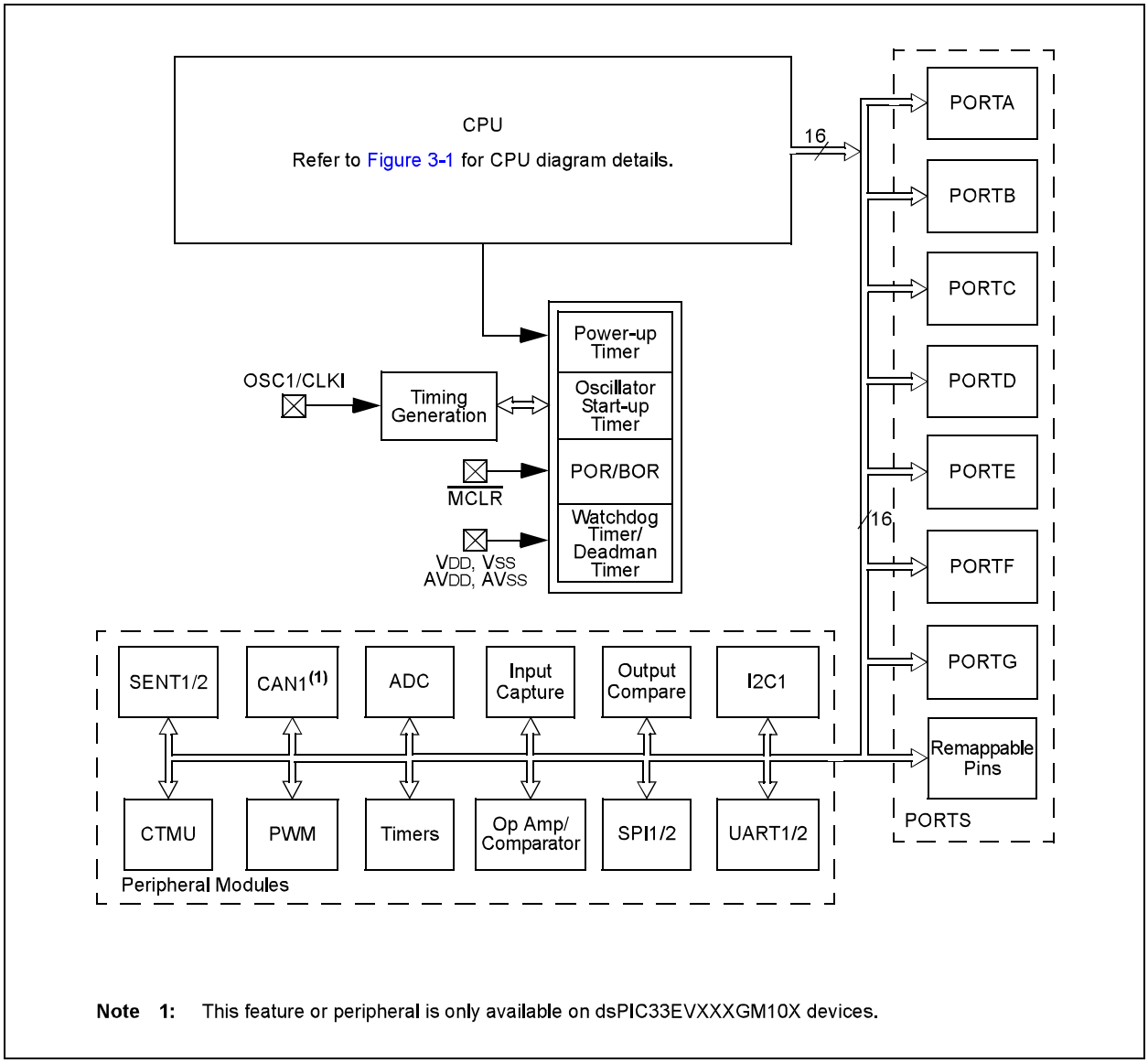
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EVXXXGM00X/10X family Digital Signal Controller (DSC) devices.

dsPIC33EVXXXGM00X/10X family devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

FIGURE 1-1: dsPIC33EVXXXGM00X/10X FAMILY BLOCK DIAGRAM



Note 1: This feature or peripheral is only available on dsPIC33EVXXXGM10X devices.

TABLE 1-1: PINOUT I/O DESCRIPTIONS

Pin Name	Pin Type	Buffer Type	PPS	Description
AN0-AN19 AN24-AN32 AN48, AN49 AN51-AN56	I	Analog	No	Analog input channels.
CLKI	I	ST/ CMOS	No	External clock source input. Always associated with OSC1 pin function.
CLKO	O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function.
OSC1	I	ST/ CMOS	No	Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.
OSC2	I/O	—	No	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes.
REFCLKO	O	—	Yes	Reference clock output.
IC1-IC4	I	ST	Yes	Capture Inputs 1 to 4.
OCFA	I	ST	Yes	Compare Fault A input (for compare channels).
OC1-OC4	O	—	Yes	Compare Outputs 1 to 4.
INT0	I	ST	No	External Interrupt 0.
INT1	I	ST	Yes	External Interrupt 1.
INT2	I	ST	Yes	External Interrupt 2.
RA0-RA4, RA7-RA12	I/O	ST	Yes	PORTA is a bidirectional I/O port.
RB0-RB15	I/O	ST	Yes	PORTB is a bidirectional I/O port.
RC0-RC13, RC15	I/O	ST	Yes	PORTC is a bidirectional I/O port.
RD5-RD6, RD8	I/O	ST	Yes	PORTD is a bidirectional I/O port.
RE12-RE15	I/O	ST	Yes	PORTE is a bidirectional I/O port.
RF0-RF1	I/O	ST	No	PORTF is a bidirectional I/O port.
RG6-RG9	I/O	ST	Yes	PORTG is a bidirectional I/O port.
T1CK	I	ST	No	Timer1 external clock input.
T2CK	I	ST	Yes	Timer2 external clock input.
T3CK	I	ST	No	Timer3 external clock input.
T4CK	I	ST	No	Timer4 external clock input.
T5CK	I	ST	No	Timer5 external clock input.
CTPLS	O	ST	No	CTMU pulse output.
CTED1	I	ST	No	CTMU External Edge Input 1.
CTED2	I	ST	No	CTMU External Edge Input 2.
$\overline{\text{U1CTS}}$	I	ST	Yes	UART1 Clear-to-Send.
$\overline{\text{U1RTS}}$	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
$\overline{\text{U2CTS}}$	I	ST	Yes	UART2 Clear-to-Send.
$\overline{\text{U2RTS}}$	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
$\overline{\text{SS1}}$	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

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TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
$\overline{SS2}$	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
C1RX	I	ST	Yes	CAN1 bus receive pin.
C1TX	O	—	Yes	CAN1 bus transmit pin.
SENT1TX	O	—	Yes	SENT1 transmit pin.
SENT1RX	I	—	Yes	SENT1 receive pin.
SENT2TX	O	—	Yes	SENT2 transmit pin.
SENT2RX	I	—	Yes	SENT2 receive pin.
CVREF	O	Analog	No	Comparator Voltage Reference output.
C1IN1+, C1IN2-, C1IN1-, C1IN3-	I	Analog	No	Comparator 1 inputs.
C1OUT	O	—	Yes	Comparator 1 output.
C2IN1+, C2IN2-, C2IN1-, C2IN3-	I	Analog	No	Comparator 2 inputs.
C2OUT	O	—	Yes	Comparator 2 output.
C3IN1+, C3IN2-, C2IN1-, C3IN3-	I	Analog	No	Comparator 3 inputs.
C3OUT	O	—	Yes	Comparator 3 output.
C4IN1+, C4IN2-, C4IN1-, C4IN3-	I	Analog	No	Comparator 4 inputs.
C4OUT	O	—	Yes	Comparator 4 output.
C5IN1+, C5IN2-, C5IN1-, C5IN3-	I	Analog	No	Comparator 5 inputs.
C5OUT	O	—	Yes	Comparator 5 output.
FLT1-FLT2	I	ST	Yes	PWM Fault Inputs 1 and 2.
FLT3-FLT8	I	ST	NO	PWM Fault Inputs 3 to 8.
FLT32	I	ST	NO	PWM Fault Input 32.
DTCMP1-DTCMP3	I	ST	Yes	PWM Dead-Time Compensation Inputs 1 to 3.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 to 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 to 3.
SYNCI1	I	ST	Yes	PWM Synchronization Input 1.
SYNCO1	O	—	Yes	PWM Synchronization Output 1.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
AVDD	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AVSS	P	P	No	Ground reference for analog modules.
VDD	P	—	No	Positive supply for peripheral logic and I/O pins.
VCAP	P	—	No	CPU logic filter capacitor connection.
VSS	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output
Analog = Analog input
P = Power
ST = Schmitt Trigger input with CMOS levels
O = Output
I = Input
PPS = Peripheral Pin Select
TTL = TTL input buffer

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2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

2.1 Basic Connection Requirements

Getting started with the dsPIC33EVXXXGM00X/10X family of 16-bit microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins
  (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used)
  (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP
  (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin
  (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes
  (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used
  (see **Section 2.6 "External Oscillator Pins"**)

Note: The AVDD and AVSS pins must be connected, regardless of the ADC voltage reference source.

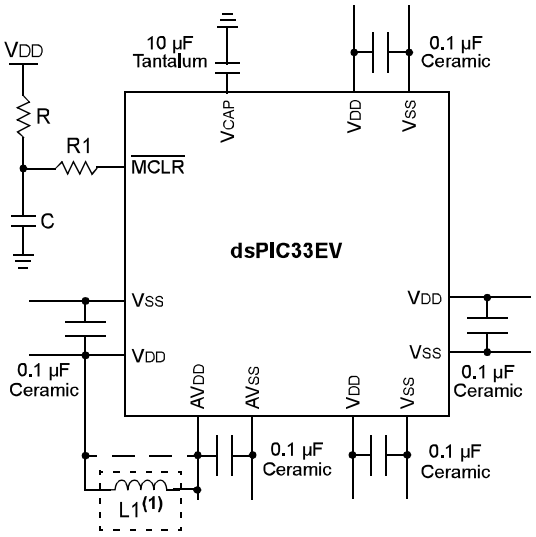
2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS, is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10V-20V is recommended. This capacitor should be a Low Equivalent Series Resistance (low-ESR), and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the Printed Circuit Board (PCB):** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing the PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{FCNV}{2} \quad \text{(i.e., ADC Conversion Rate/2)}$$

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (<1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the internal voltage regulator output. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 µF (10 µF is recommended), with at least a 16V rating connected to the ground. The type can be ceramic or tantalum. See **Section 30.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length should not exceed one-quarter inch (6 mm).

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

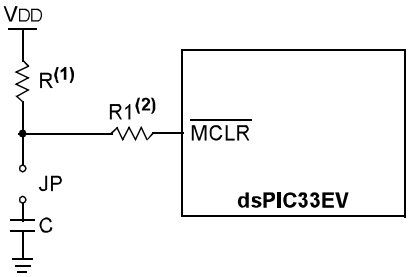
- Device Reset
- Device Programming and Debugging

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-1, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flow into MCLR from the external capacitor, C, in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

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2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not exceeding 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip website (www.microchip.com).

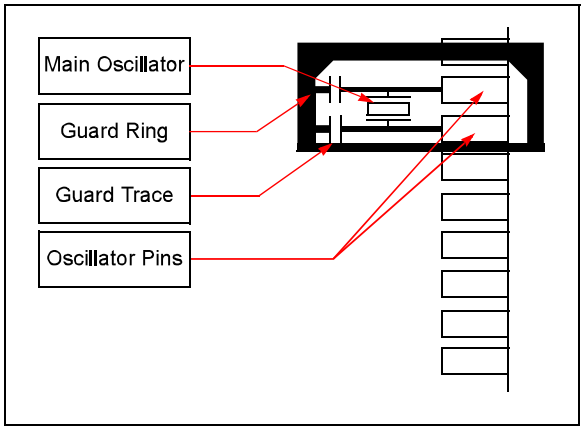
- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"MPLAB® ICD 3 Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* (DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For more information, see **Section 9.0 "Oscillator Configuration"**.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed as shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 5 MHz < F_{IN} < 13.6 MHz to comply with device PLL start-up conditions. This intends that, if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source.

Note:	Clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between Vss and unused pins, and drive the output to logic low.

NOTES:

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3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CPU"** (www.microchip.com/DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EVXXXGM00X/10X family devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a Data, Address or Address Offset register. The sixteenth Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

In addition, the dsPIC33EVXXXGM00X/10X devices include two alternate Working register sets, which consist of W0 through W14. The alternate registers can be made persistent to help reduce the saving and restoring of register content during Interrupt Service Routines (ISRs). The alternate Working registers can be assigned to a specific Interrupt Priority Level (IPL1 through IPL6) by configuring the CTXTx[2:0] bits in the FALTREG Configuration register.

The alternate Working registers can also be accessed manually by using the `CTXTSWP` instruction.

The CCTXI[2:0] and MCTXI[2:0] bits in the CTXTSTAT register can be used to identify the current, and most recent, manually selected Working register sets.

3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EV devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space (DS) memory map can optionally be mapped into Program Space (PS) at any 16K program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. For more information on EDS, PSV and table accesses, refer to **"Data Memory"** (www.microchip.com/DS70595) and **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*.

On dsPIC33EV devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms. Figure 3-1 illustrates the block diagram of the dsPIC33EVXXXGM00X/10X family devices.

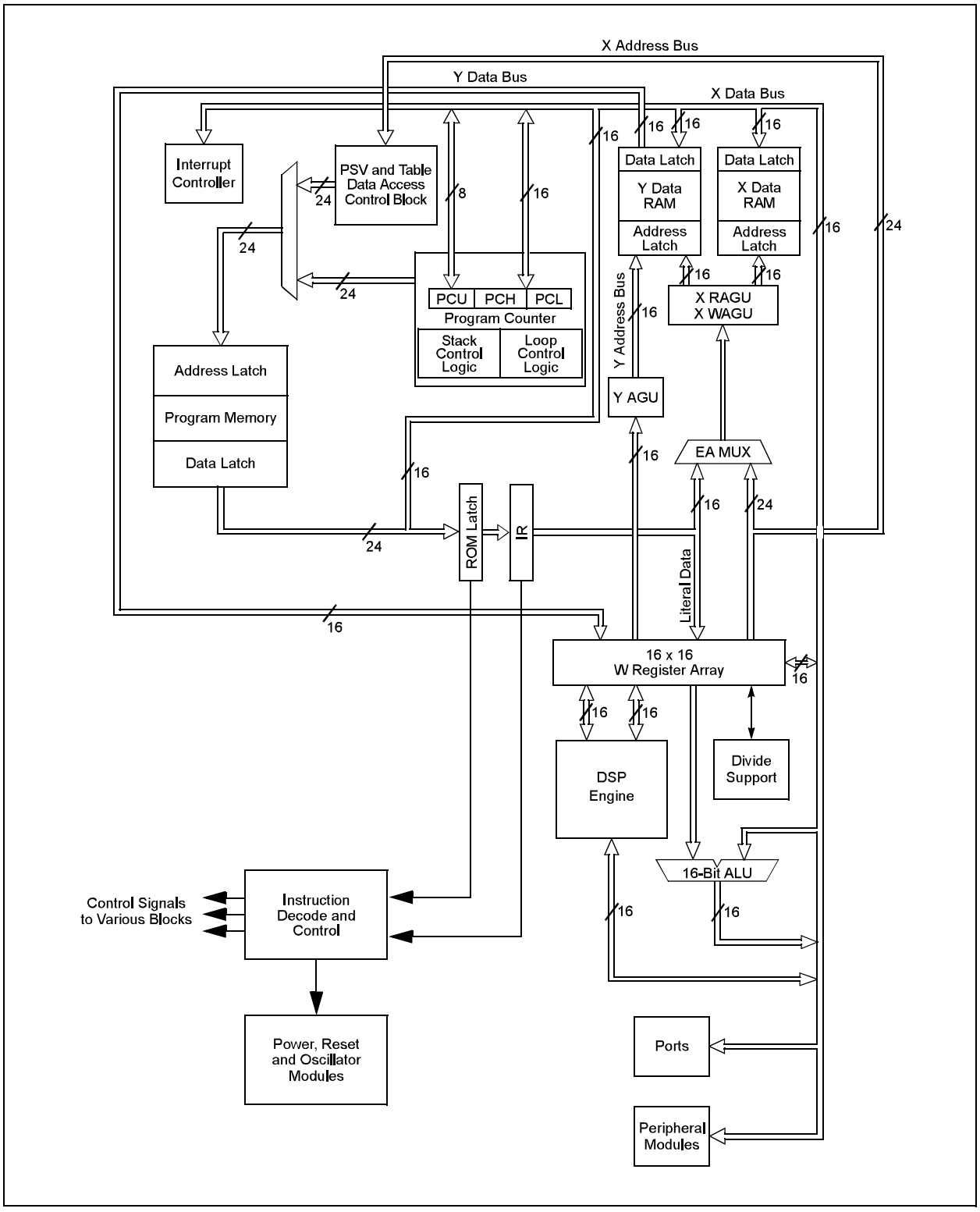
3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

FIGURE 3-1: dsPIC33EVXXXGM00X/10X FAMILY CPU BLOCK DIAGRAM



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3.5 Programmer's Model

The programmer's model for the dsPIC33EVXXXGM00X/10X family is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EVXXXGM00X/10X family devices contain control registers for Modulo Addressing and Bit-Reversed Addressing, and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

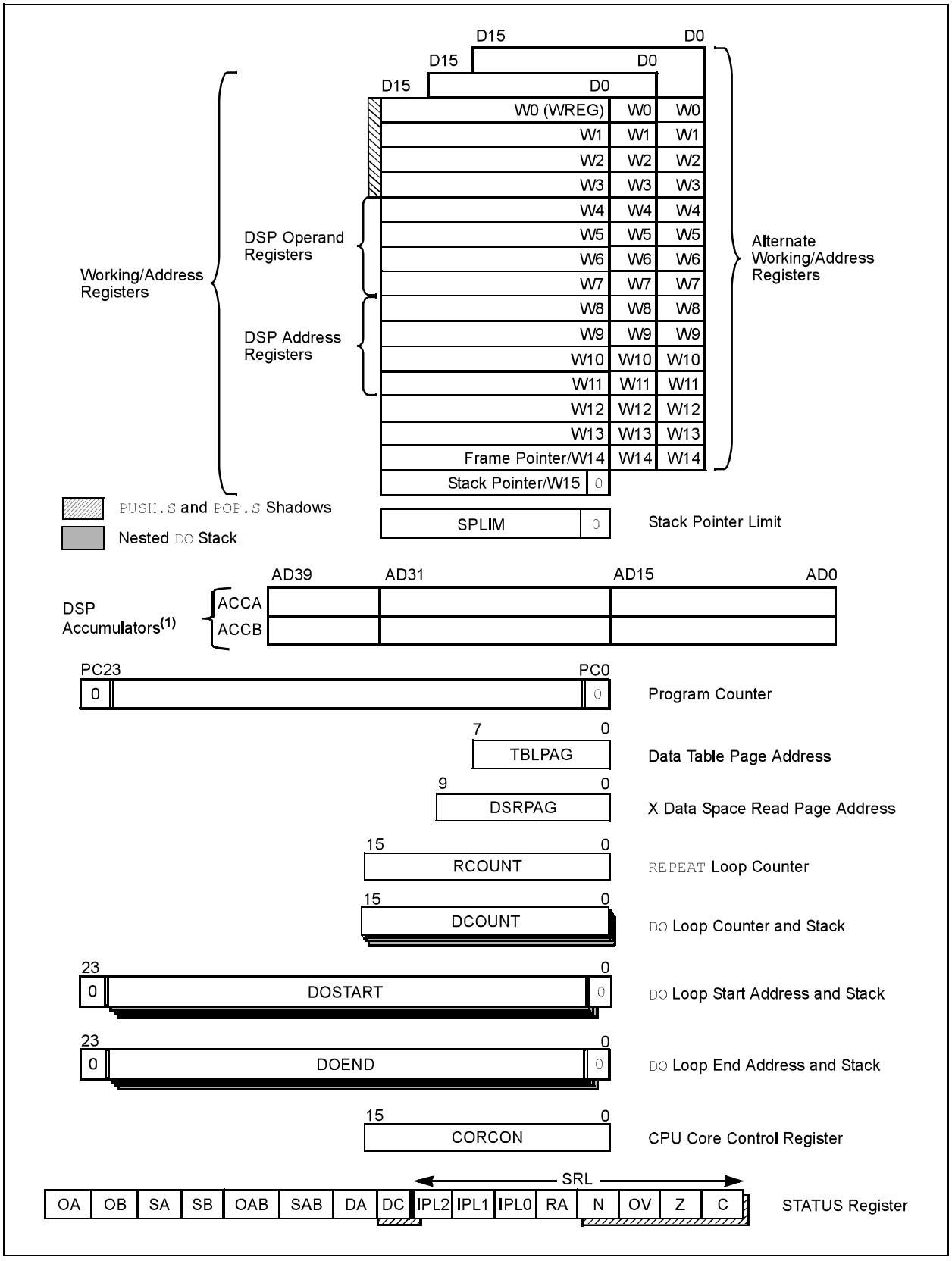
TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS

Register(s) Name	Description
W0 through W15(1)	Working Register Array
W0 through W14(1)	Alternate Working Register Array 1
W0 through W14(1)	Alternate Working Register Array 2
ACCA, ACCB	40-Bit DSP Accumulators
PC	23-Bit Program Counter
SR	ALU and DSP Engine STATUS Register
SPLIM	Stack Pointer Limit Value Register
TBLPAG	Table Memory Page Address Register
DSRPAG	Extended Data Space (EDS) Read Page Register
RCOUNT	REPEAT Loop Counter Register
DCOUNT	DO Loop Count Register
DOSTARTH(2), DOSTARTL(2)	DO Loop Start Address Register (High and Low)
DOENDH, DOENDL	DO Loop End Address Register (High and Low)
CORCON	Contains DSP Engine, DO Loop Control and Trap Status bits

Note 1: Memory-mapped W0 through W14 represent the value of the register in the currently active CPU context.

2: The DOSTARTH and DOSTARTL registers are read-only.

FIGURE 3-2: PROGRAMMER'S MODEL



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3.6 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA(3)	SB(3)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(1,2)	IPL1(1,2)	IPL0(1,2)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(3)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(3)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
0 = Accumulator A and B have not overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulator A or B is saturated or has been saturated at some time
0 = Accumulator A and B have not been saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop is in progress
0 = DO loop is not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: The IPL[2:0] bits are concatenated with the IPL3 bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1. User interrupts are disabled when IPL3 = 1.

2: The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using the bit operations.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5 **IPL[2:0]:** CPU Interrupt Priority Level Status bits(1,2)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop is in progress
0 = REPEAT loop is not in progress

bit 3 **N:** MCU ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit
This bit is used for signed arithmetic (two's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = Overflow has not occurred for signed arithmetic

bit 1 **Z:** MCU ALU Zero bit
1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit (MSb) of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: The IPL[2:0] bits are concatenated with the IPL3 bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1. User interrupts are disabled when IPL3 = 1.

2: The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using the bit operations.

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REGISTER 3-2: CORCON: CORE CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT(1)	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US[1:0]:** DSP Multiply Unsigned/Signed Control bits
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1)
1 = Terminates executing the DO loop at the end of the current loop iteration
0 = No effect

bit 10-8 **DL[2:0]:** DO Loop Nesting Level Status bits
111 = Seven DO loops are active
•
•
•
001 = One DO loop is active
000 = Zero DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

Note 1: This bit is always read as '0'.
2: The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

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REGISTER 3-3: CTXTSTAT: CPU W REGISTER CONTEXT STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	CCTXI[2:0]		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R-0	R/W-0	R/W-0
—	—	—	—	—	MCTXI[2:0]		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **CCTXI[2:0]:** Current (W Register) Context Identifier bits
111 = Reserved
•
•
•
011 = Reserved
010 = Alternate Working Register Set 2 is currently in use
001 = Alternate Working Register Set 1 is currently in use
000 = Default register set is currently in use

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **MCTXI[2:0]:** Manual (W Register) Context Identifier bits
111 = Reserved
•
•
•
011 = Reserved
010 = Alternate Working Register Set 2 was most recently manually selected
001 = Alternate Working Register Set 1 was most recently manually selected
000 = Default register set was most recently manually selected

3.7 Arithmetic Logic Unit (ALU)

The dsPIC33EVXXXGM00X/10X family ALU is 16 bits wide and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. The data for the ALU operation can come from the W register array or from the data memory, depending on the addressing mode of the instruction. Similarly, the output data from the ALU can be written to the W register array or a data memory location.

For information on the SR bits affected by each instruction, refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (DS70000157).

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

3.7.1 MULTIPLIER

Using the high-speed, 17-bit x 17-bit multiplier, the ALU supports unsigned, signed or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

3.7.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes the single-cycle per bit of the divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

3.8 DSP Engine

The DSP engine consists of a high-speed, 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON) as follows:

- Fractional or Integer DSP Multiply (IF)
- Signed, Unsigned or Mixed-Sign DSP Multiply (US)
- Conventional or Convergent Rounding (RND)
- Automatic Saturation On/Off for ACCA (SATA)
- Automatic Saturation On/Off for ACCB (SATB)
- Automatic Saturation On/Off for Writes to Data Memory (SATDW)
- Accumulator Saturation mode Selection (ACCSAT)

TABLE 3-2: DSP INSTRUCTIONS SUMMARY

Instruction	Algebraic Operation	ACC Write-Back
CLR	$A = 0$	Yes
ED	$A = (x-y)^2$	No
EDAC	$A = A + (x-y)^2$	No
MAC	$A = A + (x \cdot y)$	Yes
MAC	$A = A + x^2$	No
MOVSAC	No change in A	Yes
MPY	$A = x \cdot y$	No
MPY	$A = x^2$	No
MPY.N	$A = -x \cdot y$	No
MSC	$A = A - x \cdot y$	Yes

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4.0 MEMORY ORGANIZATION

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*.

The dsPIC33EVXXXGM00X/10X family architecture features separate program and data memory spaces and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

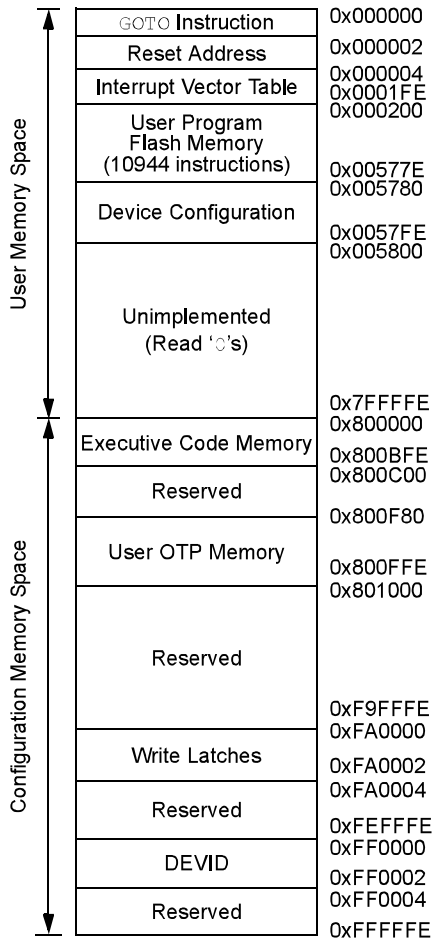
4.1 Program Address Space

The program address memory space of the dsPIC33EVXXXGM00X/10X family devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC, during program execution or from table operation, or from DS remapping, as described in **Section 4.7 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x02ABFF). The exception is the use of the TBLRD operations, which use TBLPAG[7] to read Device ID sections of the configuration memory space and the TBLWT operations, which are used to set up the write latches located in configuration memory space.

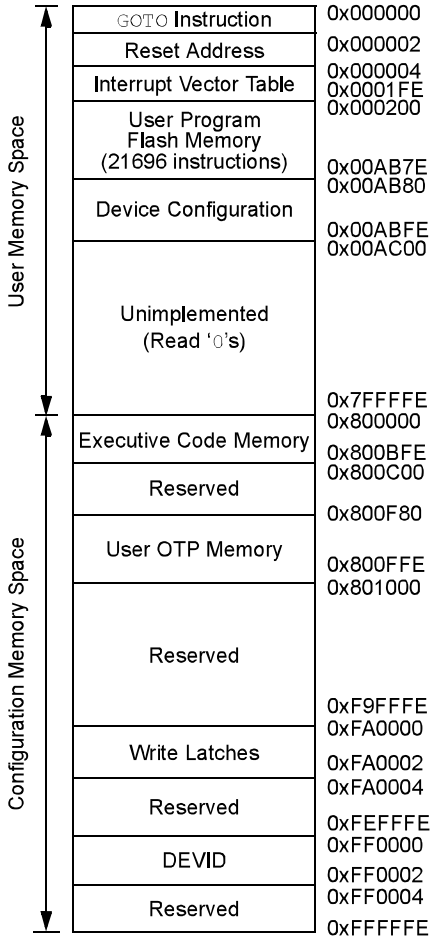
The program memory maps, which are presented by the device family and memory size, are shown in Figure 4-1 through Figure 4-4.

FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EV32GM00X/10X DEVICES(1)



Note 1: Memory areas are not shown to scale.

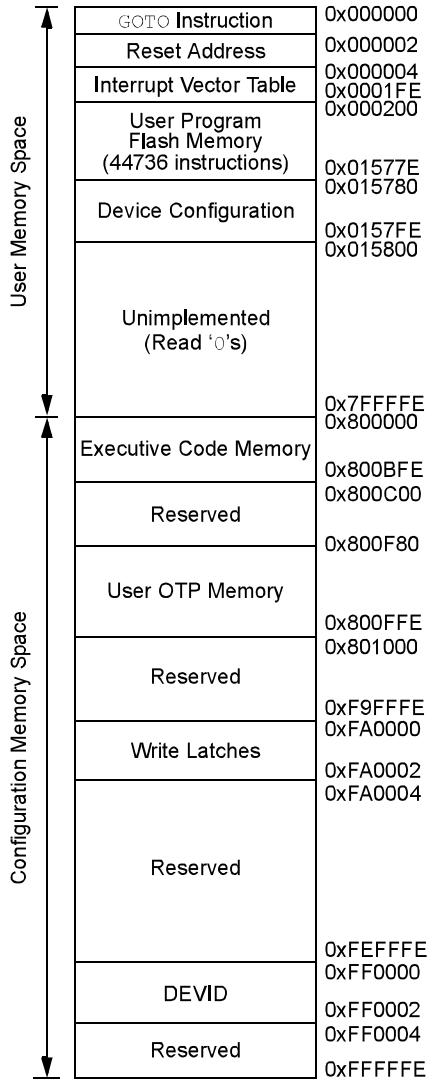
FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EV64GM00X/10X DEVICES(1)



Note 1: Memory areas are not shown to scale.

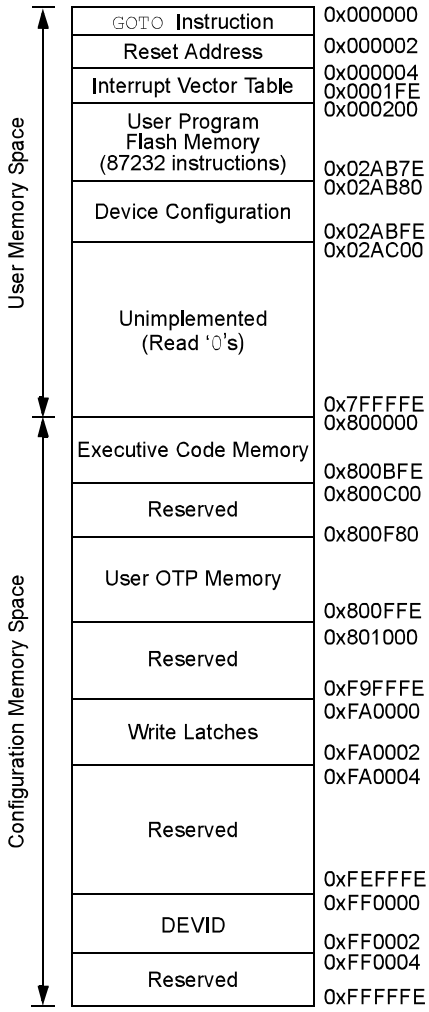
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FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EV128GM00X/10X DEVICES(1)



Note 1: Memory areas are not shown to scale.

FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EV256GM00X/10X DEVICES(1)



Note 1: Memory areas are not shown to scale.

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4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (see Figure 4-5).

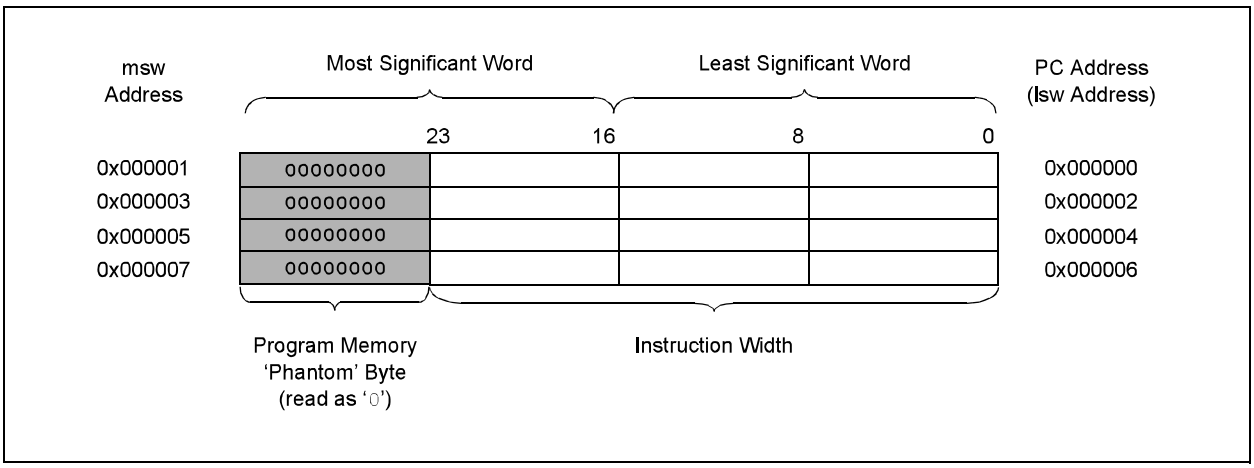
Program memory addresses are always word-aligned on the lower word and addresses are incremented or decremented by two during the code execution. This arrangement provides compatibility with the Data Memory Space Addressing and makes data in the program memory space accessible.

4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EVXXXGM00X/10X family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000 of Flash memory, with the actual address for the start of code at address, 0x000002 of Flash memory.

For more information on the Interrupt Vector Tables, see **Section 7.1 "Interrupt Vector Table"**.

FIGURE 4-5: PROGRAM MEMORY ORGANIZATION



4.2 Data Address Space

The dsPIC33EVXXXGM00X/10X family CPU has a separate, 16-bit wide data memory space. The Data Space (DS) is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-6 and Figure 4-8.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the DS. This arrangement gives a Base Data Space address range of 64 Kbytes or 32K words.

The Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS), which has a total address range of 16 Mbytes.

dsPIC33EVXXXGM00X/10X family devices implement up to 20 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 16 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all zero word or byte is returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data are aligned in data memory and registers as 16-bit words, but all DS EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33EVXXXGM00X/10X family instruction set supports both word and byte operations. As a consequence of byte accessibility, all the Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, therefore, care must be taken when mixing byte and word operations or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (`SE`) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (`ZE`) instruction on the appropriate address.

4.2.3 SFR SPACE

The first four Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EVXXXGM00X/10X family core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

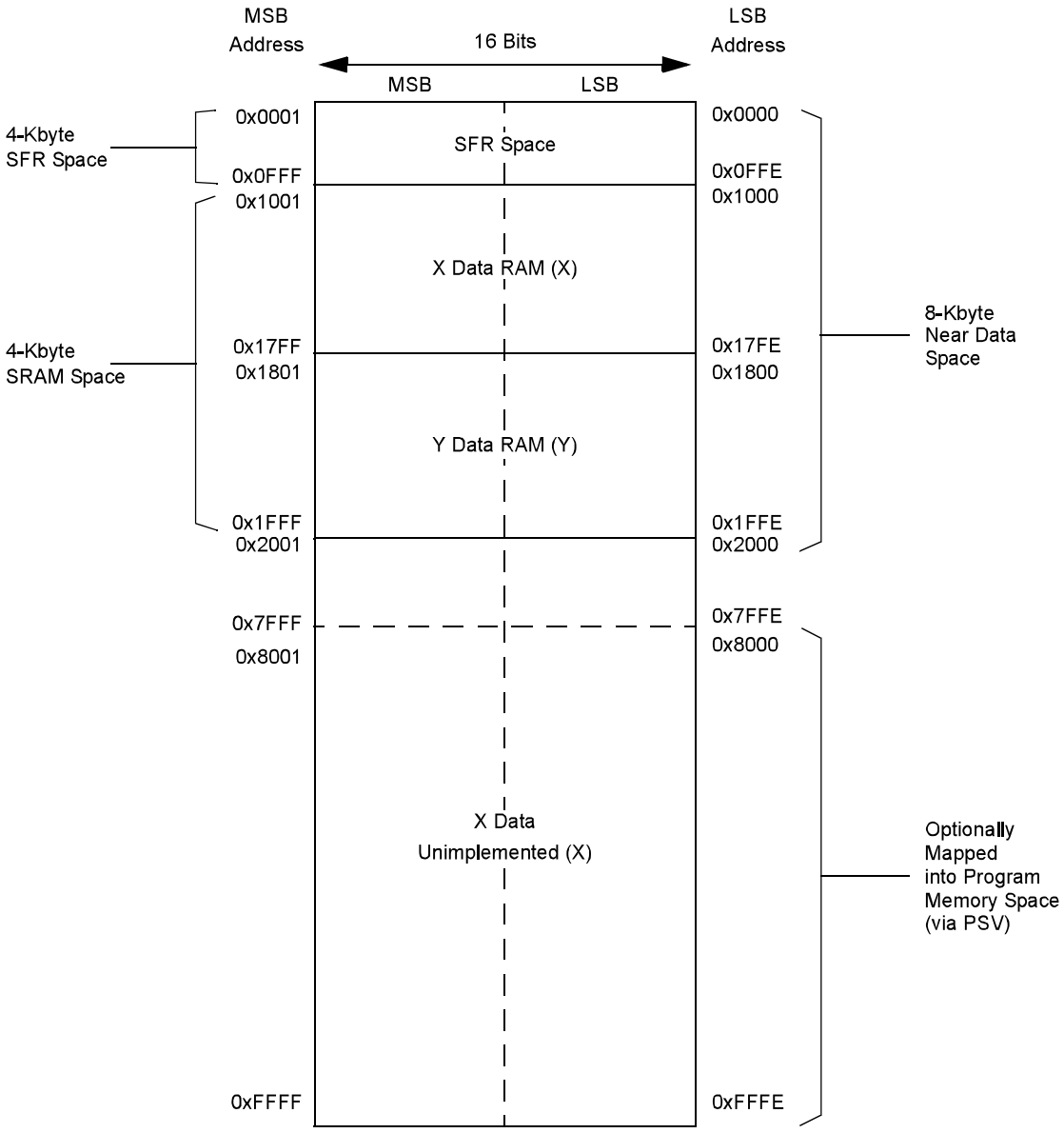
Note:	The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole DS is addressable using `MOV` instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

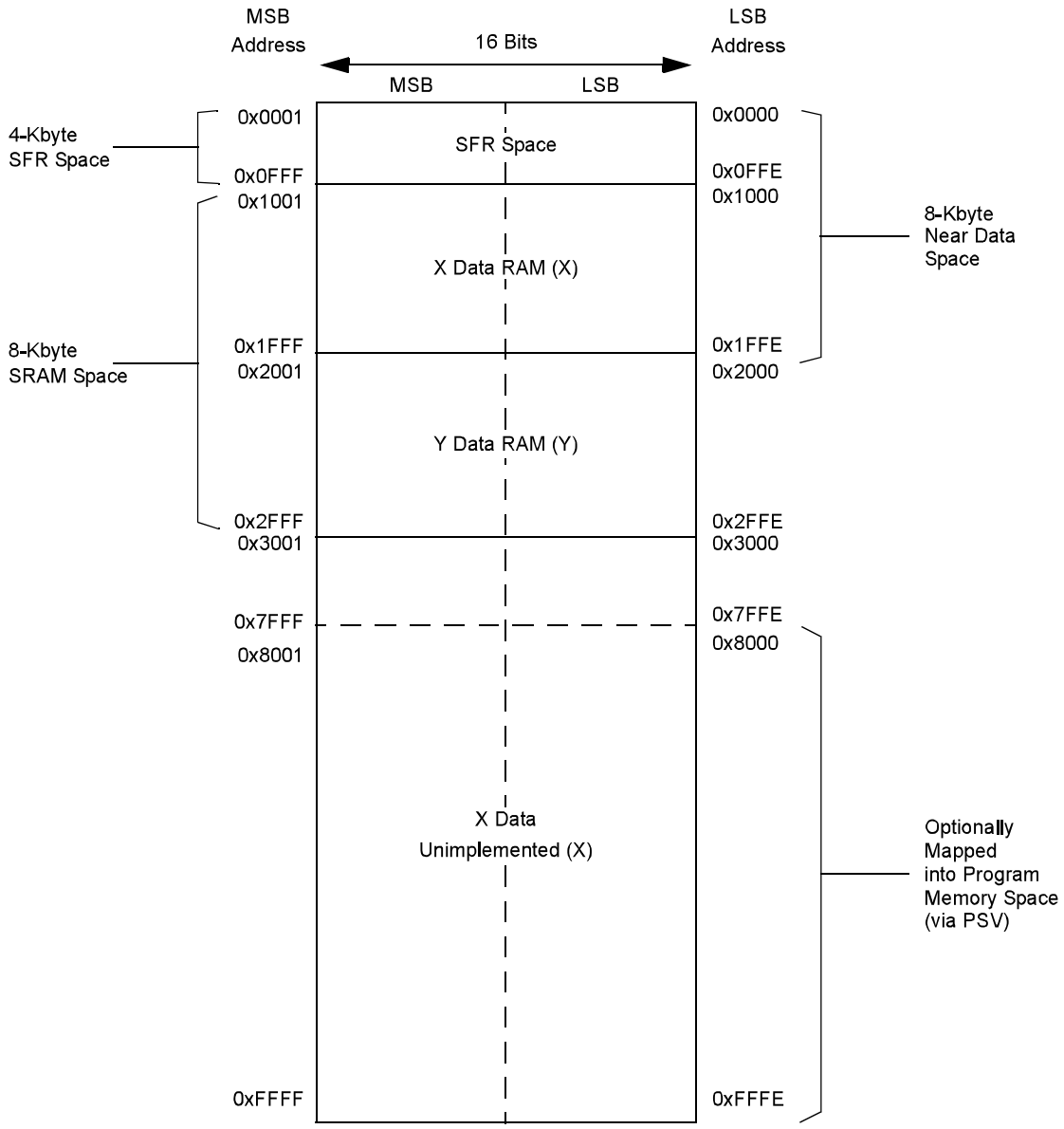
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FIGURE 4-6: DATA MEMORY MAP FOR 32-Kbyte DEVICES(1)



Note 1: Memory areas are not shown to scale.

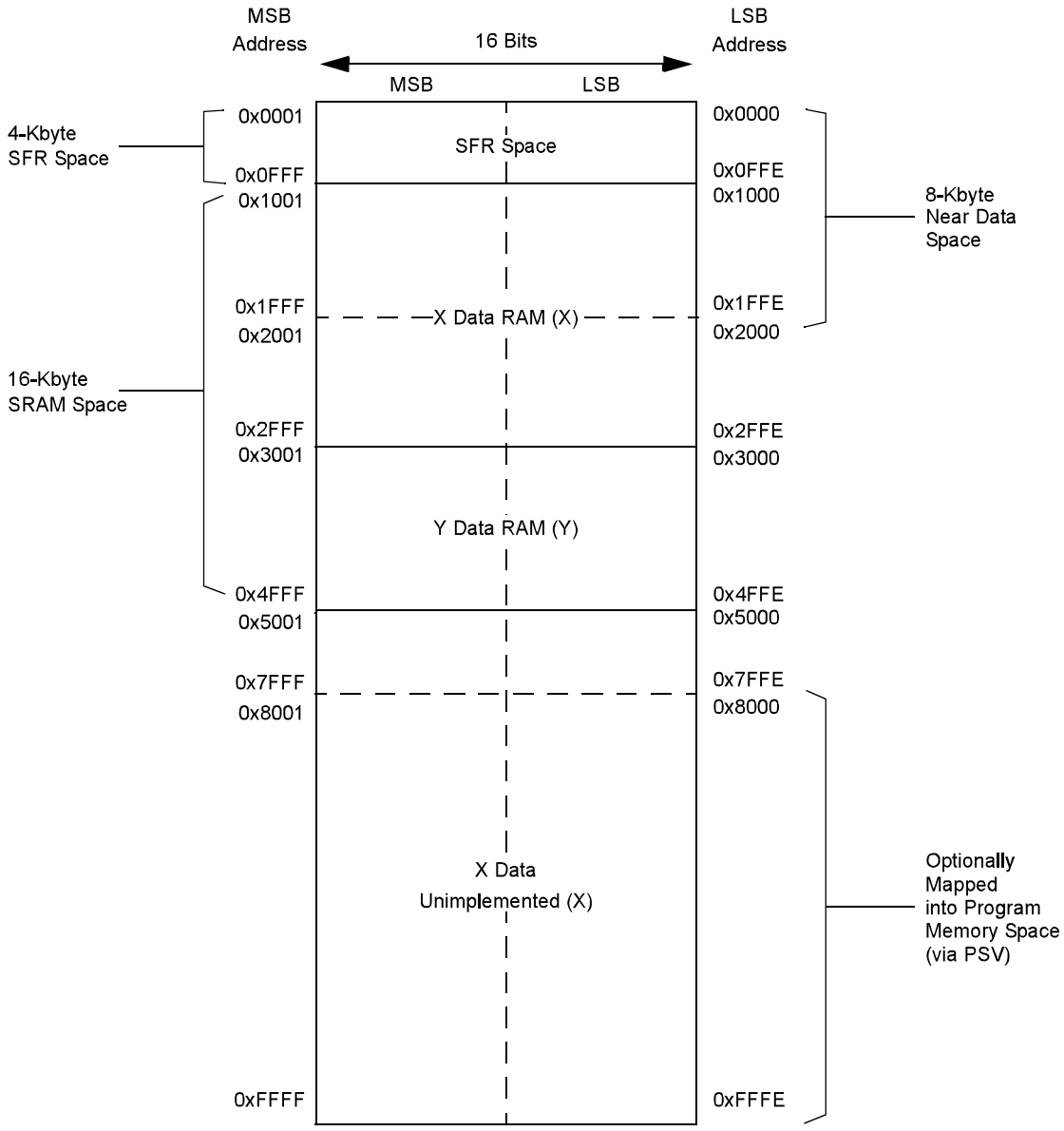
FIGURE 4-7: DATA MEMORY MAP FOR 64-Kbyte/128-Kbyte DEVICES(1)



Note 1: Memory areas are not shown to scale.

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FIGURE 4-8: DATA MEMORY MAP FOR 256-Kbyte DEVICES(1)



Note 1: Memory areas are not shown to scale.

4.2.5 X AND Y DATA SPACES

The dsPIC33EVXXXGM00X/10X family core has two Data Spaces: X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified, linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X DS is used by all instructions and supports all addressing modes. The X DS has separate read and write data buses. The X read data bus is the read data path for all instructions that view the DS as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y DS is used in concert with the X DS by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to the X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

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4.3 Special Function Register Maps

TABLE 4-1: CPU CORE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
W0	0000	W0 (WREG)																0000
W1	0002	W1																0000
W2	0004	W2																0000
W3	0006	W3																0000
W4	0008	W4																0000
W5	000A	W5																0000
W6	000C	W6																0000
W7	000E	W7																0000
W8	0010	W8																0000
W9	0012	W9																0000
W10	0014	W10																0000
W11	0016	W11																0000
W12	0018	W12																0000
W13	001A	W13																0000
W14	001C	W14																0000
W15	001E	W15																0800
SPLIM	0020	SPLIM																xxxx
ACCAL	0022	ACCAL																xxxx
ACCAH	0024	ACCAH																xxxx
ACCAU	0026	Sign Extension of ACCA[39]									ACCAU							xxxx
ACCBL	0028	ACCBL																xxxx
ACCBH	002A	ACCBH																xxxx
ACCBU	002C	Sign Extension of ACCB[39]									ACCBU							xxxx
PCL	002E	Program Counter Low Word Register															—	0000
PCH	0030	—	—	—	—	—	—	—	—	—	Program Counter High Word Register							0000
DSRPAG	0032	—	—	—	—	—	—	Data Space Read Page Register										0001
DSWPAG	0034	—	—	—	—	—	—	—	Data Space Write Page Register									0001
RCOUNT	0036	REPEAT Loop Counter Register															0	xxxx
DCOUNT	0038	DCOUNT[15:1]															0	xxxx
DOSTARTL	003A	DOSTARTL[15:1]															0	xxxx
DOSTARTH	003C	—	—	—	—	—	—	—	—	—	—	DOSTARTH[5:0]						00xx
DOENDL	003E	DOENDL[15:1]															—	xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-1: CPU CORE REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DOENDH	0040	—	—	—	—	—	—	—	—	—	—	DOENDH[5:0]						00xx
SR	0042	OA	OB	SA	SB	OAB	SAB	DA	DC	IPL2	IPL1	IPL0	RA	N	OV	Z	C	0000
CORCON	0044	VAR	—	US1	US0	EDT	DL2	DL1	DL0	SATA	SATB	SATDW	ACCSAT	IPL3	SFA	RND	IF	0020
MODCON	0046	XMODEN	YMODEN	—	—	BWM3	BWM2	BWM1	BWM0	YWM3	YWM2	YWM1	YWM0	XWM3	XWM2	XWM1	XWM0	0000
XMODSRT	0048	XMODSRT[15:1]															0	xxxx
XMODEND	004A	XMODEND[15:1]															1	xxxx
YMODSRT	004C	YMODSRT[15:1]															0	xxxx
YMODEND	004E	YMODEND[15:1]															1	xxxx
XBREV	0050	BREN	XBREV[14:0]															0xxx
DISICNT	0052	—	—	DISICNT[13:0]														xxxx
TBLPAG	0054	—	—	—	—	—	—	—	—	TBLPAG[7:0]								0000
MSTRPR	0058	MSTRPR[15:0]																0000
CTXTSTAT	005A	—	—	—	—	—	CCTXI[2:0]			—	—	—	—	—	MCTXI[2:0]			0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-2: TIMERS REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	0100	Timer1 Register																0000
PR1	0102	Period Register 1																FFFF
T1CON	0104	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0106	Timer2 Register																0000
TMR3HLD	0108	Timer3 Holding Register (For 32-bit timer operations only)																0000
TMR3	010A	Timer3 Register																0000
PR2	010C	Period Register 2																FFFF
PR3	010E	Period Register 3																FFFF
T2CON	0110	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	0112	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0114	Timer4 Register																0000
TMR5HLD	0116	Timer5 Holding Register (For 32-bit operations only)																0000
TMR5	0118	Timer5 Register																0000
PR4	011A	Period Register 4																FFFF
PR5	011C	Period Register 5																FFFF
T4CON	011E	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T5CON	0120	TON	—	TSIDL	—	—	—	—	—	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-3: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140	—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC1CON2	0142	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC1BUF	0144	Input Capture 1 Buffer Register																xxxx
IC1TMR	0146	Input Capture 1 Timer Register																0000
IC2CON1	0148	—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC2CON2	014A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC2BUF	014C	Input Capture 2 Buffer Register																xxxx
IC2TMR	014E	Input Capture 2 Timer Register																0000
IC3CON1	0150	—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC3CON2	0152	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC3BUF	0154	Input Capture 3 Buffer Register																xxxx
IC3TMR	0156	Input Capture 3 Timer Register																0000
IC4CON1	0158	—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC4CON2	015A	—	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC4BUF	015C	Input Capture 4 Buffer Register																xxxx
IC4TMR	015E	Input Capture 4 Timer Register																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-4: I2C1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1CON1	0200	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CON2	0202	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	1000
I2C1STAT	0204	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	0206	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	0208	—	—	—	—	—	—	I2C1 Address Mask Register										0000
I2C1BRG	020A	Baud Rate Generator Register																0000
I2C1TRN	020C	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1RCV	020E	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-5: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	UART1 Baud Rate Generator Prescaler Register																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	UART2 Baud Rate Generator Prescaler Register																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-6: SPI1 AND SPI2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248	SPI1 Transmit and Receive Buffer Register																0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	—	—	—	—	—	—	—	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268	SPI2 Transmit and Receive Buffer Register																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-7: ADC1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
ADC1BUF0	0300	ADC1 Data Buffer 0																xxxx
ADC1BUF1	0302	ADC1 Data Buffer 1																xxxx
ADC1BUF2	0304	ADC1 Data Buffer 2																xxxx
ADC1BUF3	0306	ADC1 Data Buffer 3																xxxx
ADC1BUF4	0308	ADC1 Data Buffer 4																xxxx
ADC1BUF5	030A	ADC1 Data Buffer 5																xxxx
ADC1BUF6	030C	ADC1 Data Buffer 6																xxxx
ADC1BUF7	030E	ADC1 Data Buffer 7																xxxx
ADC1BUF8	0310	ADC1 Data Buffer 8																xxxx
ADC1BUF9	0312	ADC1 Data Buffer 9																xxxx
ADC1BUFA	0314	ADC1 Data Buffer 10																xxxx
ADC1BUFB	0316	ADC1 Data Buffer 11																xxxx
ADC1BUFC	0318	ADC1 Data Buffer 12																xxxx
ADC1BUFD	031A	ADC1 Data Buffer 13																xxxx
ADC1BUFE	031C	ADC1 Data Buffer 14																xxxx
ADC1BUFF	031E	ADC1 Data Buffer 15																xxxx
AD1CON1	0320	ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0	SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE	0000
AD1CON2	0322	VCFG2	VCFG1	VCFG0	—	—	CSCNA	CHPS1	CHPS0	BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS	0000
AD1CON3	0324	ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0	ADCS7	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0	0000
AD1CHS123	0326	—	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0	—	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0	0000
AD1CHS0	0328	CH0NB	—	CH0SB5	CH0SB4	CH0SB3	CH0SB2	CH0SB1	CH0SB0	CH0NA	—	CH0SA5	CH0SA4	CH0SA3	CH0SA2	CH0SA1	CH0SA0	0000
AD1CSSH	032E	CSS[31:24]								—	—	—	—	CSS[19:16]				0000
AD1CSSL	0330	CSS[15:0]																0000
AD1CON4	0332	—	—	—	—	—	—	—	ADDMAEN	—	—	—	—	—	DMABL2	DMABL1	DMABL0	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-8: CTMU REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CTMUCON1	033A	CTMUEN	—	CTMUSIDL	TGEN	EDGEN	EDGSEQEN	IDISSEN	CTTRIG	—	—	—	—	—	—	—	—	0000
CTMUCON2	033C	EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT	EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—	0000
CTMUICON	033E	ITRIM[5:0]						IRNG[1:0]		—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-9: CAN1 REGISTER MAP WHEN WIN (C1CTRL[0]) = 0 OR 1 FOR dsPIC33EVXXXGM10X DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0	OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT[4:0]					0000
C1VEC	0404	—	—	—	FILHIT[4:0]					—	ICODE[6:0]							0000
C1FCTRL	0406	DMABS[2:0]			—	—	—	—	—	—	—	FSA[5:0]						0000
C1FIFO	0408	—	—	FBP[5:0]						—	—	FNRB[5:0]						0000
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT[7:0]								RERRCNT[7:0]								0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0	SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0	0000
C1FEN1	0414	FLTEN[15:0]																FFFF
C1FMSKSEL1	0418	F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0	F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0	0000
C1FMSKSEL2	041A	F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK1	F13MSK0	F12MSK1	F12MSK0	F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-10: CAN1 REGISTER MAP WHEN WIN (C1CTRL[0]) = 0 FOR dsPIC33EVXXXGM10X DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1RXFUL1	0420	RXFUL[15:0]																0000
C1RXFUL2	0422	RXFUL[31:16]																0000
C1RXOVF1	0428	RXOVF[15:0]																0000
C1RXOVF2	042A	RXOVF[31:16]																0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI1	TX1PRI0	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI1	TX0PRI0	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI1	TX3PRI0	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI1	TX2PRI0	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI1	TX5PRI0	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI1	TX4PRI0	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI1	TX7PRI0	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI1	TX6PRI0	xxxx
C1RXD	0440	CAN1 Receive Data Word Register																xxxx
C1TXD	0442	CAN1 Transmit Data Word Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL[0]) = 1 FOR dsPIC33EVXXXGM10X DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1BUFPNT1	0420	F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0	F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0	0000
C1BUFPNT2	0422	F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0	F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0	0000
C1BUFPNT3	0424	F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0	F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0	0000
C1BUFPNT4	0426	F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0	F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0	0000
C1RXM0SID	0430	SID[10:0]											—	MIDE	—	EID17	EID16	xxxx
C1RXM0EID	0432	EID[15:0]																xxxx
C1RXM1SID	0434	SID[10:0]											—	MIDE	—	EID17	EID16	xxxx
C1RXM1EID	0436	EID[15:0]																xxxx
C1RXM2SID	0438	SID[10:0]											—	MIDE	—	EID17	EID16	xxxx
C1RXM2EID	043A	EID[15:0]																xxxx
C1RXF0SID	0440	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF0EID	0442	EID[15:0]																xxxx
C1RXF1SID	0444	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF1EID	0446	EID[15:0]																xxxx
C1RXF2SID	0448	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF2EID	044A	EID[15:0]																xxxx
C1RXF3SID	044C	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF3EID	044E	EID[15:0]																xxxx
C1RXF4SID	0450	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF4EID	0452	EID[15:0]																xxxx
C1RXF5SID	0454	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF5EID	0456	EID[15:0]																xxxx
C1RXF6SID	0458	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF6EID	045A	EID[15:0]																xxxx
C1RXF7SID	045C	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF7EID	045E	EID[15:0]																xxxx
C1RXF8SID	0460	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF8EID	0462	EID[15:0]																xxxx
C1RXF9SID	0464	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF9EID	0466	EID[15:0]																xxxx
C1RXF10SID	0468	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF10EID	046A	EID[15:0]																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-11: CAN1 REGISTER MAP WHEN WIN (C1CTRL[0]) = 1 FOR dsPIC33EVXXXGM10X DEVICES (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11SID	046C	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF11EID	046E	EID[15:0]																xxxx
C1RXF12SID	0470	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF12EID	0472	EID[15:0]																xxxx
C1RXF13SID	0474	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF13EID	0476	EID[15:0]																xxxx
C1RXF14SID	0478	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF14EID	047A	EID[15:0]																xxxx
C1RXF15SID	047C	SID[10:0]											—	EXIDE	—	EID17	EID16	xxxx
C1RXF15EID	047E	EID[15:0]																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: SENT1 RECEIVER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENT1CON1	0500	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0000
SENT1CON2	0504	TICKTIME[15:0] (Transmit modes) or SYNCMAX[15:0] (Receive mode)																FFFF
SENT1CON3	0508	FRAMETIME[15:0] (Transmit modes) or SYNCMIN[15:0] (Receive mode)																FFFF
SENT1STAT	050C	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENT1SYNC	0510	Synchronization Time Period Register (Transmit mode)																0000
SENT1DATL	0514	DATA4[3:0]				DATA5[3:0]				DATA6[3:0]				CRC[3:0]				0000
SENT1DATH	0516	STAT[3:0]				DATA1[3:0]				DATA2[3:0]				DATA3[3:0]				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-13: SENT2 RECEIVER REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SENT2CON1	0520	SNTEN	—	SNTSIDL	—	RCVEN	TXM	TXPOL	CRCEN	PPP	SPCEN	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0	0000
SENT2CON2	0524	TICKTIME[15:0] (Transmit modes) or SYNCMAX[15:0] (Receive mode)																FFFF
SENT2CON3	0528	FRAMETIME[15:0] (Transmit modes) or SYNCMIN[15:0] (Receive mode)																FFFF
SENT2STAT	052C	—	—	—	—	—	—	—	—	PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN	0000
SENT2SYNC	0530	Synchronization Time Period Register (Transmit mode)																0000
SENT2DATL	0534	DATA4[3:0]				DATA5[3:0]				DATA6[3:0]				CRC[3:0]				0000
SENT2DATH	0536	STAT[3:0]				DATA1[3:0]				DATA2[3:0]				DATA3[3:0]				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-14: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM002/102 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR10	0684	—	—	RP176R[5:0]						—	—	—	—	—	—	—	—	0000
RPOR11	0686	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	—	—	—	—	—	—	—	—	—	—	RP181R[5:0]						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-15: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM004/104 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR5	067A	—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0	—	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0	0000
RPOR6	067C	—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0	—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0	0000
RPOR7	067E	—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0	—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0	0000
RPOR10	0684	—	—	RP176R[5:0]						—	—	—	—	—	—	—	—	0000
RPOR11	0686	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	—	—	—	—	—	—	—	—	—	—	RP181R[5:0]						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-16: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EVXXXGM006/106 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0670	—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0	—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0	0000
RPOR1	0672	—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0	—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0	0000
RPOR2	0674	—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0	—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0	0000
RPOR3	0676	—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0	—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0	0000
RPOR4	0678	—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0	—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0	0000
RPOR5	067A	—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0	—	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0	0000
RPOR6	067C	—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0	—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0	0000
RPOR7	067E	—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0	—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0	0000
RPOR8	0680	—	—	RP70R5	RP70R4	RP70R3	RP70R2	RP70R1	RP70R0	—	—	RP69R5	RP69R4	RP69R3	RP69R2	RP69R1	RP69R0	0000
RPOR9	0682	—	—	RP118R5	RP118R4	RP118R3	RP118R2	RP118R1	RP118R0	—	—	RP97R5	RP97R4	RP97R3	RP97R2	RP97R1	RP97R0	0000
RPOR10	0684	—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0	—	—	RP120R5	RP120R4	RP120R3	RP120R2	RP120R1	RP120R0	0000
RPOR11	0686	—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0	—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0	0000
RPOR12	0688	—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0	—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0	0000
RPOR13	068A	—	—	—	—	—	—	—	—	—	—	RP181R[5:0]						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-17: PERIPHERAL PIN SELECT INPUT REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPINR0	06A0	INT1R[7:0]								—	—	—	—	—	—	—	—	0000
RPINR1	06A2	—	—	—	—	—	—	—	—	INT2R[7:0]								0000
RPINR3	06A6	—	—	—	—	—	—	—	—	T2CKR[7:0]								0000
RPINR7	06AE	IC2R7	IC2R6	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0	IC1R7	IC1R6	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0	0000
RPINR8	06B0	IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0	IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0	0000
RPINR11	06B6	—	—	—	—	—	—	—	—	OCFAR[7:0]								0000
RPINR12	06B8	FLT2R7	FLT2R6	FLT2R5	FLT2R4	FLT2R3	FLT2R2	FLT2R1	FLT2R0	FLT1R7	FLT1R6	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0	0000
RPINR18	06C4	—	—	—	—	—	—	—	—	U1RXR[7:0]								0000
RPINR19	06C6	—	—	—	—	—	—	—	—	U2RXR[7:0]								0000
RPINR22	06CC	SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0	SDI2R7	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0	0000
RPINR23	06CE	—	—	—	—	—	—	—	—	SS2R[7:0]								0000
RPINR26	06D4	—	—	—	—	—	—	—	—	C1RXR[7:0](1)								0000
RPINR37	06EA	SYNCI1R[7:0]								—	—	—	—	—	—	—	—	0000
RPINR38	06EC	DTCMP1R[7:0]								—	—	—	—	—	—	—	—	0000
RPINR39	06EE	DTCMP3R7	DTCMP3R6	DTCMP3R5	DTCMP3R4	DTCMP3R3	DTCMP3R2	DTCMP3R1	DTCMP3R0	DTCMP2R7	DTCMP2R6	DTCMP2R5	DTCMP2R4	DTCMP2R3	DTCMP2R2	DTCMP2R1	DTCMP2R0	0000
RPINR44	06F8	SENT1R[7:0]								—	—	—	—	—	—	—	—	0000
RPINR45	06FA	—	—	—	—	—	—	—	—	SENT2R[7:0]								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

TABLE 4-18: DMT REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMTCON	0700	ON	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
DMTPRECLR	0704	STEP1[7:0]								—	—	—	—	—	—	—	—	0000
DMTCLR	0708	—	—	—	—	—	—	—	—	STEP2[7:0]								0000
DMTSTAT	070C	—	—	—	—	—	—	—	—	BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN	0000
DMTCNTL	0710	COUNTER[15:0]																0000
DMTCNTH	0712	COUNTER[31:16]																0000
DMTHOLDREG	0714	UPRCNT[15:0]																0000
DMTPSCNTL	0718	PSCNT[15:0]																0000
DMTPSCNTH	071A	PSCNT[31:16]																0000
DMTPSINTVL	071C	PSINTV[15:0]																0000
DMTPSINTVH	071E	PSINTV[31:16]																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-19: NVM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
NVMCON	0728	WR	WREN	WRERR	NVMSIDL	—	—	RPDF	URERR	—	—	—	—	NVMOP3	NVMOP2	NVMOP1	NVMOP0	0000
NVMADR	072A	NVMADR[15:0]																0000
NVMADRU	072C	—	—	—	—	—	—	—	—	NVMADRU[23:16]								0000
NVMKEY	072E	—	—	—	—	—	—	—	—	NVMKEY[7:0]								0000
NVMSRCADRL	0730	NVMSRCADR[15:1]															0	0000
NVMSRCADRH	0732	—	—	—	—	—	—	—	—	NVMSRCADR[23:16]								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-20: SYSTEM CONTROL REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RCON	0740	TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS	EXTR	SWR	SWDTEN	WDTO	SLEEP	IDLE	BOR	POR	Note 1
OSCCON	0742	—	COSC2	COSC1	COSC0	—	NOSC2	NOSC1	NOSC0	CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN	Note 2
CLKDIV	0744	ROI	DOZE2	DOZE1	DOZE0	DOZEN	FRCDIV2	FRCDIV1	FRCDIV0	PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0	0000
PLLFBD	0746	—	—	—	—	—	—	—	PLLDIV[8:0]									0000
OSCTUN	0748	—	—	—	—	—	—	—	—	—	—	TUN[5:0]						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: RCON register Reset values are dependent on the type of Reset.
2: OSCCON register Reset values are dependent on the Configuration fuses.

TABLE 4-21: REFERENCE CLOCK REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
REFOCON	074E	ROON	—	ROSSLP	ROSEL	RODIV3	RODIV2	RODIV1	RODIV0	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-22: PMD REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	—	PWMMD	—	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD(1)	AD1MD	0000
PMD2	0762	—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD	—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	—	—	—	—	—	CMPMD	—	—	—	—	—	—	—	—	—	—	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—		—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	—	—	—	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	—	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD	—	—	—	—	0000
													DMA1MD					
													DMA2MD					
													DMA3MD					
PMD8	076E	—	—	—	SENT2MD	SENT1MD	—	—	DMTMD	—	—	—	—	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

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TABLE 4-23: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IFS0	0800	NVMIF	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	—	—	—	INT1IF	CNIF	CMPIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	—	—	—	—	—	—	—	—	—	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF(1)	SPI2IF	SPI2EIF	0000
IFS3	0806	—	—	—	—	—	—	PSEMIF	—	—	—	—	—	—	—	—	—	0000
IFS4	0808	—	—	CTMUIF	—	—	—	—	—	—	C1TXIF(1)	—	—	—	U2EIF	U1EIF	—	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IF	0000
IFS8	0810	—	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS10	0814	—	—	I2C1BCIF	—		—	—	—	—	—	—	—	—	—	—	—	0000
IFS11	0816	—	—	—	—	—	ECCSBEIF	SENT2IF	SENT2EIF	SENT1IF	SENT1EIF	—	—	—	—	—	—	0000
IEC0	0820	NVMIE	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	—	—	—	INT1IE	CNIE	CMPIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	—	—	—	—	—	—	—	—	—	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE(1)	SPI2IE	SPI2EIE	0000
IEC3	0826	—	—	—	—	—	—	PSEMIE	—	—	—	—	—	—	—	—	—	0000
IEC4	0828	—	—	CTMUIE	—	—	—	—	—	—	C1TXIE(1)	—	—	—	U2EIE	U1EIE	—	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IE	0000
IEC8	0830	—	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC10	0834	—	—	I2C1BCIE	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC11	0836	—	—	—	—	—	ECCSBEIE	SENT2IE	SENT2EIE	SENT1IE	SENT1EIE	—	—	—	—	—	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	DMA0IP2	DMA0IP1	DMA0IP0	4444
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	NVMIP2	NVMIP1	NVMIP0	—	DMA1IP2	DMA1IP1	DMA1IP0	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4444
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	CMPIP2	CMPIP1	CMPIP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	—	—	—	—	—	—	—	—	—	—	—	—		INT1IP[2:0]		0004
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	DMA2IP2	DMA2IP1	DMA2IP0	4444
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	C1IP2	C1IP1	C1IP0	—	C1RXIP2(1)	C1RXIP1(1)	C1RXIP0(1)	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	4444
IPC9	0852	—	—	—	—	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	DMA3IP2	DMA3IP1	DMA3IP0	0444
IPC14	085C	—	—	—	—	—	—	—	—	—		PSEMIP[2:0]		—	—	—	—	0040
IPC16	0860	—	—	—	—	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	—	—	—	0440
IPC17	0862	—	—	—	—	—		C1TXIP[2:0](1)		—	—	—	—	—	—	—	—	0400

Legend: — = unimplemented, read as '0' Reset values are shown in hexadecimal.

Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

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TABLE 4-23: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EVXXXGM00X/10X FAMILY DEVICES (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP[2:0]			—	—	—	—	0040
IPC23	086E	—	PWM2IP2	PWM2IP1	PWM2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC24	0870	—	—	—	—	—	—	—	—	—	—	—	—	—	PWM3IP[2:0]			0004
IPC35	0886	—	—	—	—	—	ICDIP[2:0]			—	—	—	—	—	—	—	—	0400
IPC43	0896	—	—	—	—	—	—	—	—	—	I2C1BCIP[2:0]			—	—	—	—	0040
IPC45	089A	—	SENT1IP2	SENT1IP1	SENT1IP0	—	SENT1EIP2	SENT1EIP1	SENT1EIP0	—	—	—	—	—	—	—	—	4400
IPC46	089C	—	—	—	—	—	ECCSBEIP2	ECCSBEIP1	ECCSBEIP0	—	SENT2IP2	SENT2IP1	SENT2IP0	—	SENT2EIP2	SENT2EIP1	SENT2EIP0	0444
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	AIVTEN	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
INTCON3	08C4	DMT	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ECCDBE	SGHT	0000
INTTREG	08C8	—	—	—	—	—	ILR[3:1]			VECNUM[7:0]								0000

Legend: — = unimplemented, read as '0' Reset values are shown in hexadecimal.

Note 1: This feature is available only on dsPIC33EVXXXGM10X devices.

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TABLE 4-24: OUTPUT COMPARE REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
OC1CON1	0900	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC1CON2	0902	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC1RS	0904	Output Compare 1 Secondary Register																xxxx
OC1R	0906	Output Compare 1 Register																xxxx
OC1TMR	0908	Output Compare 1 Timer Value Register																xxxx
OC2CON1	090A	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC2CON2	090C	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC2RS	090E	Output Compare 2 Secondary Register																xxxx
OC2R	0910	Output Compare 2 Register																xxxx
OC2TMR	0912	Output Compare 2 Timer Value Register																xxxx
OC3CON1	0914	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC3CON2	0916	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC3RS	0918	Output Compare 3 Secondary Register																xxxx
OC3R	091A	Output Compare 3 Register																xxxx
OC3TMR	091C	Output Compare 3 Timer Value Register																xxxx
OC4CON1	091E	—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—	ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0	0000
OC4CON2	0920	FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32	OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000C
OC4RS	0922	Output Compare 4 Secondary Register																xxxx
OC4R	0924	Output Compare 4 Register																xxxx
OC4TMR	0926	Output Compare 4 Timer Value Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-25: OP AMP/COMPARATOR REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
CMSTAT	0A80	PSIDL	—	—	C5EVT	C4EVT	C3EVT	C2EVT	C1EVT	—	—	—	C5OUT	C4OUT	C3OUT	C2OUT	C1OUT	0000
CVR1CON	0A82	CVREN	CVROE(1)	—	—	CVRSS	VREFSEL	—	—	—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0	0000
CM1CON	0A84	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM1MSKSRC	0A86	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM1MSKCON	0A88	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM1FLTR	0A8A	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM2CON	0A8C	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM2MSKSRC	0A8E	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM2MSKCON	0A90	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM2FLTR	0A92	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM3CON	0A94	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM3MSKSRC	0A96	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM3MSKCON	0A98	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM3FLTR	0A9A	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM4CON	0A9C	CON	COE	CPOL	—	—	—	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM4MSKSRC	0A9E	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM4MSKCON	0AA0	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM4FLTR	0AA2	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CM5CON	0AA4	CON	COE	CPOL	—	—	OPAEN	CEVT	COUT	EVPOL1	EVPOL0	—	CREF	—	—	CCH1	CCH0	0000
CM5MSKSRC	0AA6	—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0	SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0	0000
CM5MSKCON	0AA8	HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN	NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN	0000
CM5FLTR	0AAA	—	—	—	—	—	—	—	—	—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0	0000
CVR2CON	0AB4	CVREN	CVROE(1)	—	—	CVRSS	VREFSEL	—	—	—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: CVROE (CVR2CON[14]) is not available on 28-pin and 36-pin devices.

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TABLE 4-26: DMAC REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMA0CON	0B00	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA0REQ	0B02	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA0STAL	0B04	STA[15:0]																0000
DMA0STAH	0B06	—	—	—	—	—	—	—	—	STA[23:16]								0000
DMA0STBL	0B08	STB[15:0]																0000
DMA0STBH	0B0A	—	—	—	—	—	—	—	—	STB[23:16]								0000
DMA0PAD	0B0C	PAD[15:0]																0000
DMA0CNT	0B0E	—	—	CNT[13:0]														0000
DMA1CON	0B10	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA1REQ	0B12	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA1STAL	0B14	STA[15:0]																0000
DMA1STAH	0B16	—	—	—	—	—	—	—	—	STA[23:16]								0000
DMA1STBL	0B18	STB[15:0]																0000
DMA1STBH	0B1A	—	—	—	—	—	—	—	—	STB[23:16]								0000
DMA1PAD	0B1C	PAD[15:0]																0000
DMA1CNT	0B1E	—	—	CNT[13:0]														0000
DMA2CON	0B20	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA2REQ	0B22	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA2STAL	0B24	STA[15:0]																0000
DMA2STAH	0B26	—	—	—	—	—	—	—	—	STA[23:16]								0000
DMA2STBL	0B28	STB[15:0]																0000
DMA2STBH	0B2A	—	—	—	—	—	—	—	—	STB[23:16]								0000
DMA2PAD	0B2C	PAD[15:0]																0000
DMA2CNT	0B2E	—	—	CNT[13:0]														0000
DMA3CON	0B30	CHEN	SIZE	DIR	HALF	NULLW	—	—	—	—	—	AMODE1	AMODE0	—	—	MODE1	MODE0	0000
DMA3REQ	0B32	FORCE	—	—	—	—	—	—	—	IRQSEL7	IRQSEL6	IRQSEL5	IRQSEL4	IRQSEL3	IRQSEL2	IRQSEL1	IRQSEL0	00FF
DMA3STAL	0B34	STA[15:0]																0000
DMA3STAH	0B36	—	—	—	—	—	—	—	—	STA[23:16]								0000
DMA3STBL	0B38	STB[15:0]																0000
DMA3STBH	0B3A	—	—	—	—	—	—	—	—	STB[23:16]								0000
DMA3PAD	0B3C	PAD[15:0]																0000
DMA3CNT	0B3E	—	—	CNT[13:0]														0000
DMAPWC	0BF0	—	—	—	—	—	—	—	—	—	—	—	—	PWCOL[3:0]				0000
DMARQC	0BF2	—	—	—	—	—	—	—	—	—	—	—	—	RQCOL[3:0]				0000
DMAPPS	0BF4	—	—	—	—	—	—	—	—	—	—	—	—	PPST[3:0]				0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-26: DMAC REGISTER MAP (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
DMALCA	0BF6	—	—	—	—	—	—	—	—	—	—	—	—	LSTCH[3:0]				000F
DSADRL	0BF8	DSADR[15:0]																0000
DSADRH	0BFA	—	—	—	—	—	—	—	—	DSADR[23:16]								0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-27: PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV[2:0]			0000
PTPER	0C04	PTPER[15:0]																FFF8
SEVTCMP	0C06	SEVTCMP[15:0]																0000
MDC	0C0A	MDC[15:0]																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK[9:0]										0000
PWMKEY	0C1E	PWMKEY[15:0]																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-28: PWM GENERATOR 1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	—	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON1	0C24	—	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC1	0C26	PDC1[15:0]																0000
PHASE1	0C28	PHASE1[15:0]																0000
DTR1	0C2A	—	—	DTR1[13:0]														0000
ALTDTR1	0C2C	—	—	ALTDTR1[13:0]														0000
TRIG1	0C32	TRGCMP[15:0]																0000
TRGCON1	0C34	TRGDIV[3:0]				—	—	—	—	—	—	TRGSTRT[5:0]						0000
PWMCAP1	0C38	PWMCAP1[15:0]																0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB[11:0]												0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-29: PWM GENERATOR 2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON2	0C40	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	—	CAM	XPRES	IUE	0000
IOCON2	0C42	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON2	0C44	—	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC2	0C46	PDC2[15:0]																0000
PHASE2	0C48	PHASE2[15:0]																0000
DTR2	0C4A	—	—	DTR2[13:0]														0000
ALTDTR2	0C4C	—	—	ALTDTR2[13:0]														0000
TRIG2	0C52	TRGCMP[15:0]																0000
TRGCON2	0C54	TRGDIV[3:0]				—	—	—	—	—	—	TRGSTRT[5:0]						0000
PWMCAP2	0C58	PWMCAP2[15:0]																0000
LEBCON2	0C5A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY2	0C5C	—	—	—	—	LEB[11:0]												0000
AUXCON2	0C5E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-30: PWM GENERATOR 3 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON3	0C60	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	—	CAM	XPRES	IUE	0000
IOCON3	0C62	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	0000
FCLCON3	0C64	—	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC3	0C66	PDC3[15:0]																0000
PHASE3	0C68	PHASE3[15:0]																0000
DTR3	0C6A	—	—	DTR3[13:0]														0000
ALTDTR3	0C6C	—	—	ALTDTR3[13:0]														0000
TRIG3	0C72	TRGCMP[15:0]																0000
TRGCON3	0C74	TRGDIV[3:0]				—	—	—	—	—	—	TRGSTRT[5:0]						0000
PWMCAP3	0C78	PWMCAP3[15:0]																0000
LEBCON3	0C7A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY3	0C7C	—	—	—	—	LEB[11:0]												0000
AUXCON3	0C7E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-31: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	TRISA[12:7]						—	—	TRISA4	—	—	TRISA[1:0]		1F93
PORTA	0E02	—	—	—	RA[12:7]						—	—	RA4	—	—	RA[1:0]		0000
LATA	0E04	—	—	—	LATA[12:7]						—	—	LATA4	—	—	LATA[1:0]		0000
ODCA	0E06	—	—	—	ODCA[12:7]						—	—	ODCA4	—	—	ODCA[1:0]		0000
CNENA	0E08	—	—	—	CNIEA[12:7]						—	—	CNIEA4	—	—	CNIEA[1:0]		0000
CNPUA	0E0A	—	—	—	CNPUA[12:7]						—	—	CNPUA4	—	—	CNPUA[1:0]		0000
CNPDA	0E0C	—	—	—	CNPDA[12:7]						—	—	CNPDA4	—	—	CNPDA[1:0]		0000
ANSELA	0E0E	—	—	—	ANSA[12:9]				—	ANSA7	—	—	ANSA4	—	—	ANSA[1:0]		1E93
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	TRISA[10:7]				—	—	TRISA[4:0]					DF9F
PORTA	0E02	—	—	—	—	—	RA[10:7]				—	—	RA[4:0]					0000
LATA	0E04	—	—	—	—	—	LATA[10:7]				—	—	LATA[4:0]					0000
ODCA	0E06	—	—	—	—	—	ODCA[10:7]				—	—	ODCA[4:0]					0000
CNENA	0E08	—	—	—	—	—	CNIEA[10:7]				—	—	CNIEA[4:0]					0000
CNPUA	0E0A	—	—	—	—	—	CNPUA[10:7]				—	—	CNPUA[4:0]					0000
CNPDA	0E0C	—	—	—	—	—	CNPDA[10:7]				—	—	CNPDA[4:0]					0000
ANSELA	0E0E	—	—	—	—	—	ANSA[10:9]		—	ANSA7	—	—	ANSA4	—	ANSA[2:0]			1813
SR1A	0E10	—	—	—	—	—	—	SR1A9	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	SR0A9	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-33: PORTA REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—	—	—	—	—	—	—	TRISA[4:0]					DF9F
PORTA	0E02	—	—	—	—	—	—	—	—	—	—	—	RA[4:0]					0000
LATA	0E04	—	—	—	—	—	—	—	—	—	—	—	LATA[4:0]					0000
ODCA	0E06	—	—	—	—	—	—	—	—	—	—	—	ODCA[4:0]					0000
CNENA	0E08	—	—	—	—	—	—	—	—	—	—	—	CNIEA[4:0]					0000
CNPUA	0E0A	—	—	—	—	—	—	—	—	—	—	—	CNPUA[4:0]					0000
CNPDA	0E0C	—	—	—	—	—	—	—	—	—	—	—	CNPDA[4:0]					0000
ANSELA	0E0E	—	—	—	—	—	—	—	—	—	—	—	ANSA4	—	ANSA[2:0]			1813
SR1A	0E10	—	—	—	—	—	—	—	—	—	—	—	SR1A4	—	—	—	—	0000
SR0A	0E12	—	—	—	—	—	—	—	—	—	—	—	SR0A4	—	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-34: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E14	TRISB[15:0]																FFFF
PORTB	0E16	RB[15:0]																xxxx
LATB	0E18	LATB[15:0]																xxxx
ODCB	0E1A	ODCB[15:0]																0000
CNENB	0E1C	CNIEB[15:0]																0000
CNPUB	0E1E	CNPUB[15:0]																0000
CNPDB	0E20	CNPDB[15:0]																0000
ANSELB	0E22	—	—	—	—	—	—	ANSB[9:7]			—	—	—	ANSB[3:0]				038F
SR1B	0E24	—	—	—	—	—	—	SR1B[9:7]			—	—	SR1B4	—	—	—	—	0000
SR0B	0E26	—	—	—	—	—	—	SR0B[9:7]			—	—	SR0B4	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-35: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E14	TRISB[15:0]																DF9F
PORTB	0E16	RB[15:0]																xxxx
LATB	0E18	LATB[15:0]																xxxx
ODCB	0E1A	ODCB[15:0]																0000
CNENB	0E1C	CNIEB[15:0]																0000
CNPUB	0E1E	CNPUB[15:0]																0000
CNPDB	0E20	CNPDB[15:0]																0000
ANSELB	0E22	—	—	—	—	—	—	ANSB[9:7]			—	—	—	ANSB[3:0]				010F
SR1B	0E24	—	—	—	—	—	—	SR1B[9:7]			—	—	SR1B4	—	—	—	—	0000
SR0B	0E26	—	—	—	—	—	—	SR0B[9:7]			—	—	SR0B4	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-36: PORTB REGISTER MAP FOR dsPIC33EVXXXGMX02 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E14	TRISB[15:0]																DF9F
PORTB	0E16	RB[15:0]																xxxx
LATB	0E18	LATB[15:0]																xxxx
ODCB	0E1A	ODCB[15:0]																0000
CNENB	0E1C	CNIEB[15:0]																0000
CNPUB	0E1E	CNPUB[15:0]																0000
CNPDB	0E20	CNPDB[15:0]																0000
ANSELB	0E22	—	—	—	—	—	—	ANSB[9:7]			—	—	—	ANSB[3:0]				010F
SR1B	0E24	—	—	—	—	—	—	SR1B[9:7]			—	—	SR1B4	—	—	—	—	0000
SR0B	0E26	—	—	—	—	—	—	SR0B[9:7]			—	—	SR0B4	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-37: PORTC REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E28	TRISC15	—	TRISC[13:0]														BFFF
PORTC	0E2A	RC15	—	RC[13:0]														xxxx
LATC	0E2C	LATC15	—	LATC[13:0]														xxxx
ODCC	0E2E	ODCC15	—	ODCC[13:0]														0000
CNENC	0E30	CNIEC15	—	CNIEC[13:0]														0000
CNPUC	0E32	CNPUC15	—	CNPUC[13:0]														0000
CNPDC	0E34	CNPDC15	—	CNPDC[13:0]														0000
ANSELC	0E36	—	—	—	ANSC[12:0]													1FFF
SR1C	0E38	—	—	—	—	—	—	SR1C[9:6]				—	—	SR1C3	—	—	—	0000
SR0C	0E3A	—	—	—	—	—	—	SR0C[9:6]				—	—	SR0C3	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-38: PORTC REGISTER MAP FOR dsPIC33EVXXXGMX04 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISC	0E28	—	—	—	—	—	—	TRISC[9:0]										BFFF
PORTC	0E2A	—	—	—	—	—	—	RC[9:0]										xxxx
LATC	0E2C	—	—	—	—	—	—	LATC[9:0]										xxxx
ODCC	0E2E	—	—	—	—	—	—	ODCC[9:0]										0000
CNENC	0E30	—	—	—	—	—	—	CNIEC[9:0]										0000
CNPUC	0E32	—	—	—	—	—	—	CNPUC[9:0]										0000
CNPDC	0E34	—	—	—	—	—	—	CNPDC[9:0]										0000
ANSELC	0E36	—	—	—	—	—	—	ANSC[9:0]										0807
SR1C	0E38	—	—	—	—	—	—	SR1C[9:6]				—	—	SR1C3	—	—	—	0000
SR0C	0E3A	—	—	—	—	—	—	SR0C[9:6]				—	—	SR0C3	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-39: PORTD REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISD	0E3C	—	—	—	—	—	—	—	TRISD8	—	TRISD[6:5]		—	—	—	—	—	0160
PORTD	0E3E	—	—	—	—	—	—	—	RD8	—	RD[6:5]		—	—	—	—	—	xxxx
LATD	0E40	—	—	—	—	—	—	—	LATD8	—	LATD[6:5]		—	—	—	—	—	xxxx
ODCD	0E42	—	—	—	—	—	—	—	ODCD8	—	ODCD[6:5]		—	—	—	—	—	0000
CNEND	0E44	—	—	—	—	—	—	—	CNIED8	—	CNIED[6:5]		—	—	—	—	—	0000
CNPUD	0E46	—	—	—	—	—	—	—	CNPUD8	—	CNPUD[6:5]		—	—	—	—	—	0000
CNPDD	0E48	—	—	—	—	—	—	—	CNPDD8	—	CNPDD[6:5]		—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-40: PORTE REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E50	TRISE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E52	RE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E54	LATE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E56	ODCE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E58	CNIEE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E5A	CNPUE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E5C	CNPDE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E5E	ANSE[15:12]				—	—	—	—	—	—	—	—	—	—	—	—	F000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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TABLE 4-41: PORTF REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E64	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF[1:0]		0003
PORTF	0E66	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF[1:0]		xxxx
LATF	0E68	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF[1:0]		xxxx
ODCF	0E6A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF[1:0]		0000
CNENF	0E6C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF[1:0]		0000
CNPUF	0E6E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF[1:0]		0000
CNPDF	0E70	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPDF[1:0]		0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-42: PORTG REGISTER MAP FOR dsPIC33EVXXXGMX06 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E78	—	—	—	—	—	—	TRISG[9:6]				—	—	—	—	—	—	03C0
PORTG	0E7A	—	—	—	—	—	—	RG[9:6]				—	—	—	—	—	—	xxxx
LATG	0E7C	—	—	—	—	—	—	LATG[9:6]				—	—	—	—	—	—	xxxx
ODCG	0E7E	—	—	—	—	—	—	ODCG[9:6]				—	—	—	—	—	—	0000
CNENG	0E80	—	—	—	—	—	—	CNIEG[9:6]				—	—	—	—	—	—	0000
CNPUG	0E82	—	—	—	—	—	—	CNPUG[9:6]				—	—	—	—	—	—	0000
CNPDG	0E84	—	—	—	—	—	—	CNPDG[9:6]				—	—	—	—	—	—	0000
ANSELG	0E86	—	—	—	—	—	—	ANSG[9:6]				—	—	—	—	—	—	0000

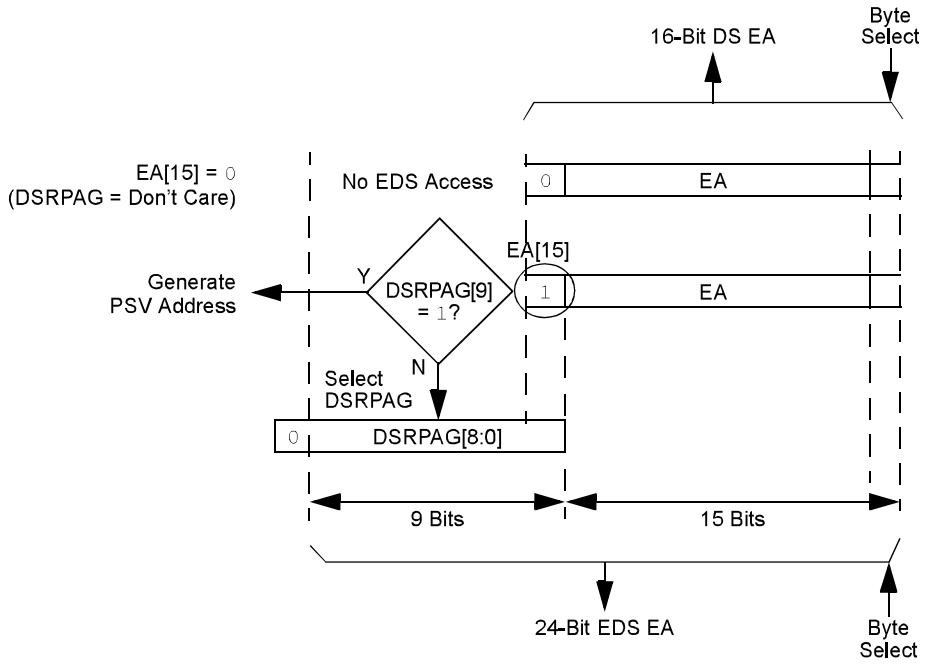
Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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4.3.1 PAGED MEMORY SCHEME

The dsPIC33EVXXXGM00X/10X family architecture extends the available DS through a paging scheme, which allows the available DS to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the Base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Data Space Read Page register (DSRPAG) or the 9-bit Data Space Write Page register (DSWPAG), to form an EDS address, or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space. Construction of the EDS address is shown in Figure 4-9 and Figure 4-10. When DSRPAG[9] = 0 and the base address bit, EA[15] = 1, the DSRPAG[8:0] bits are concatenated onto EA[14:0] to form the 24-bit EDS read address. Similarly, when the base address bit, EA[15] = 1, the DSWPAG[8:0] bits are concatenated onto EA[14:0] to form the 24-bit EDS write address.

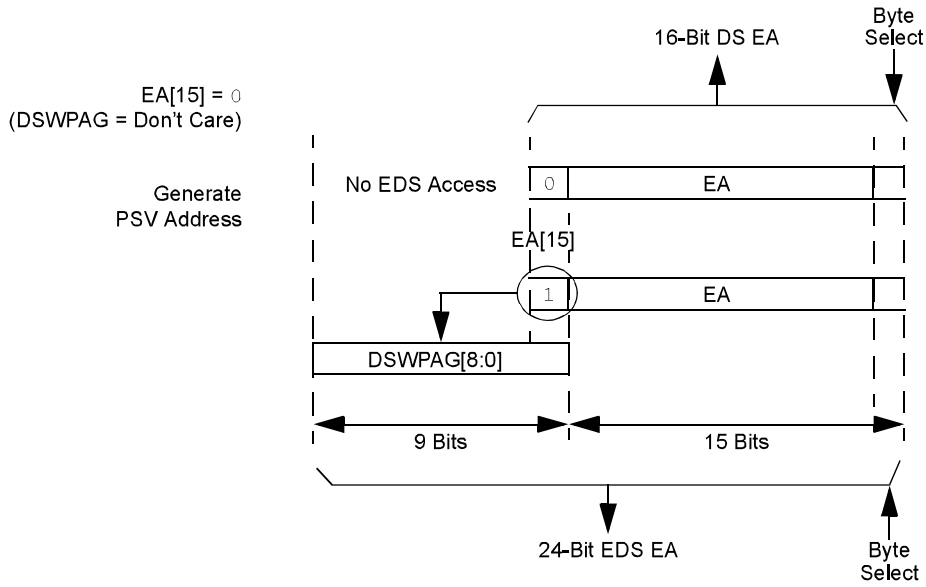
FIGURE 4-9: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION



Note: DS read access when DSRPAG = 0x000 will force an address error trap.

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FIGURE 4-10: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION

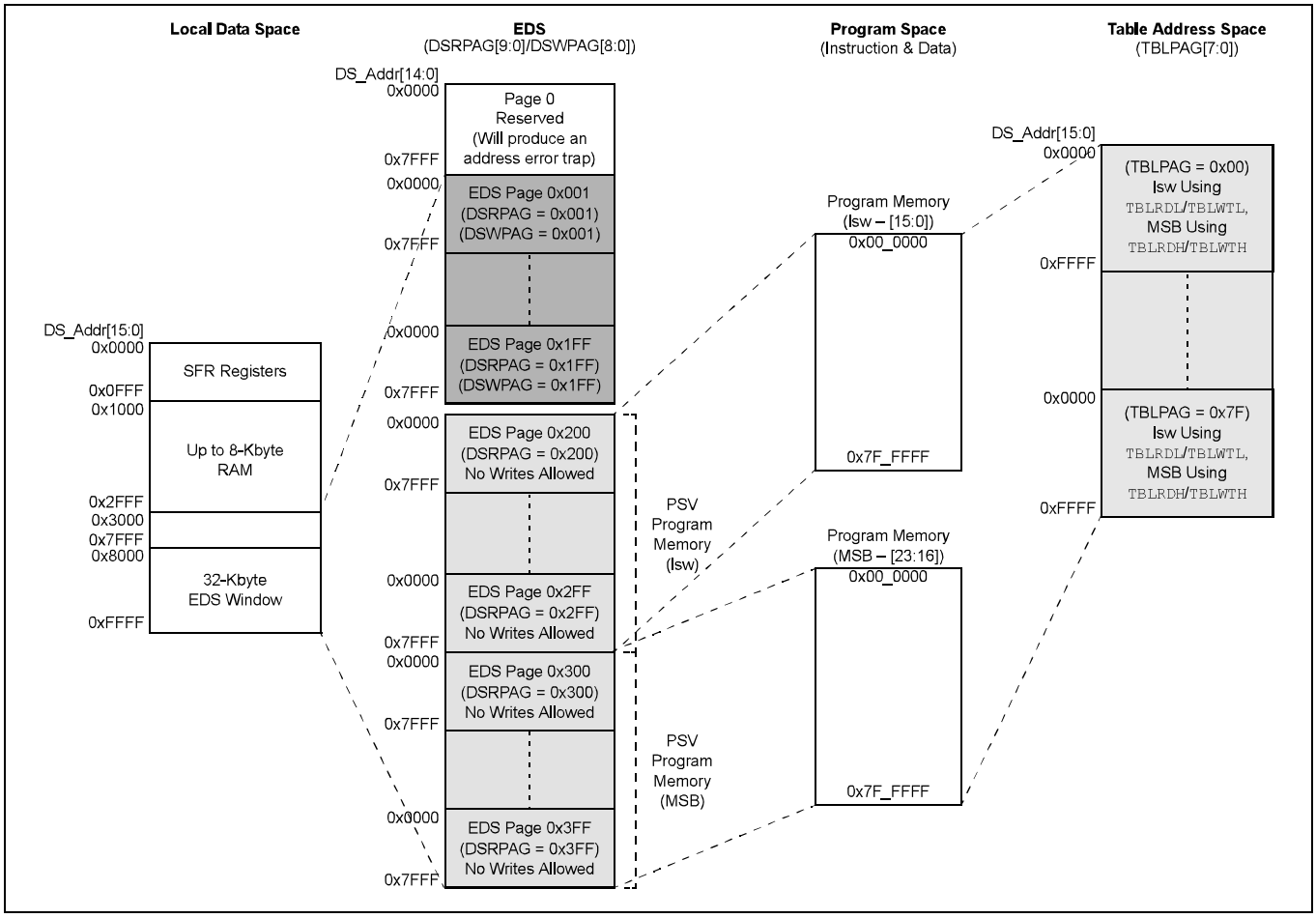


Note: DS read access when DSRPAG = 0x000 will force an address error trap.

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Figure 4-11.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, therefore, the DSWPAG is dedicated to DS, including EDS. The Data Space and EDS can be read from and written to using DSRPAG and DSWPAG, respectively.

FIGURE 4-11: PAGED DATA MEMORY SPACE



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Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in the data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configure the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA[15] is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address, prior to modification, addresses an EDS or a PSV page.
- The EA calculation uses Pre- or Post-Modified Register Indirect Addressing. However, this does not include Register Offset Addressing.

In general, when an overflow is detected, the DSxPAG register is incremented and the EA[15] bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA[15] bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using the Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-43 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when an overflow or underflow occurs, the EA[15] bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

TABLE 4-43: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS AND PSV SPACE BOUNDARIES(2,3,4)

O/U, R/W	Operation	Before			After		
		DSxPAG	DS EA[15]	Page Description	DSxPAG	DS EA[15]	Page Description
O, Read	[++Wn] or [Wn++]	DSRPAG = 0x1FF	1	EDS: Last Page	DSRPAG = 0x1FF	0	See **Note 1**
O, Read		DSRPAG = 0x2FF	1	PSV: Last lsw Page	DSRPAG = 0x300	1	PSV: First MSB Page
O, Read		DSRPAG = 0x3FF	1	PSV: Last MSB Page	DSRPAG = 0x3FF	0	See **Note 1**
O, Write		DSWPAG = 0x1FF	1	EDS: Last Page	DSWPAG = 0x1FF	0	See **Note 1**
U, Read	[--Wn] or [Wn--]	DSRPAG = 0x001	1	PSV Page	DSRPAG = 0x001	0	See **Note 1**
U, Read		DSRPAG = 0x200	1	PSV: First lsw Page	DSRPAG = 0x200	0	See **Note 1**
U, Read		DSRPAG = 0x300	1	PSV: First MSB Page	DSRPAG = 0x2FF	1	PSV: Last lsw Page

Legend: O = Overflow, U = Underflow, R = Read, W = Write

Note 1: The Register Indirect Addressing now addresses a location in the Base Data Space (0x0000-0x8000).

2: An EDS access with DSxPAG = 0x000 will generate an address error trap.

3: Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

4: Pseudolinear Addressing is not supported for large offsets.

4.3.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x2FFF, is always accessible regardless of the contents of the Data Space Page registers; it is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x002FFF with the base address bit, EA[15] = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of Base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, the DSRPAG and DSWPAG registers are initialized to 0x001 at Reset.

Note 1: DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

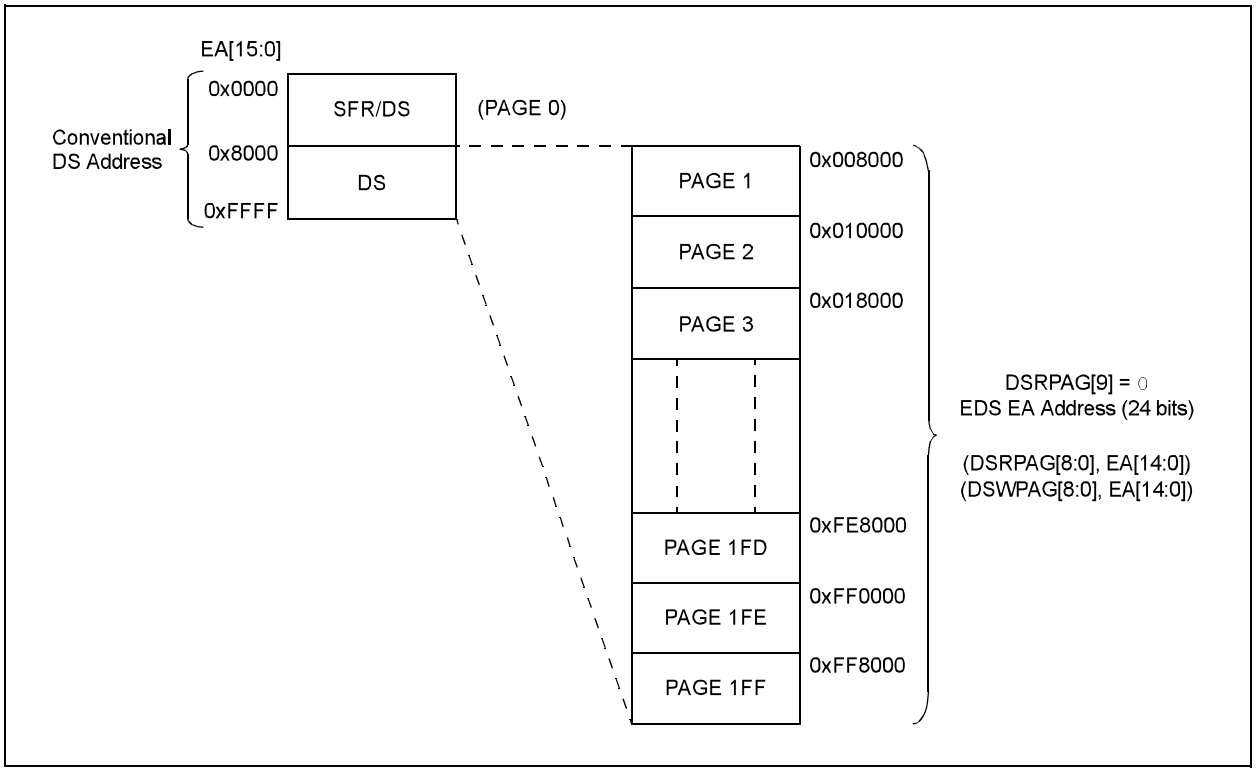
2: Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where the base address bit, EA[15] = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF of the Data Space, will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-12.

For more information on the PSV page access using Data Space Page registers, refer to **Section 5.0 "Program Space Visibility from Data Space"** in **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) of the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 4-12: EDS MEMORY MAP



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4.3.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the MPLAB® ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the MPLAB ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are listed in Table 4-44.

Figure 4-13 shows the arbiter architecture.

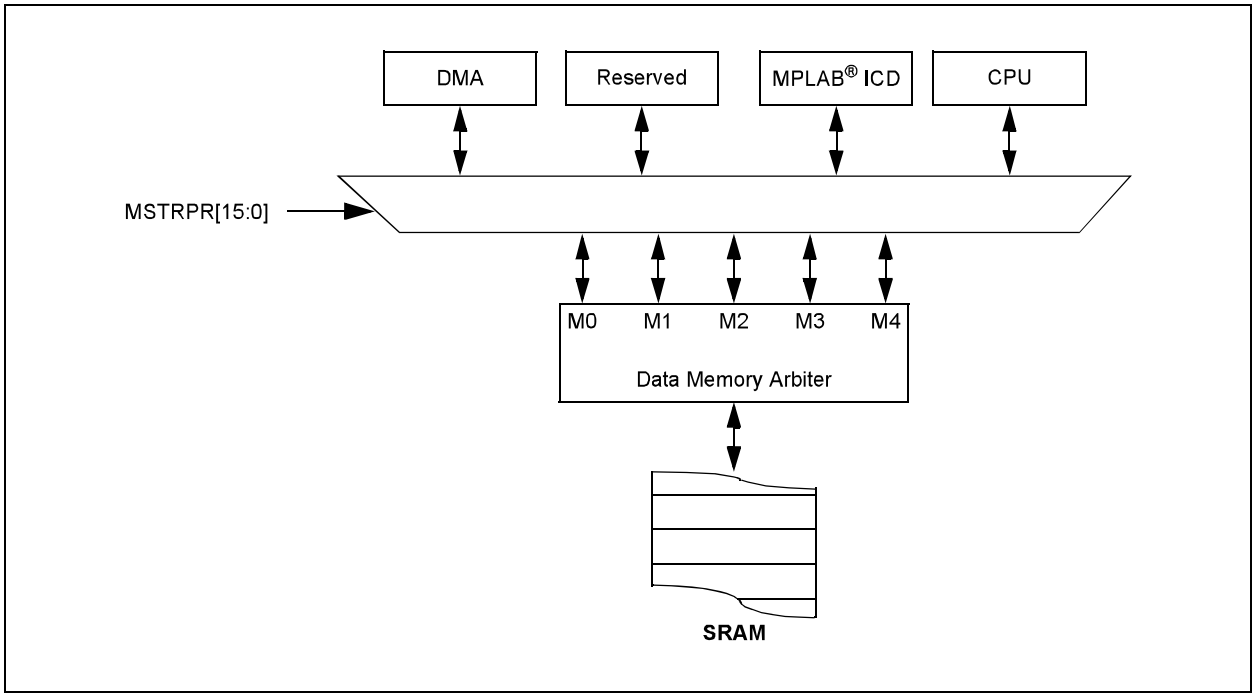
The bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

TABLE 4-44: DATA MEMORY BUS ARBITER PRIORITY

Priority	MSTRPR[15:0] Bit Setting(1)	
	0x0000	0x0020
M0 (highest)	CPU	DMA
M1	Reserved	CPU
M2	Reserved	Reserved
M3	DMA	Reserved
M4 (lowest)	MPLAB® ICD	MPLAB ICD

Note 1: All other values of MSTRPR[15:0] are reserved.

FIGURE 4-13: ARBITER ARCHITECTURE



4.3.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating the SSP (for example, creating stack frames).

Note:	To protect against misaligned stack accesses, W15[0] is fixed to '0' by the hardware.

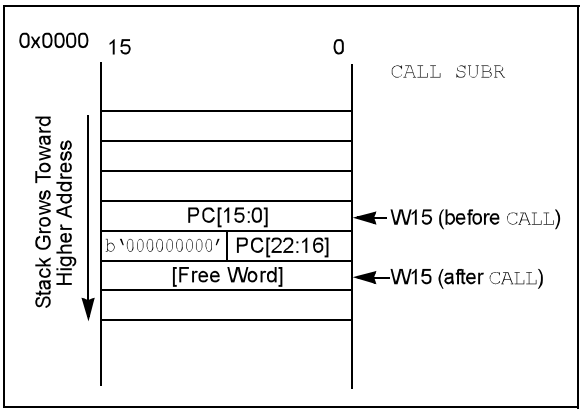
W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EVXXXGM00X/10X family devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within the Data Space.

The SSP always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-14 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC[15:0] are pushed onto the first available stack word, then PC[22:16] are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-14. During exception processing, the MSB of the PC is concatenated with the lower eight bits of the CPU STATUS Register (SR). This allows the contents of SRL to be preserved automatically during interrupt processing.

Note 1:	To maintain system SSP (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
2:	As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a 'C' development environment.

FIGURE 4-14: CALL STACK FRAME



4.4 Instruction Addressing Modes

The addressing modes shown in Table 4-45 form the basis of the addressing modes optimized to support the specific features of the individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.4.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.4.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where, Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note:	Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

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TABLE 4-45: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

4.4.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions and the DSP accumulator class of instructions provide a greater addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.4.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set, {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must, therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X Data Space) and W11 (in Y Data Space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.4.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (Branch) instructions use 16-bit signed literals to specify the Branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

4.5 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing, since these two registers are used as the SFP and SSP, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.5.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note:	Y Data Space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.5.2 W ADDRESS REGISTER SELECTION

The Modulo and Bit-Reversed Addressing Control register, MODCON[15:0], contains enable flags, as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

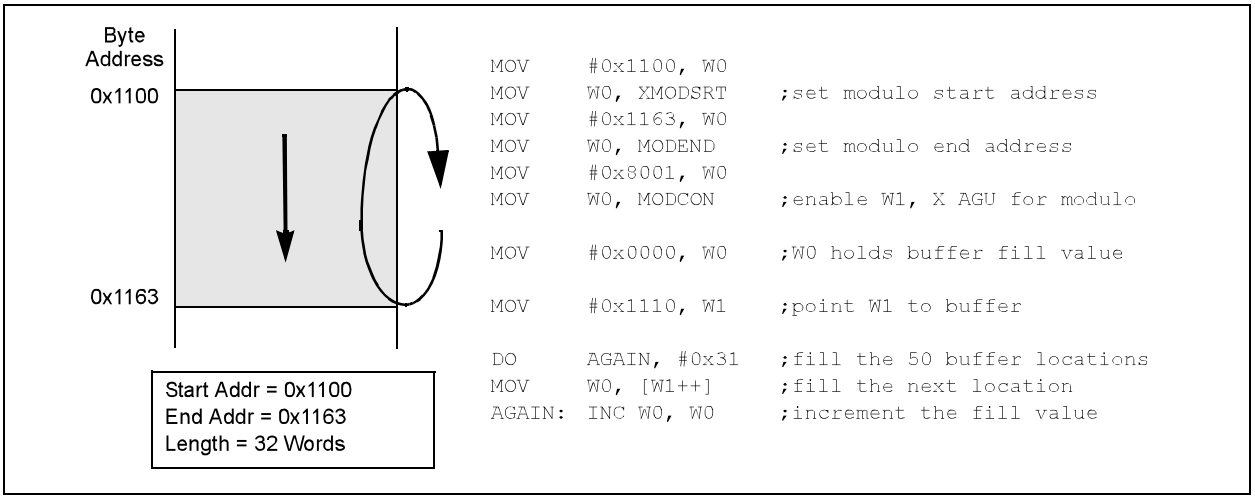
- If XWM = `1111`, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = `1111`, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM) to which Modulo Addressing is to be applied is stored in MODCON[3:0] (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit (MODCON[15]) is set

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON[7:4]. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit (MODCON[14]) is set.

Figure 4-15 shows an example of Modulo Addressing operation.

FIGURE 4-15: MODULO ADDRESSING OPERATION EXAMPLE



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4.5.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

The address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note:	The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset, such as [W7 + W2] is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.6 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.6.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all of these conditions are met:

- BWM[3:0] bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is M = 2^N bytes, the last 'N' bits of the data buffer start address must be zeros.

XB[14:0] is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data are a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV[15]) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

The operation of Bit-Reversed Addressing is shown in Figure 4-16 and Table 4-46.

FIGURE 4-16: BIT-REVERSED ADDRESSING EXAMPLE

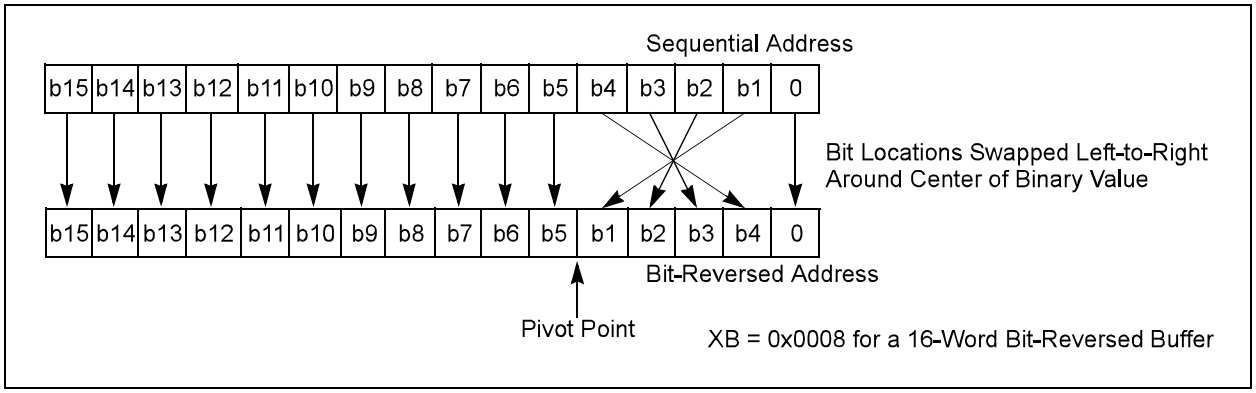


TABLE 4-46: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

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4.7 Interfacing Program and Data Memory Spaces

The dsPIC33EVXXXGM00X/10X family architecture uses a 24-bit wide Program Space and a 16-bit wide Data Space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use these data successfully, they must be accessed in a way that preserves the alignment of information in both the spaces.

Aside from normal execution, the architecture of the dsPIC33EVXXXGM00X/10X family devices provides two methods by which Program Space can be accessed during operation:

- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

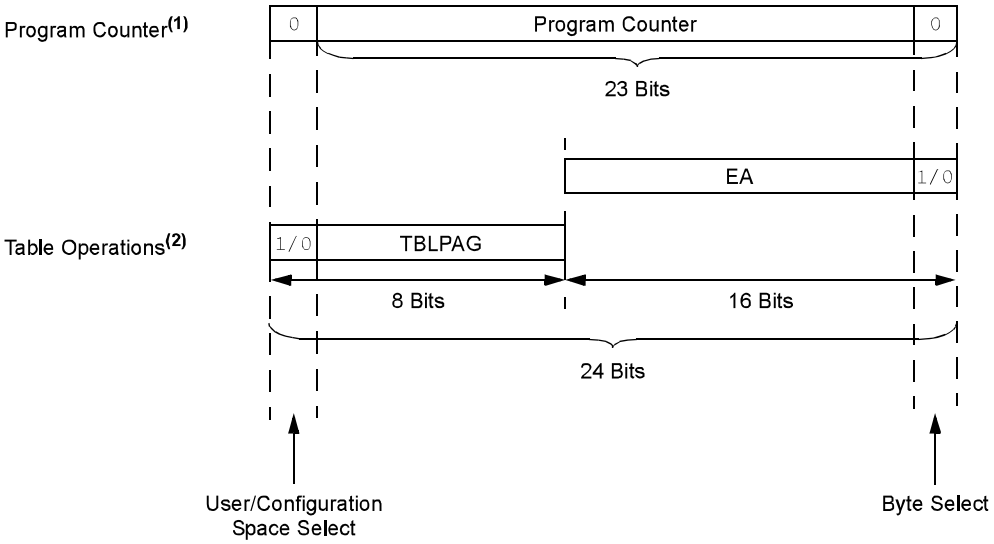
Table 4-47 shows the construction of the Program Space address.

How the data are accessed from Program Space is shown in Figure 4-17.

TABLE 4-47: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		[23]	[22:16]	[15]	[14:1]	[0]
Instruction Access (Code Execution)	User	0	PC[22:1]			0
		0xx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG[7:0]		Data EA[15:0]		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG[7:0]		Data EA[15:0]		
		1xxx xxxx		xxxx xxxx xxxx xxxx		

FIGURE 4-17: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

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4.7.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through the Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper eight bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. The TBLRDL and TBLWTL instructions access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

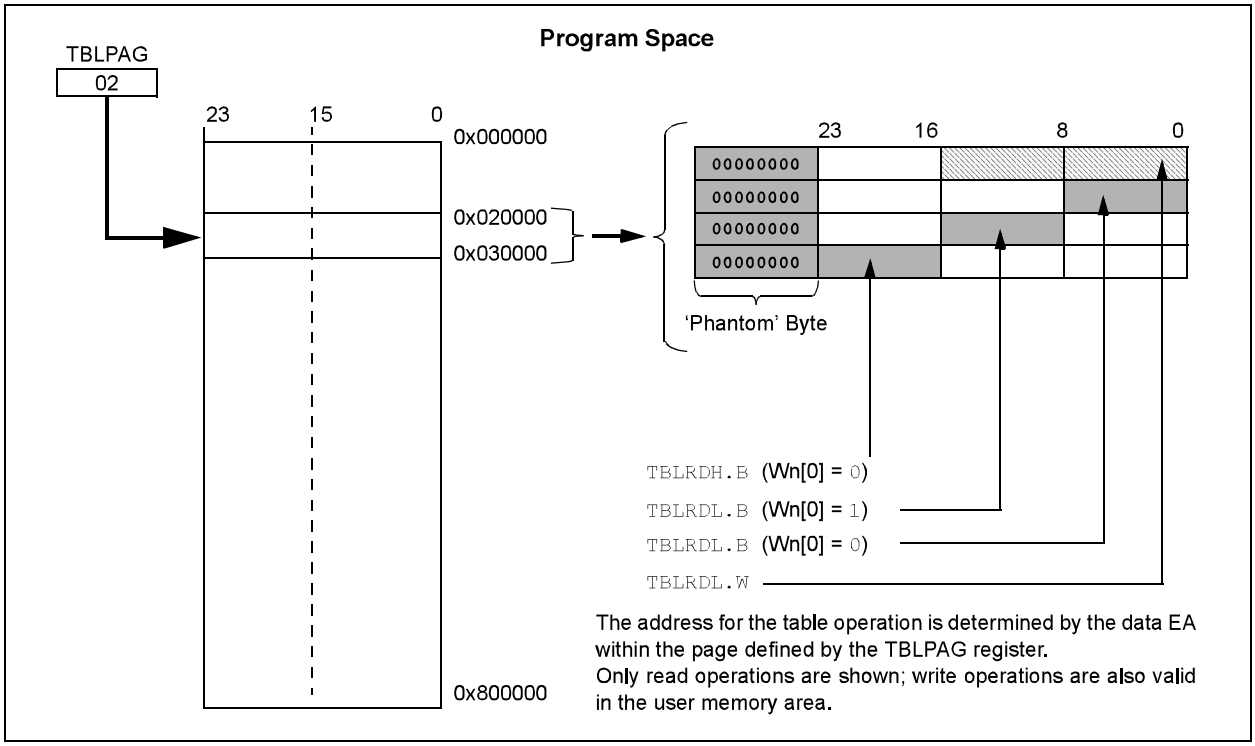
Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P[15:0]) to a data address (D[15:0]).
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P[23:16]) to a data address. The 'phantom' byte (D[15:8]) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D[7:0] of the data address, as in the TBLRDL instruction. The data are always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

Similarly, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG[7] = 0, the table page is located in the user memory space. When TBLPAG[7] = 1, the page is located in configuration space. Accessing the program memory with table instructions is shown in Figure 4-18.

FIGURE 4-18: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS



NOTES:

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5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Flash Programming"** (www.microchip.com/DS70000609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

The Flash memory can be programmed in the following three ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)

ICSP allows for a dsPIC33EVXXXGM00X/10X family device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (PGECx/PGEDx) lines, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

Enhanced ICSP uses an on-board bootloader, known as the Program Executive (PE), to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, refer to the specific device programming specification.

RTSP is accomplished using the TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data as a double program memory word, a row of 64 instructions (192 bytes) and erase program memory in blocks of 512 instruction words (1536 bytes) at a time.

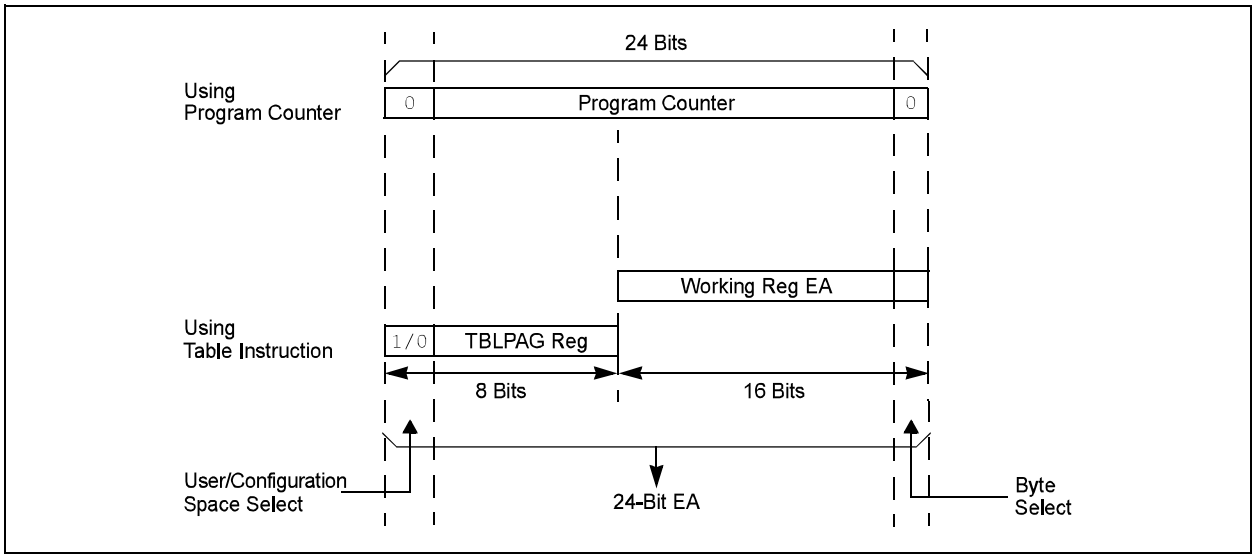
5.1 Table Instructions and Flash Programming

The Flash memory read and the double-word programming operations make use of the TBLRD and TBLWT instructions, respectively. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits[7:0] of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits[15:0] of the program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits[23:16] of the program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory, program a row and to program two instruction words at a time. See Table 1 in the **"dsPIC33EVXXXGM00X/10X Product Families"** section for the page sizes of each device.memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to era

The Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of program memory, which consists of eight rows (512 instructions) at a time, and to program one row or two adjacent words at a time. The 8-row erase pages and single row write rows are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively. Table 30-13 in **Section 30.0 "Electrical Characteristics"** lists the typical erase and programming times.

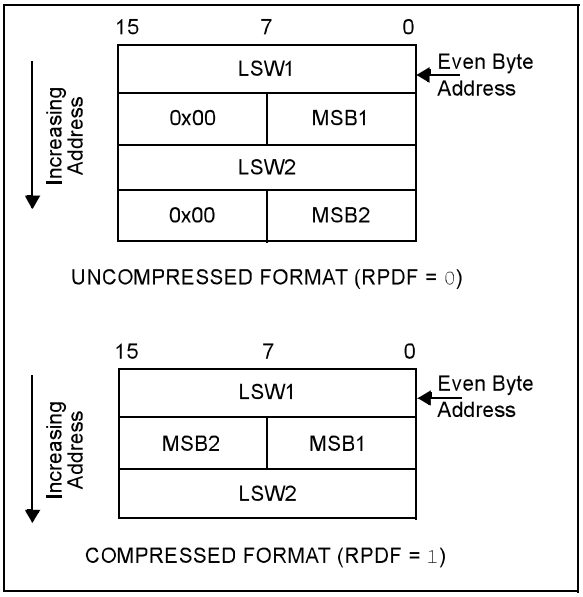
The basic sequence for RTSP word programming is to use the TBLWTL and TBLWTH instructions to load two of the 24-bit instructions into the write latches found in configuration memory space. See Figure 4-1 to Figure 4-5 for write latch addresses. Programming is performed by unlocking and setting the control bits in the NVMCON register.

Row programming is performed by loading 192 bytes into data memory and then loading the address of the first byte in that row into the NVMSRCADR register. Once the write has been initiated, the device will automatically load the write latches and increment the NVMSRCADR and the NVMADR(U) registers until all bytes have been programmed. The RPDF bit (NVMCON[9]) selects the format of the stored data in RAM to be either compressed or uncompressed. See Figure 5-2 for data formatting. Compressed data help to reduce the amount of required RAM by using the upper byte of the second word for the MSB of the second instruction.

For more information on erasing and programming the Flash memory, refer to **"Flash Programming"** (www.microchip.com/DS70000609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

Note 1:	Before reprogramming either of the two words in a double-word pair, the user must erase the Flash memory page in which it is located.
2:	Before reprogramming any word in a row, the user must erase the Flash memory page in which it is located.

FIGURE 5-2: UNCOMPRESSED/ COMPRESSED FORMAT



5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished. Setting the WR bit (NVMCON[15]) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, erase the page that contains the desired address of the location the user wants to change. For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Refer to **"Flash Programming"** (www.microchip.com/DS70000609) in the "*dsPIC33/PIC24 Family Reference Manual*" for details and code examples on programming using RTSP.

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5.4 Error Correcting Code (ECC)

In order to improve program memory performance and durability, these devices include Error Correcting Code functionality (ECC) as an integral part of the Flash memory controller. ECC can determine the presence of single bit errors in program data, including which bit is in error, and correct the data automatically without user intervention. ECC cannot be disabled.

When data are written to program memory, ECC generates a 7-bit Hamming code parity value for every two (24-bit) instruction words. The data are stored in blocks of 48 data bits and seven parity bits; parity data are not memory-mapped and are inaccessible. When the data are read back, the ECC calculates the parity on them and compares it to the previously stored parity value. If a parity mismatch occurs, there are two possible outcomes:

- Single bit errors are automatically identified and corrected on read-back. An optional device-level interrupt (ECCSBEIF) is also generated.
- Double-bit errors will generate a generic hard trap and the read data are not changed. If special exception handling for the trap is not implemented, a device Reset will also occur.

To use the single bit error interrupt, set the ECC Single Bit Error Interrupt Enable bit (ECCSBEIE) and configure the ECCSBEIP bits to set the appropriate interrupt priority.

Except for the single bit error interrupt, error events are not captured or counted by hardware. This functionality can be implemented in the software application, but it is the user's responsibility to do so.

5.5 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

5.5.1 KEY RESOURCES

- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

5.6 Control Registers

The following five SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADR, NVMADRU and NVMSRCADR.

The NVMCON register (Register 5-1) selects the operation to be performed (page erase, word/row program, inactive panel erase) and initiates the program/erase cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word/row for programming operations or the selected page for erase operations. The NVMADRU register is used to hold the upper eight bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA. For row programming operation, data to be written to program Flash memory are written into data memory space (RAM) at an address defined by the NVMSRCADR register (location of the first element in row programming data).

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
WR(1)	WREN(1)	WRERR(1)	NVMSIDL(2)	—	—	RPDF	URERR
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	NVMOP3(1,3,4)	NVMOP2(1,3,4)	NVMOP1(1,3,4)	NVMOP0(1,3,4)
bit 7							bit 0

Legend:	SO = Settable Only bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Flash program or erase operations are enabled
- 0 = Flash program or erase operations are inhibited

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
- 1 = Primary Flash operation discontinues when the device enters Idle mode
- 0 = Primary Flash operation continues when the device enters Idle mode.

bit 11-10 **Unimplemented:** Read as '0'

bit 9 **RPDF:** Row Programming Data Format Control bit
- 1 = Row data to be stored in RAM are in a compressed format
- 0 = Row data to be stored in RAM are in an uncompressed format

bit 8 **URERR:** Row Programming Data Underrun Error Flag bit
- 1 = Row programming operation has been terminated due to a data underrun error
- 0 = No data underrun has occurred

bit 7-4 **Unimplemented:** Read as '0'

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (I_{IDLE}), and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.

3: All other combinations of NVMOP[3:0] are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

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REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER (CONTINUED)

bit 3-0 **NVMOP[3:0]:** NVM Operation Select bits(1,3,4)

1111 = Reserved
1110 = User memory and executive memory bulk erase operation
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0101 = Reserved
0100 = Reserved
0011 = Memory page erase operation
0010 = Memory row program operation
0001 = Memory double word(5)
0000 = Reserved

Note 1: These bits can only be reset on a POR.

2: If this bit is set, there will be minimal power savings (IIDLE), and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.

3: All other combinations of NVMOP[3:0] are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADRU[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADRU[23:16]:** NVM Memory Upper Write Address bits

Selects the upper eight bits of the location to program or erase in program Flash memory. This register may be read or written to by the user application.

REGISTER 5-3: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **NVMADR[15:0]:** NVM Memory Lower Write Address bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written to by the user application.

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REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY[7:0]:** NVM Key Register bits (write-only)

REGISTER 5-5: NVMSRCADRH: NVM DATA MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADR[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMSRCADRH[23:16]:** Data Memory Upper Address bits

REGISTER 5-6: NVMSRCADRL: NVM DATA MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADR[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	r-0
NVMSRCADR[7:1]							—
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **NVMSRCADRL[15:1]:** Data Memory Lower Address bits

bit 0 **Reserved:** Maintain as '0'

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6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Reset"** (www.microchip.com/DS70602) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{SYSRST}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{MCLR}$: Master Clear Pin Reset
- SWR: `RESET` Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset
  - Illegal Address Mode Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{SYSRST}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 "Memory Organization"** of this device data sheet for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

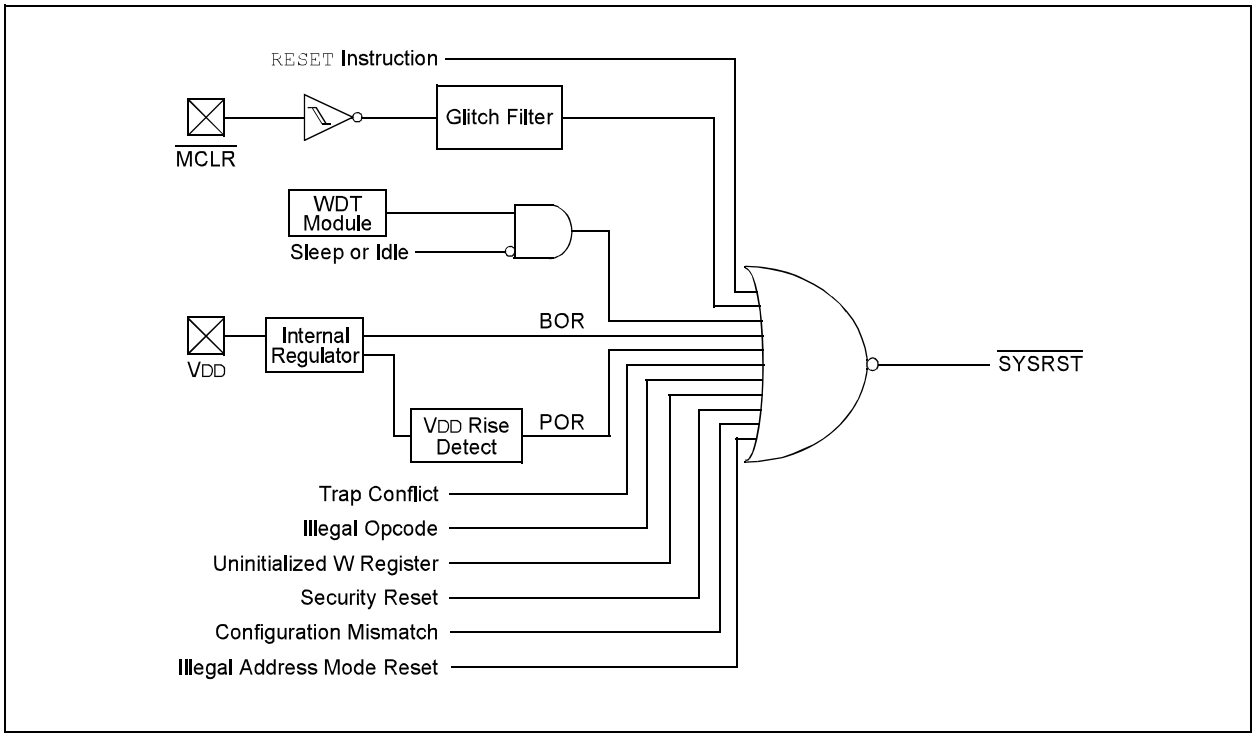
A POR clears all the bits, except for the POR and BOR bits (RCON[1:0]) that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in the other sections of this device data sheet.

Note: The status bits in the RCON register should be cleared after they are read. Therefore, the next RCON register value after a device Reset is meaningful.

Note: In all types of Resets, to select the device clock source, the contents of OSCCON are initialized from the FNOSCx Configuration bits in the FOSCSEL Configuration register.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM



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REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	R/W-0
TRAPR	IOPUWR	—	—	VREGSF	—	CM	VREGS
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EXTR	SWR	SWDTEN(2)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Register Access Reset Flag bit
1 = An Illegal Opcode detection or an Illegal Address mode, or Uninitialized W register used as an Address Pointer caused a Reset
0 = An Illegal Opcode Reset or Uninitialized W Register Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash voltage regulator is active during Sleep mode
0 = Flash voltage regulator goes into Standby mode during Sleep mode

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN[1:0] Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN[1:0] Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

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7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EVXXXGM00X/10X CPU. The Interrupt Vector Table (IVT) provides 246 interrupt sources (unused sources are reserved for future use) that can be programmed with different priority levels.

The interrupt controller has the following features:

- Interrupt Vector Table with up to 246 Vectors
- Alternate Interrupt Vector Table (AIVT)
- Up to Eight Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Software can Generate any Peripheral Interrupt
- Alternate Interrupt Vector Table (AIVT) is available if Boot Security is Enabled and AIVTEN = 1

7.1 Interrupt Vector Table

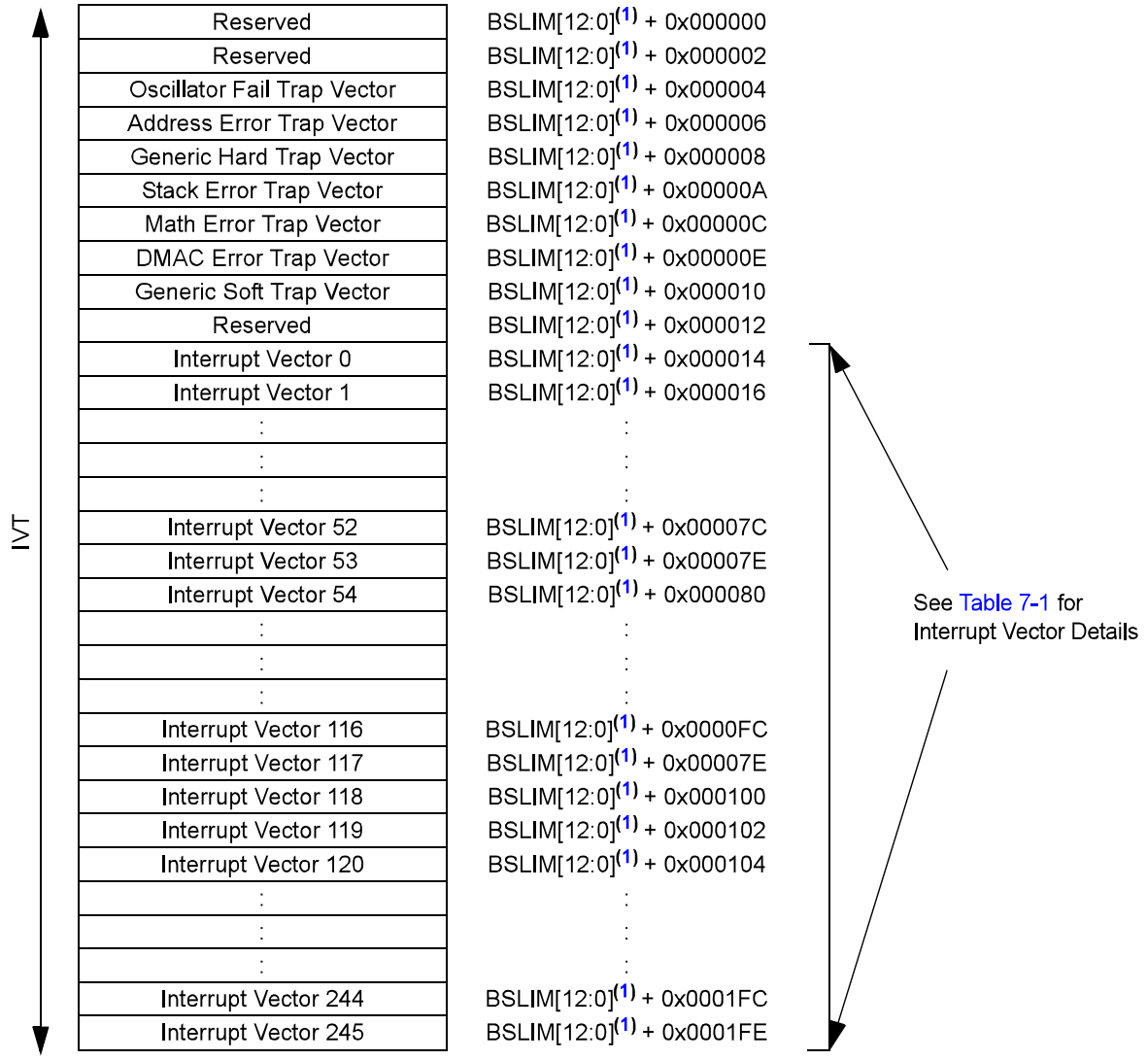
The dsPIC33EVXXXGM00X/10X family IVT, shown in Figure 7-2, resides in program memory, starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 187 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Alternate Interrupt Vector Table

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-1, is available if the Boot Segment (BS) is defined, the AIVTEN bit is set in the INTCON2 register and if the AIVTDIS Configuration bit is set to '1'. The AIVT begins at the start of the last page of the Boot Segment.

FIGURE 7-1: dsPIC33EVXXXGM00X/10X FAMILY ALTERNATE INTERRUPT VECTOR TABLE



Note 1: The address depends on the size of the Boot Segment defined by BSLIM[12:0]: [(BSLIM[12:0] – 1) x 0x400] + Offset.

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FIGURE 7-2: dsPIC33EVXXXGM00X/10X FAMILY INTERRUPT VECTOR TABLE

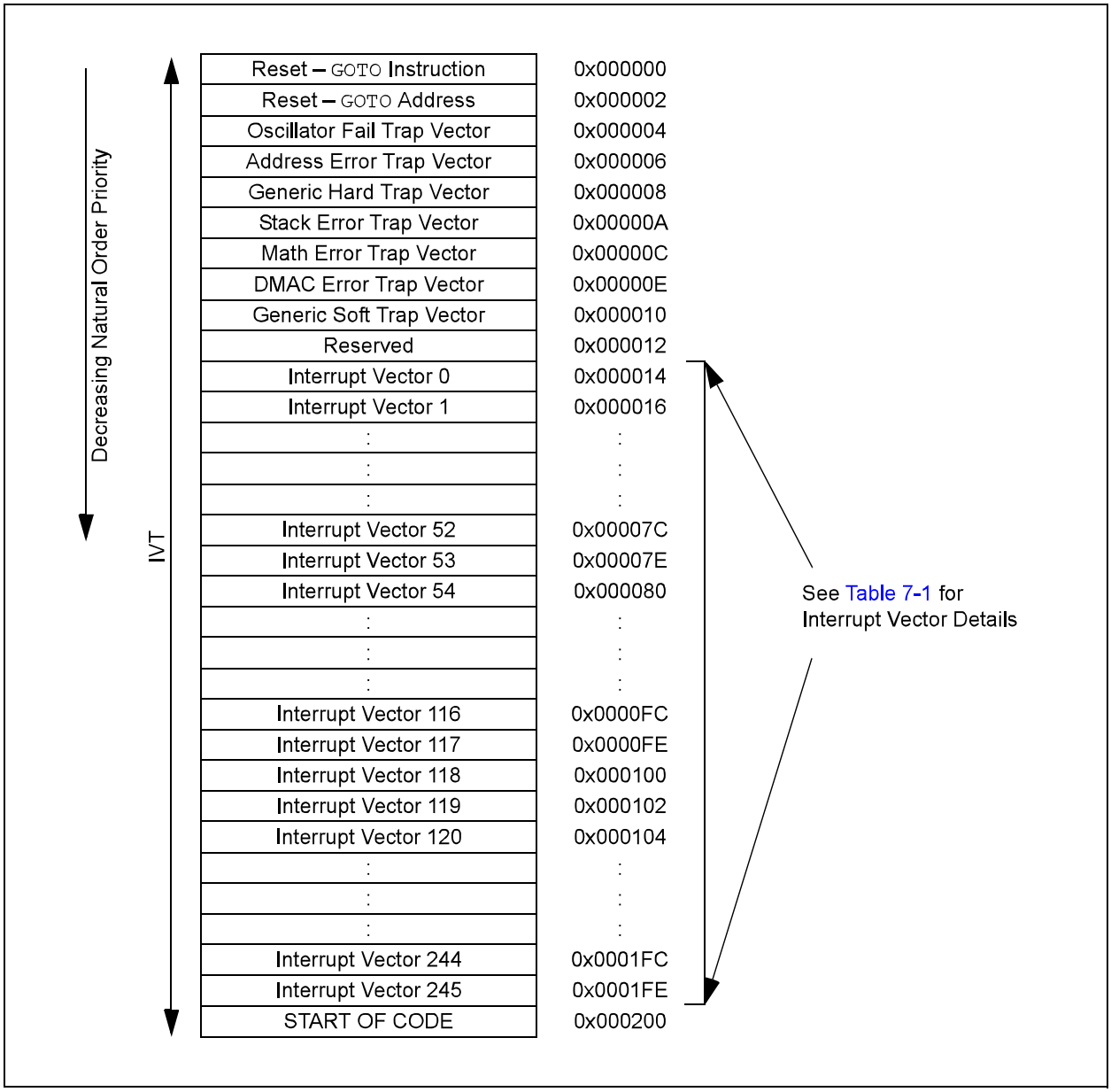


TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector No.	IRQ No.	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
External Interrupt 0 (INT0)	8	0	0x000014	IFS0[0]	IEC0[0]	IPC0[2:0]
Input Capture 1 (IC1)	9	1	0x000016	IFS0[1]	IEC0[1]	IPC0[6:4]
Output Compare 1 (OC1)	10	2	0x000018	IFS0[2]	IEC0[2]	IPC0[10:8]
Timer1 (T1)	11	3	0x00001A	IFS0[3]	IEC0[3]	IPC0[14:12]
DMA Channel 0 (DMA0)	12	4	0x00001C	IFS0[4]	IEC0[4]	IPC1[2:0]
Input Capture 2 (IC2)	13	5	0x00001E	IFS0[5]	IEC0[5]	IPC1[6:4]
Output Compare 2 (OC2)	14	6	0x000020	IFS0[6]	IEC0[6]	IPC1[10:8]
Timer2 (T2)	15	7	0x000022	IFS0[7]	IEC0[7]	IPC1[14:12]
Timer3 (T3)	16	8	0x000024	IFS0[8]	IEC0[8]	IPC2[2:0]
SPI1 Error (SPI1E)	17	9	0x000026	IFS0[9]	IEC0[9]	IPC2[6:4]
SPI1 Transfer Done (SPI1)	18	10	0x000028	IFS0[10]	IEC0[10]	IPC2[10:8]
UART1 Receiver (U1RX)	19	11	0x00002A	IFS0[11]	IEC0[11]	IPC2[14:12]
UART1 Transmitter (U1TX)	20	12	0x00002C	IFS0[12]	IEC0[12]	IPC3[2:0]
ADC1 Convert Done (AD1)	21	13	0x00002E	IFS0[13]	IEC0[13]	IPC3[6:4]
DMA Channel 1 (DMA1)	22	14	0x000030	IFS0[14]	IEC0[14]	IPC3[10:8]
NVM Write Complete (NVM)	23	15	0x000032	IFS0[15]	IEC0[15]	IPC3[14:12]
I2C1 Slave Event (SI2C1)	24	16	0x000034	IFS1[0]	IEC1[0]	IPC4[2:0]
I2C1 Master Event (MI2C1)	25	17	0x000036	IFS1[1]	IEC1[1]	IPC4[6:4]
Comparator Combined Event (CMP1)	26	18	0x000038	IFS1[2]	IEC1[2]	IPC4[10:8]
Input Change Interrupt (CN)	27	19	0x00003A	IFS1[3]	IEC1[3]	IPC4[14:12]
External Interrupt 1 (INT1)	28	20	0x00003C	IFS1[4]	IEC1[4]	IPC5[2:0]
DMA Channel 2 (DMA2)	32	24	0x000044	IFS1[8]	IEC1[8]	IPC6[2:0]
Output Compare 3 (OC3)	33	25	0x000046	IFS1[9]	IEC1[9]	IPC6[6:4]
Output Compare 4 (OC4)	34	26	0x000048	IFS1[10]	IEC1[10]	IPC6[10:8]
Timer4 (T4)	35	27	0x00004A	IFS1[11]	IEC1[11]	IPC6[14:12]
Timer5 (T5)	36	28	0x00004C	IFS1[12]	IEC1[12]	IPC7[2:0]
External Interrupt 2 (INT2)	37	29	0x00004E	IFS1[13]	IEC1[13]	IPC7[6:4]
UART2 Receiver (U2RX)	38	30	0x000050	IFS1[14]	IEC1[14]	IPC7[10:8]
UART2 Transmitter (U2TX)	39	31	0x000052	IFS1[15]	IEC1[15]	IPC7[14:12]
SPI2 Error (SPI2E)	40	32	0x000054	IFS2[0]	IEC2[0]	IPC8[2:0]
SPI2 Transfer Done (SPI2)	41	33	0x000056	IFS2[1]	IEC2[1]	IPC8[6:4]
CAN1 RX Data Ready (C1RX)(1)	42	34	0x000058	IFS2[2]	IEC2[2]	IPC8[10:8]
CAN1 Event (C1)(1)	43	35	0x00005A	IFS2[3]	IEC2[3]	IPC8[14:12]
DMA Channel 3 (DMA3)	44	36	0x00005C	IFS2[4]	IEC2[4]	IPC9[2:0]
Input Capture 3 (IC3)	45	37	0x00005E	IFS2[5]	IEC2[5]	IPC9[6:4]
Input Capture 4 (IC4)	46	38	0x000060	IFS2[6]	IEC2[6]	IPC9[10:8]
Reserved	54	46	0x000070	—	—	—
PWM Special Event Match Interrupt (PSEM)	65	57	0x000086	IFS3[9]	IEC3[9]	IPC14[6:4]
Reserved	69	61	0x00008E	—	—	—
Reserved	71-72	63-64	0x000092-0x000094	—	—	—

Note 1: This interrupt source is available on dsPIC33EVXXXGM10X devices only.

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TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector No.	IRQ No.	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
UART1 Error Interrupt (U1E)	73	65	0x000096	IFS4[1]	IEC4[1]	IPC16[6:4]
UART2 Error Interrupt (U2E)	74	66	0x000098	IFS4[2]	IEC4[2]	IPC16[10:8]
Reserved	76-77	68–69	0x00009C-0x00009E	—	—	—
CAN1 TX Data Request (C1TX)(1)	78	70	0x0000A0	IFS4[6]	IEC4[6]	IPC17[10:8]
Reserved	80	72	0x0000A4	—	—	—
Reserved	82	74	0x0000A8	—	—	—
Reserved	84	76	0x0000AC	—	—	—
CTMU Interrupt (CTMU)	85	77	0x0000AE	IFS4[13]	IEC4[13]	IPC19[6:4]
Reserved	86-88	78-80	0x0000B0-0x0000B4	—	—	—
Reserved	92-94	84-86	0x0000BC-0x0000C0	—	—	—
Reserved	100-101	92-93	0x0000CC-0x0000CE	—	—	—
PWM Generator 1 (PWM1)	102	94	0x0000D0	IFS5[14]	IEC5[14]	IPC23[10:8]
PWM Generator 2 (PWM2)	103	95	0x0000D2	IFS5[15]	IEC5[15]	IPC23[14:12]
PWM Generator 3 (PWM3)	104	96	0x0000D4	IFS6[0]	IEC6[0]	IPC24[2:0]
Reserved	108-149	100-141	0x0000DC-0x00012E	—	—	—
ICD Application (ICD)	150	142	0x000142	IFS8[14]	IEC8[14]	IPC35[10:8]
Reserved	152	144	0x000134	—	—	—
Bus Collision (I2C1)	—	173	0x00016E	IFS10[13]	IEC10[13]	IPC43[4:6]
SENT1 Error (SENT1ERR)	—	182	0x000180	IFS11[6]	IEC11[6]	IPC45[10:8]
SENT1 TX/RX (SENT1)	—	183	0x000182	IFS11[7]	IEC11[7]	IPC45[14:12]
SENT2 Error (SENT2ERR)	—	184	0x000184	IFS11[8]	IEC11[8]	IPC46[2:0]
SENT2 TX/RX (SENT2)	—	185	0x000186	IFS11[9]	IEC11[9]	IPC46[6:4]
ECC Single Bit Error (ECCSBE)	—	186	0x000188	IFS11[10]	IEC11[10]	IPC45[10:8]
Reserved	159-245	187-245	0x000142-0x0001FE	—	—	—
Lowest Natural Order Priority						

Note 1: This interrupt source is available on dsPIC33EVXXXGM10X devices only.

7.3 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EVXXXGM00X/10X family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

7.4 Interrupt Control and Status Registers

dsPIC33EVXXXGM00X/10X family devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- IFSx
- IECx
- IPCx
- INTTREG

7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from the INTCON1, INTCON2, INTCON3 and INTCON4 registers.

INTCON1 contains the Interrupt Nesting Disable bit (NSTDIS), as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and also contains the Global Interrupt Enable bit (GIE).

INTCON3 contains the status flags for the DMT (Dead-man Timer), DMA and DO stack overflow status trap sources.

The INTCON4 register contains the ECC Double-Bit Error (ECCDBE) and Software-Generated Hard Trap (SGHT) status bit.

7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared through software.

7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into Vector Number (VECNUM[7:0]) and Interrupt Priority Level bit (ILR[3:0]) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0[0], the INT0IE bit in IEC0[0] and the INT0IP bits in the first position of IPC0 (IPC0[2:0]).

7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers, refer to **"CPU"** (www.microchip.com/DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL[2:0] bits (SR[7:5]). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL[2:0], also indicates the current CPU Interrupt Priority Level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 to Register 7-7.

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REGISTER 7-1: SR: CPU STATUS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(2,3)	IPL1(2,3)	IPL0(2,3)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL[2:0]:** CPU Interrupt Priority Level Status bits(2,3)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

Note 1: For complete register details, see Register 3-1.
2: The IPL[2:0] bits are concatenated with the IPL3 bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL3 = 1. User interrupts are disabled when IPL3 = 1.
3: The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.

REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0
VAR	—	US1	US0	EDT	DL2	DL1	DL0
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-0	R/C-0	R-0	R/W-0	R/W-0
SATA	SATB	SATDW	ACCSAT	IPL3(2)	SFA	RND	IF
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

Note 1: For complete register details, see Register 3-2.
2: The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

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REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBTE	COVTE
bit 15							bit 8

R/W-0	HC/R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMAC Trap Flag bit
1 = DMAC trap has occurred
0 = DMAC trap has not occurred

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

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REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2

R/W-1	R/W-0	R/W-0	U-0	U-0	U-0	U-0	R/W-0
GIE	DISI	SWTRAP	—	—	—	—	AIVTEN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	INT2EP	INT1EP	INT0EP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupts and associated IECx bits are enabled
0 = Interrupts are disabled, but traps are still enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Software trap is enabled
0 = Software trap is disabled

bit 12-9 **Unimplemented:** Read as '0'

bit 8 **AIVTEN:** Alternate Interrupt Vector Table is Enabled bit
1 = AIVT is enabled
0 = AIVT is disabled

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
DMT	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
—	—	DAE	DOOVR	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **DMT:** Deadman Timer (Soft) Trap Status bit
1 = Deadman Timer trap has occurred
0 = Deadman Timer trap has not occurred

bit 14-6 **Unimplemented:** Read as '0'

bit 5 **DAE:** DMA Address Error Soft Trap Status bit
1 = DMA address error soft trap has occurred
0 = DMA address error soft trap has not occurred

bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
1 = DO stack overflow soft trap has occurred
0 = DO stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as '0'

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REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	SC/HS/R-0	SC/HS/R-0
—	—	—	—	—	—	ECCDBE(1)	SGHT
bit 7							bit 0

Legend:	HS = Hardware Settable bit	SC = Software Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **ECCDBE:** ECC Double-Bit Error Trap bit(1)
1 = ECC double-bit error trap has occurred
0 = ECC double-bit error trap has not occurred

bit 0 **SGHT:** Software-Generated Hard Trap Status bit
1 = Software-generated hard trap has occurred
0 = Software-generated hard trap has not occurred

Note 1: ECC double-bit error causes a generic hard trap.

REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	ILR[3:0]		
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VECNUM[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **ILR[3:0]:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7-0 **VECNUM[7:0]:** Vector Number of Pending Interrupt bits
11111111 = 255, Reserved; do not use
•
•
•
00001001 = 9, Input Capture 1 (IC1)
00001000 = 8, External Interrupt 0 (INT0)
00000111 = 7, Reserved; do not use
00000110 = 6, Generic soft error trap
00000101 = 5, DMAC error trap
00000100 = 4, Math error trap
00000011 = 3, Stack error trap
00000010 = 2, Generic hard trap
00000001 = 1, Address error trap
00000000 = 0, Oscillator fail trap

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8.0 DIRECT MEMORY ACCESS (DMA)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Direct Memory Access (DMA)"** (www.microchip.com/DS70348) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM. For the simplified DMA block diagram, refer to Figure 8-1.

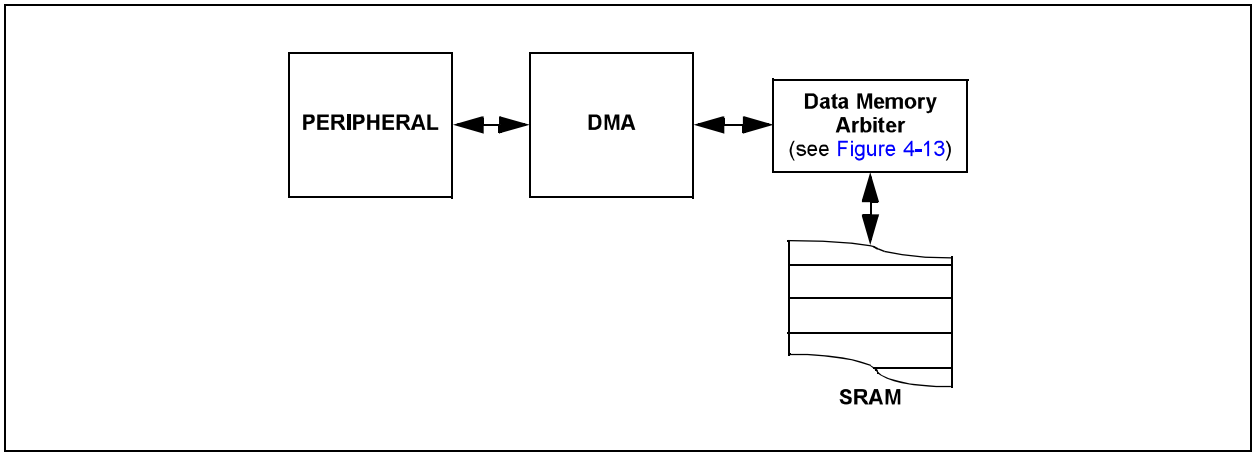
In addition, DMA can access the entire data memory space. The data memory bus arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU Stalls.

The DMA Controller supports four independent channels. Each channel can be configured for transfers to or from selected peripherals. The peripherals supported by the DMA Controller include:

- CAN
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

FIGURE 8-1: PERIPHERAL TO DMA CONTROLLER



In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel or channels are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA Channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer complete)
- DMA Request for Each Channel can be Selected from any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

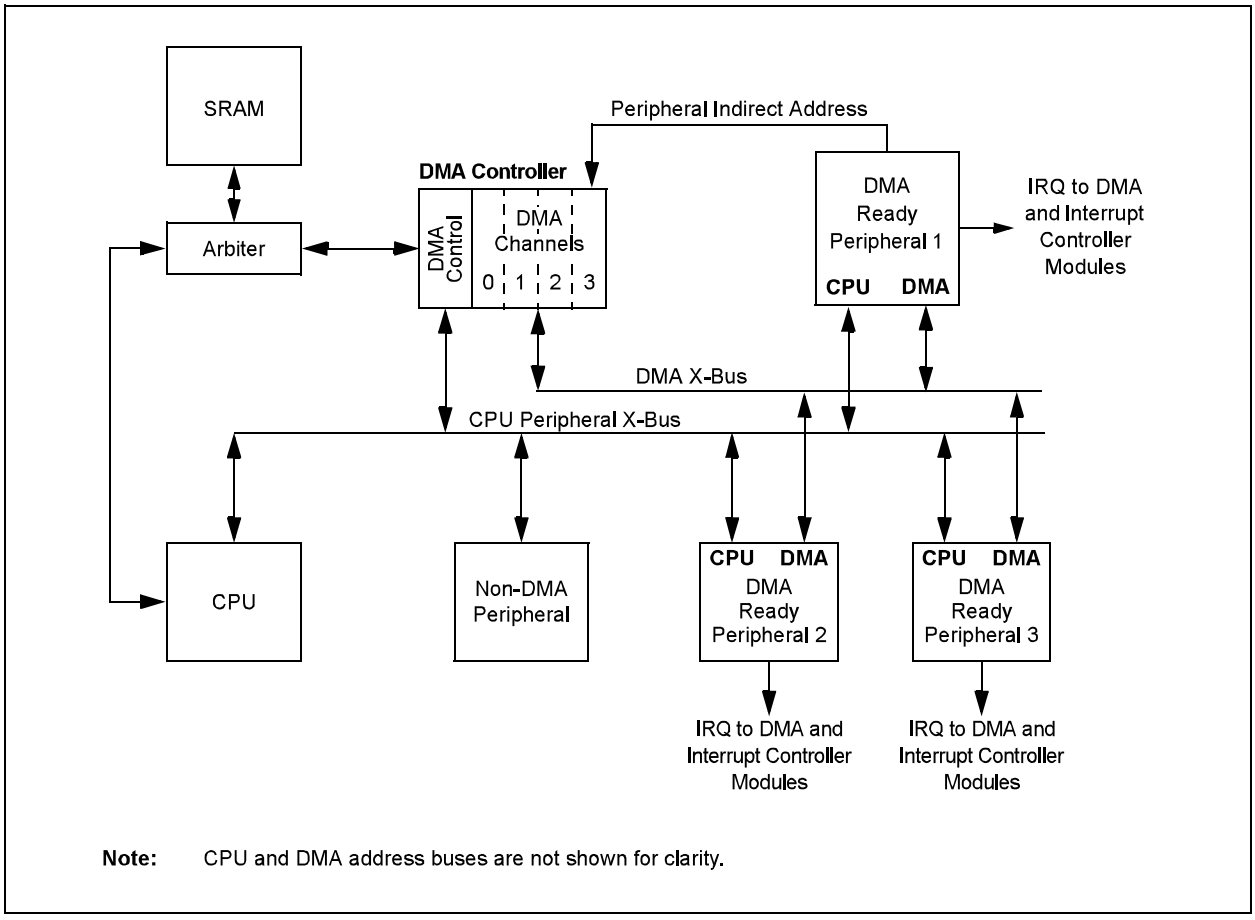
TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL[7:0] Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
External Interrupt 0 (INT0)	00000000	—	—
Input Capture 1 (IC1)	00000001	0x0144 (IC1BUF)	—
Input Capture 2 (IC2)	00000101	0x014C (IC2BUF)	—
Input Capture 3 (IC3)	00100101	0x0154 (IC3BUF)	—
Input Capture 4 (IC4)	00100110	0x015C (IC4BUF)	—
Output Compare 1 (OC1)	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
Output Compare 2 (OC2)	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
Output Compare 3 (OC3)	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
Output Compare 4 (OC4)	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
Timer2 (TMR2)	00000111	—	—
Timer3 (TMR3)	00001000	—	—
Timer4 (TMR4)	00011011	—	—
Timer5 (TMR5)	00011100	—	—
SPI1 Transfer Done	00001010	0x0248 (SPI1BUF)	0x0248 (SPI1BUF)
SPI2 Transfer Done	00100001	0x0268 (SPI2BUF)	0x0268 (SPI2BUF)
UART1 Receiver (UART1RX)	00001011	0x0226 (U1RXREG)	—
UART1 Transmitter (UART1TX)	00001100	—	0x0224 (U1TXREG)
UART2 Receiver (UART2RX)	00011110	0x0236 (U2RXREG)	—
UART2 Transmitter (UART2TX)	00011111	—	0x0234 (U2TXREG)
RX Data Ready (CAN1)	00100010	0x0440 (C1RXD)	—
TX Data Request (CAN1)	01000110	—	0x0442 (C1TXD)
ADC1 Convert Done (ADC1)	00001101	0x0300 (ADC1BUF0)	—

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Figure 8-2 illustrates the DMA Controller block diagram.

FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM



Note: CPU and DMA address buses are not shown for clarity.

8.1 DMAC Controller Registers

Each DMAC Channel x (where x = 0 to 3) contains the following registers:

- 16-Bit DMA Channel x Control Register (DMAxCON)
- 16-Bit DMA Channel x IRQ Select Register (DMAxREQ)
- 32-Bit DMA Channel x Start Address Register A High/Low (DMAxSTAH/L)
- 32-Bit DMA Channel x Start Address Register B High/Low (DMAxSTBH/L)
- 16-Bit DMA Channel x Peripheral Address Register (DMAxPAD)
- 14-Bit DMA Channel x Transfer Count Register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADRH/L) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The DMA Interrupt Flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding DMA Interrupt Enable bits (DMAxIE) are located in an IECx register in the interrupt controller and the corresponding DMA Interrupt Priority bits (DMAxIP) are located in an IPCx register in the interrupt controller.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CHEN:** DMA Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data have been moved
0 = Initiates interrupt when all of the data have been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **AMODE[1:0]:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **MODE[1:0]:** DMA Channel Operating Mode Select bits
11 = One-Shot Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous Ping-Pong modes are enabled
01 = One-Shot Ping-Pong modes are disabled
00 = Continuous Ping-Pong modes are disabled

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REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
FORCE(1)	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IRQSEL[7:0]							
bit 7							bit 0

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FORCE:** Force DMA Transfer bit(1)
1 = Forces a single DMA transfer (Manual mode)
0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL[7:0]:** DMA Peripheral IRQ Number Select bits
01000110 = TX data request (CAN1)(2)
00100110 = Input Capture 4 (IC4)
00100101 = Input Capture 3 (IC3)
00100010 = RX data ready (CAN1)
00100001 = SPI2 transfer done (SPI2)
00011111 = UART2 Transmitter (UART2TX)
00011110 = UART2 Receiver (UART2RX)
00011100 = Timer5 (TMR5)
00011011 = Timer4 (TMR4)
00011010 = Output Compare 4 (OC4)
00011001 = Output Compare 3 (OC3)
00001101 = ADC1 convert done (ADC1)
00001100 = UART1 Transmitter (UART1TX)
00001011 = UART1 Receiver (UART1RX)
00001010 = SPI1 transfer done (SPI1)
00001000 = Timer3 (TMR3)
00000111 = Timer2 (TMR2)
00000110 = Output Compare 2 (OC2)
00000101 = Input Capture 2 (IC2)
00000010 = Output Compare 1 (OC1)
00000001 = Input Capture 1 (IC1)
00000000 = External Interrupt 0 (INT0)

Note 1: The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

2: This select bit is only available on dsPIC33EVXXXGM10X devices.

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STA[23:16]:** DMA Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **STA[15:0]:** DMA Primary Start Address bits (source or destination)

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REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STB[23:16]:** DMA Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **STB[15:0]:** DMA Secondary Start Address bits (source or destination)

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PAD[15:0]:** DMA Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CNT[13:8](2)					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT[7:0](2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **CNT[13:0]:** DMA Transfer Count Register bits(2)

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT[13:0] + 1.

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REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **DSADR[23:16]:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR[15:8]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **DSADR[15:0]:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PWCOL3	PWCOL2	PWCOL1	PWCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **PWCOL3:** Channel 3 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

bit 2 **PWCOL2:** Channel 2 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

bit 1 **PWCOL1:** Channel 1 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

bit 0 **PWCOL0:** Channel 0 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = Write collision is not detected

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REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = User force and interrupt-based request collision is not detected

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = User force and interrupt-based request collision is not detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = User force and interrupt-based request collision is not detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = User force and interrupt-based request collision is not detected

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	LSTCH[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3-0 **LSTCH[3:0]:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

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REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
1 = DMA3STB register is selected
0 = DMA3STA register is selected

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit
1 = DMA2STB register is selected
0 = DMA2STA register is selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit
1 = DMA1STB register is selected
0 = DMA1STA register is selected

bit 0 **PPST0:** Channel 0 Ping-Pong mode Status Flag bit
1 = DMA0STB register is selected
0 = DMA0STA register is selected

NOTES:

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9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Oscillator"** (www.microchip.com/DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"*.

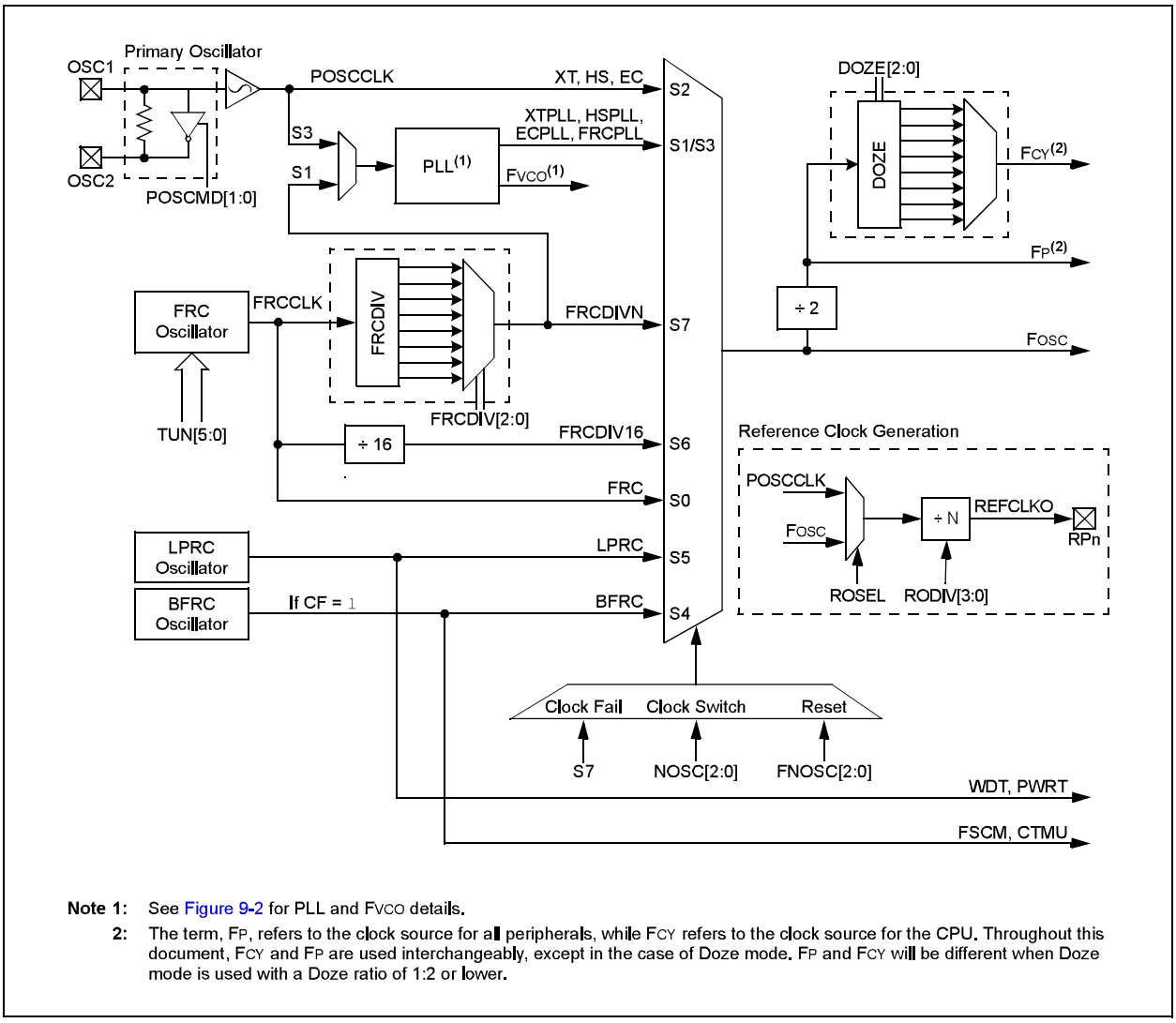
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family oscillator system provides:

- On-Chip Phase-Locked Loop (PLL) to Boost Internal Operating Frequency on Select Internal and External Oscillator Sources
- On-the-Fly Clock Switching between Various Clock Sources
- Doze mode for System Power Savings
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown.
- Backup FRC (BFRC) Function that Provides a System Clock when there is a Failure in the FRC Clock
- Configuration bits for Clock Source Selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL and FVCO details.

2: The term, FP, refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used with a Doze ratio of 1:2 or lower.

9.1 CPU Clocking System

The dsPIC33EVXXXGM00X/10X family of devices provides the following six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

For instruction execution speed or device operating frequency (FCY), see Equation 9-1.

EQUATION 9-1: DEVICE OPERATING FREQUENCY

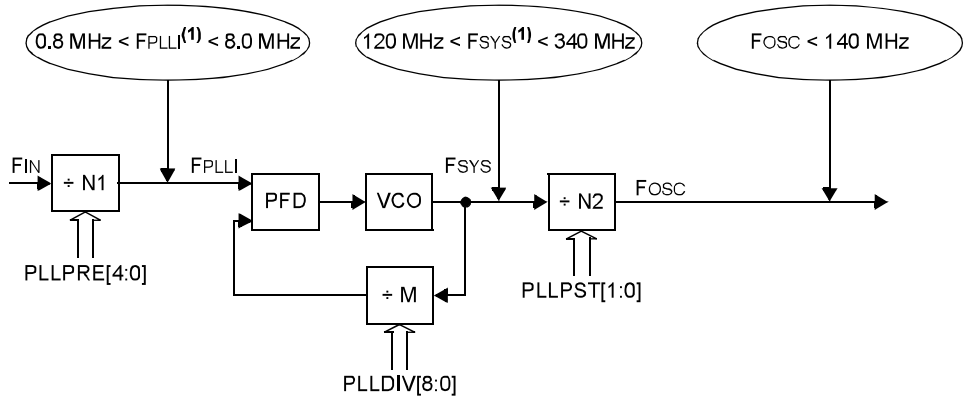
$$FCY = FOSC/2$$

Figure 9-2 provides the block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FOSC).

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FSYS).

FIGURE 9-2: PLL BLOCK DIAGRAM



Note 1: This frequency range must be met at all times.

EQUATION 9-2: Fosc CALCULATION

$$FOSC = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV[8:0] + 2)}{(PLLPRE[4:0] + 2) \times 2(PLLPOST[1:0] + 1)}\right)$$

Where:

$N1 = PLLPRE[4:0] + 2$

$N2 = 2 \times (PLLPOST[1:0] + 1)$

$M = PLLDIV[8:0] + 2$

EQUATION 9-3: Fvco CALCULATION

$$FSYS = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV[8:0] + 2)}{(PLLPRE[4:0] + 2)}\right)$$

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Table 9-1 provides the Configuration bits which allow users to choose between the various clock modes.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD[1:0]	FNOSC[2:0]
Fast RC Oscillator with Divide-by-N (FRCDIVN)(1,2)	Internal	xx	111
Fast RC Oscillator with Divide-by-16 (FRCDIV16)(1)	Internal	xx	110
Low-Power RC Oscillator (LPRC)(1)	Internal	xx	101
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011
Primary Oscillator (EC) with PLL (ECPLL)(1)	Primary	00	011
Primary Oscillator (HS)	Primary	10	010
Primary Oscillator (XT)	Primary	01	010
Primary Oscillator (EC)(1)	Primary	00	010
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)(1)	Internal	xx	001
Fast RC Oscillator (FRC)(1)	Internal	xx	000

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3)

U-0	R-0	R-0	R-0	U-0	R/W-y	R/W-y	R/W-y
—	COSC2	COSC1	COSC0	—	NOSC2(2)	NOSC1(2)	NOSC0(2)
bit 15							bit 8

R/W-0	R/W-0	R-0	U-0	R/C-0	U-0	U-0	R/W-0
CLKLOCK	IOLOCK	LOCK	—	CF	—	—	OSWEN
bit 7							bit 0

Legend:	C = Clearable bit	y = Value set from Configuration bits on POR	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC[2:0]:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-N
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Backup FRC Oscillator (BFRC)(4)
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) Divided by N and PLL
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC[2:0]:** New Oscillator Selection bits(2)
111 = Fast RC Oscillator (FRC) with Divide-by-N
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved(5)
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) Divided by N and PLL
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
1 = If FCKSM0 = 1, then clock and PLL configurations are locked; if FCKSM0 = 0, then clock and PLL configurations may be modified
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

Note 1: Writes to this register require an unlock sequence. Refer to **"Oscillator"** (www.microchip.com/DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"* (available from the Microchip website) for details.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This register resets only on a Power-on Reset (POR).

4: COSC[2:0] bits will be set to '0b100' when FRC fails.

5: User cannot write '0b100' to NOSC[2:0]. COSC[2:0] will be set to '0b100' (BFRC) when the FRC fails.

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REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1,3) (CONTINUED)

bit 4	**Unimplemented:** Read as '0'
bit 3	**CF:** Clock Fail Detect bit (read/clear by application) 1 = FSCM has detected a clock failure 0 = FSCM has not detected a clock failure
bit 2-1	**Unimplemented:** Read as '0'
bit 0	**OSWEN:** Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC[2:0] bits 0 = Oscillator switch is complete

Note 1: Writes to this register require an unlock sequence. Refer to **"Oscillator"** (www.microchip.com/DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"* (available from the Microchip website) for details.

2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

3: This register resets only on a Power-on Reset (POR).

4: COSC[2:0] bits will be set to '0b100' when FRC fails.

5: User cannot write '0b100' to NOSC[2:0]. COSC[2:0] will be set to '0b100' (BFRC) when the FRC fails.

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ROI	DOZE2(3)	DOZE1(3)	DOZE0(3)	DOZEN(1,4)	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE[2:0]:** Processor Clock Reduction Select bits(3)
111 = FCY divided by 128
110 = FCY divided by 64
101 = FCY divided by 32
100 = FCY divided by 16
011 = FCY divided by 8
010 = FCY divided by 4
001 = FCY divided by 2
000 = FCY divided by 1 (default)

bit 11 **DOZEN:** Doze Mode Enable bit(1,4)
1 = DOZE[2:0] field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio are forced to 1:1

bit 10-8 **FRCDIV[2:0]:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2 (default)
000 = FRC divided by 1

bit 7-6 **PLLPOST[1:0]:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4
00 = Output divided by 2

bit 5 **Unimplemented:** Read as '0'

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.
2: This register resets only on a Power-on Reset (POR).
3: DOZE[2:0] bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE[2:0] are ignored.
4: The DOZEN bit cannot be set if DOZE[2:0] = 000. If DOZE[2:0] = 000, any attempt by user software to set the DOZEN bit is ignored.

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REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2) (CONTINUED)

bit 4-0 **PLLPRE[4:0]:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: This register resets only on a Power-on Reset (POR).

3: DOZE[2:0] bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE[2:0] are ignored.

4: The DOZEN bit cannot be set if DOZE[2:0] = 000. If DOZE[2:0] = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV8
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV[8:0]:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2

Note 1: This register is reset only on a Power-on Reset (POR).

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REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN[5:0]:** FRC Oscillator Tuning bits

111111 = Center frequency – 0.048% (7.363 MHz)
•
•
•
100001 = Center frequency – 1.5% (7.259 MHz)
100000 = Center frequency – 1.548% (7.2552 MHz)
011111 = Center frequency + 1.5% (7.48 MHz)
011110 = Center frequency + 1.452% (7.477 MHz)
•
•
•
000001 = Center frequency + 0.048% (7.373 MHz)
000000 = Center frequency (7.37 MHz nominal)

Note 1: This register is reset only on a Power-on Reset (POR).

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3(1)	RODIV2(1)	RODIV1(1)	RODIV0(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on the REFCLK pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep mode
0 = Reference oscillator output is disabled in Sleep mode

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV[3:0]:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. See **Section 11.5 "Peripheral Pin Select (PPS)"** for more information.

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10.0 POWER-SAVING FEATURES

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (www.microchip.com/DS70615) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

The dsPIC33EVXXXGM00X/10X family devices can manage power consumption in the following four methods:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

10.1 Clock Frequency and Clock Switching

The dsPIC33EVXXXGM00X/10X family devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON[10:8]). For more information on the process of changing a system clock during operation, as well as limitations to the process, see **Section 9.0 "Oscillator Configuration"**.

10.2 Instruction-Based Power-Saving Modes

The dsPIC33EVXXXGM00X/10X family devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the `PWRSAV` instruction is shown in Example 10-1.

Note: `SLEEP_MODE` and `IDLE_MODE` are constants defined in the Assembler Include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

EXAMPLE 10-1: `PWRSAV` INSTRUCTION SYNTAX

```
PWRSAV  #SLEEP_MODE     ; Put the device into Sleep mode
PWRSAV  #IDLE_MODE      ; Put the device into Idle mode
```

10.2.1 SLEEP MODE

The following events occur in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared before entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into Standby mode when Sleep mode is entered by clearing the VREGS (RCON[8]) and VREGSF (RCON[11]) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON[8]) and VREGSF (RCON[11]) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following events occur in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (two to four clock cycles later), starting with the instruction following the `PWRSAV` instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON[13]).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up either from Sleep mode or Idle mode.

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10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this may not be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV[11]). The ratio between peripheral and core clock speed is determined by the DOZE[2:0] bits (CLKDIV[14:12]). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV[15]). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode, with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled, using the appropriate PMDx control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have any effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMDx register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMDx register by default.

Note:	If a PMDx bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMDx bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
T5MD	T4MD	T3MD	T2MD	T1MD	—	PWMMD	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	—	C1MD(1)	AD1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **Unimplemented:** Read as '0'

bit 9 **PWMMD:** PWM Module Disable bit
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

Note 1: This bit is available on dsPIC33EVXXXGM10X devices only.

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REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)

bit 2 **Unimplemented:** Read as '0'

bit 1 **C1MD:** CAN1 Module Disable bit(1)
1 = CAN1 module is disabled
0 = CAN1 module is enabled

bit 0 **AD1MD:** ADC1 Module Disable bit
1 = ADC1 module is disabled
0 = ADC1 module is enabled

Note 1: This bit is available on dsPIC33EVXXXGM10X devices only.

REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	IC4MD	IC3MD	IC2MD	IC1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	OC4MD	OC3MD	OC2MD	OC1MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **IC[4:1]MD:** Input Capture x (x = 1-4) Module Disable bits
1 = Input Capture x module is disabled
0 = Input Capture x module is enabled

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **OC[4:1]MD:** Output Compare x (x = 1-4) Module Disable bits
1 = Output Compare x module is disabled
0 = Output Compare x module is enabled

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	R/W-0	U-0	U-0
—	—	—	—	—	CMPMD	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9-0 **Unimplemented:** Read as '0'

REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	REFOMD	CTMUMD	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2 **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled

bit 1-0 **Unimplemented:** Read as '0'

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REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PWM[3:1]MD		
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **PWM[3:1]MD:** PWMx (x = 1-3) Module Disable bits
1 = PWMx module is disabled
0 = PWMx module is enabled

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	U-0
—	—	—	DMA0MD(1)	—	—	—	—
			DMA1MD(1)				
			DMA2MD(1)				
			DMA3MD(1)				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **DMA0MD:** DMA0 Module Disable bit(1)
1 = DMA0 module is disabled
0 = DMA0 module is enabled

DMA1MD: DMA1 Module Disable bit(1)
1 = DMA1 module is disabled
0 = DMA1 module is enabled

DMA2MD: DMA2 Module Disable bit(1)
1 = DMA2 module is disabled
0 = DMA2 module is enabled

DMA3MD: DMA3 Module Disable bit(1)
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: This single bit enables and disables all four DMA channels.

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REGISTER 10-7: PMD8: PERIPHERAL MODULE DISABLE CONTROL REGISTER 8

U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
—	—	—	SENT2MD	SENT1MD	—	—	DMTMD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **SENT2MD:** SENT2 Module Disable bit
1 = SENT2 module is disabled
0 = SENT2 module is enabled

bit 11 **SENT1MD:** SENT1 Module Disable bit
1 = SENT1 module is disabled
0 = SENT1 module is enabled

bit 10-9 **Unimplemented:** Read as '0'

bit 8 **DMTMD:** Deadman Timer Disable bit
1 = Deadman Timer is disabled
0 = Deadman Timer is enabled

bit 7-0 **Unimplemented:** Read as '0'

NOTES:

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11.0 I/O PORTS

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"I/O Ports"** (www.microchip.com/DS70000598) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the Parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity. All the pins in the device are 5V tolerant pins.

11.1 Parallel I/O (PIO) Ports

Generally, a Parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through", in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

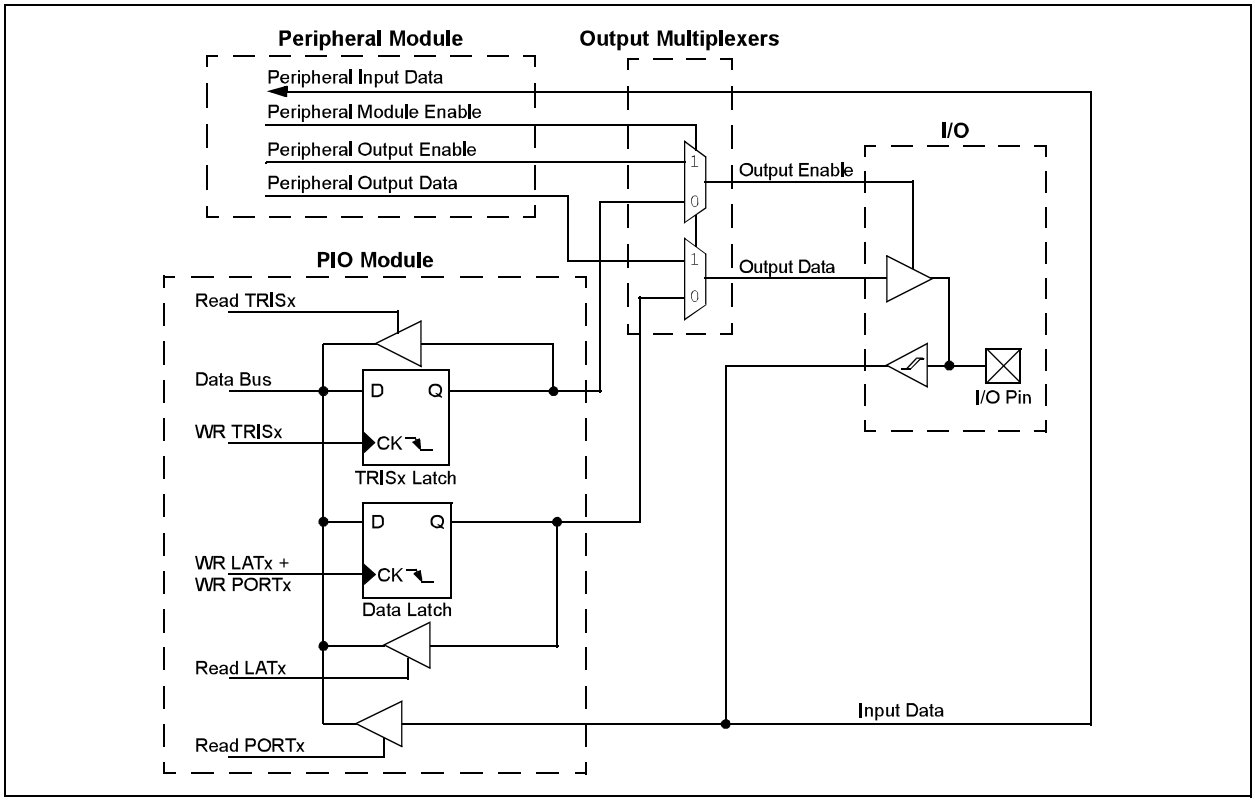
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the Data Direction register bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the latch (LATx), read the latch; writes to the latch, write the latch. Reads from the port (PORTx), read the port pins, while writes to the port pins, write the latch.

Any bit and its associated data and control registers that are not valid for a particular device are disabled. This means that the corresponding LATx and TRISx registers, and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port, because there is no other competing source of output.

FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE



11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain outputs. This is controlled by the Open-Drain Control x register (ODCx) associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See Table 30-10 in **Section 30.0 "Electrical Characteristics"** for the maximum VIH specification of each pin.

11.2 Configuring Analog and Digital Port Pins

The ANSELx registers control the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as timers, UARTs, etc., the corresponding ANSELx bits must be cleared.

The ANSELx register has a default value of 0xFFFF. Therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions table (see Table 1-1 in **Section 1.0 "Device Overview"**).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically, this instruction would be a NOP, as shown in Example 11-1.

11.3 Input Change Notification (ICN)

The Input Change Notification function (ICN) of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States, even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the ICN functionality of each I/O port. The CNENx registers contain the ICN interrupt enable control bits for each of the input pins. Setting any of these bits enables an ICN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin, and eliminate the need for external resistors when push button or keypad devices are connected. The pull-ups and pull-downs are enabled separately using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

Note:	The pull-ups and pull-downs on ICN pins should always be disabled when the port pin is configured as a digital output.

EXAMPLE 11-1: PORT WRITE/READ EXAMPLE

```
MOV   0xFF00, W0    ; Configure PORTB<15:8>
                    ; as inputs
MOV   W0, TRISB     ; and PORTB<7:0>
                    ; as outputs
NOP                 ; Delay 1 cycle
BTSS  PORTB, #13    ; Next Instruction
```


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11.4 Slew Rate Selection

The slew rate selection feature allows the device to have control over the slew rate selection on the required I/O pin which supports this feature. For this purpose, for each I/O port, there are two registers: SR1x and SR0x, which configure the selection of the slew rate. The register outputs are directly connected to the associated I/O pins, which support the slew rate selection function. The SR1x register specifies the MSb and the SR0x register provides the LSb of the 2-bit field that selects the desired slew rate. For example, slew rate selections for PORTA are as follows:

EXAMPLE 11-2: SLEW RATE SELECTIONS FOR PORTA

```
SR1Ax, SR0Ax = 00 = Fastest Slew rate
SR1Ax, SR0Ax = 01 = 4x slower Slew rate
SR1Ax, SR0Ax = 10 = 8x slower Slew rate
SR1Ax, SR0Ax = 11 = 16x slower Slew rate
```

11.5 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

The Peripheral Pin Select (PPS) configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The PPS configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping after it has been established.

11.5.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the PPS feature include the designation, “RPn” or “RPIn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

11.5.2 AVAILABLE PERIPHERALS

The peripherals managed by the PPS are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and Interrupt-on-Change (IOC) inputs.

In comparison, some digital only peripheral modules are never included in the PPS feature, because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between the remappable and non-remappable peripherals is that the remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, the non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all the other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.5.3 CONTROLLING PERIPHERAL PIN SELECT

The PPS features are controlled through two sets of SFRs: one to map the peripheral inputs and the other to map the outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

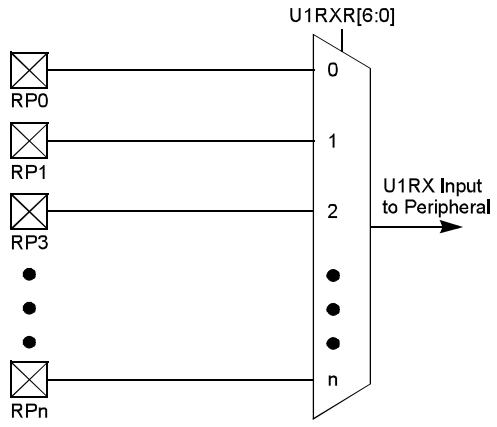
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

11.5.4 INPUT MAPPING

The inputs of the PPS options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Table 11-1 and Register 11-1 through Register 11-17). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral’s bit field with an appropriate 8-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selects supported by the device.

For example, Figure 11-2 shows the remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



Note: For input only, PPS functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

11.5.4.1 Virtual Connections

dsPIC33EVXXXGM00X/10X family devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 "Op Amp/Comparator Module"**).

These devices provide six virtual output pins (RPV0-RPV5) that correspond to the outputs of six peripheral pin output remapper blocks (RP176-RP181). The six virtual remapper outputs (RP176-RP181) are not connected to actual pins. The six virtual pins may be read by any of the input remappers as inputs, RPI176-RPI181. These virtual pins can be used to connect the internal peripherals, whose signals are of significant use to the other peripherals, but these output signals are not present on the device pin.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R[7:0] bits of the RPINR12 register to the value of 'b0000001', the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

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TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name(1)	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R[7:0]
External Interrupt 2	INT2	RPINR1	INT2R[7:0]
Timer2 External Clock	T2CK	RPINR3	T2CKR[7:0]
Input Capture 1	IC1	RPINR7	IC1R[7:0]
Input Capture 2	IC2	RPINR7	IC2R[7:0]
Input Capture 3	IC3	RPINR8	IC3R[7:0]
Input Capture 4	IC4	RPINR8	IC4R[7:0]
Output Compare Fault A	OCFA	RPINR11	OCFAR[7:0]
PWM Fault 1	FLT1	RPINR12	FLT1R[7:0]
PWM Fault 2	FLT2	RPINR12	FLT2R[7:0]
UART1 Receive	U1RX	RPINR18	U1RXR[7:0]
UART2 Receive	U2RX	RPINR19	U2RXR[7:0]
SPI2 Data Input	SDI2	RPINR22	SDI2R[7:0]
SPI2 Clock Input	SCK2	RPINR22	SCK2R[7:0]
SPI2 Slave Select	$\overline{SS2}$	RPINR23	SS2R[7:0]
CAN1 Receive	C1RX	RPINR26	C1RXR[7:0]
PWM Sync Input 1	SYNCI1	RPINR37	SYNCI1R[7:0]
PWM Dead-Time Compensation 1	DTCMP1	RPINR38	DTCMP1R[7:0]
PWM Dead-Time Compensation 2	DTCMP2	RPINR39	DTCMP2R[7:0]
PWM Dead-Time Compensation 3	DTCMP3	RPINR39	DTCMP3R[7:0]
SENT1 Input	SENT1R	RPINR44	SENT1R[7:0]
SENT2 Input	SENT2R	RPINR45	SENT2R[7:0]

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss
000 0001	I	CMP1(1)
000 0010	I	CMP2(1)
000 0011	I	CMP3(1)
000 0100	I	CMP4(1)
000 0101	—	—
000 1100	I	CMP5(1)
000 1101	—	—
000 1110	—	—
000 1111	—	—
001 0000	I	RPI16
001 0001	I	RPI17
001 0010	I	RPI18
001 0011	I	RPI19
001 0100	I/O	RP20
001 0101	—	—
001 0110	—	—
001 0111	—	—
001 1000	I	RPI24
001 1001	I	RPI25
001 1010	—	—
001 1011	I	RPI27
001 1100	I	RPI28
001 1101	—	—
001 1110	—	—
001 1111	—	—
010 0000	I	RPI32
010 0001	I	RPI33
010 0010	I	RPI34
010 0011	I/O	RP35
010 0100	I/O	RP36
010 0101	I/O	RP37
010 0110	I/O	RP38
010 0111	I/O	RP39
010 1000	I/O	RP40
010 1100	I	RPI44
010 1101	I	RPI45
010 1110	I	RPI46
010 1111	I	RPI47
011 0000	I/O	RP48
011 0010	I	RPI50
011 0011	I	RPI51
011 0100	I	RPI52
011 0101	I	RPI53
011 0110	I/O	RP54
011 0111	I/O	RP55
011 1000	I/O	RP56
011 1001	I/O	RP57
011 1010	I	RPI58
011 1011	—	—
011 1100	I	RPI60
011 1101	I	RPI61
011 1110	—	—
011 1111	I	RPI 63
100 0000	—	—
100 0001	—	—
100 0010	—	—
100 0011	—	—
100 0100	—	—
100 0101	I/O	RP69
100 0110	I/O	RP70
100 0111	—	—
100 1000	I	RPI72
100 1001	—	—
100 1010	—	—
100 1011	—	—
100 1110	—	—
100 1111	—	—
101 0010	—	—
101 0011	—	—
101 0100	—	—
010 1001	I/O	RP41
010 1010	I/O	RP42
010 1011	I/O	RP43
101 1000	—	—
101 1001	—	—
101 1010	—	—
101 1011	—	—
101 1100	—	—
101 1101	—	—

Legend: Shaded rows indicate the PPS Input register values that are unimplemented.

Note 1: These are virtual pins. See **Section 11.5.4.1 "Virtual Connections"** for more information on selecting this pin assignment.

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TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
011 0001	I/O	RP49
110 0000	I	RPI96
110 0001	I/O	RP97
110 0010	—	—
110 0011	—	—
110 0100	—	—
110 0101	—	—
110 0110	—	—
110 0111	—	—
110 1000	—	—
110 1001	—	—
110 1010	—	—
110 1011	—	—
101 0101	—	—
101 0110	—	—
101 0111	—	—
110 1100	—	—
110 1101	—	—
110 1110	—	—
110 1111	—	—
111 0010	—	—

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
101 1110	I	RPI94
101 1111	I	RPI95
111 0011	—	—
111 0100	—	—
111 0101	—	—
111 0110	I/O	RP118
111 0111	I	RPI119
111 1000	I/O	RP120
111 1001	I	RPI121
111 1010	—	—
111 1011	—	—
111 1100	I	RPI124
111 1101	I/O	RP125
111 1110	I/O	RP126
111 1111	I/O	RP127
10110000	I/O	RP176(1)
10110001	I/O	RP177(1)
10110010	I/O	RP178(1)
10110011	I/O	RP179(1)
10110100	I/O	RP180(1)
10110101	I/O	RP181(1)

Legend: Shaded rows indicate the PPS Input register values that are unimplemented.

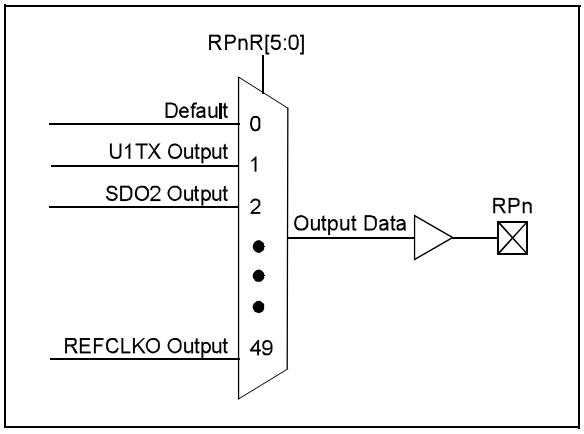
Note 1: These are virtual pins. See **Section 11.5.4.1 "Virtual Connections"** for more information on selecting this pin assignment.

11.5.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the PPS options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 to Register 11-31). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the Output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.5.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one, and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR[5:0]	Output Name
Default Port	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
C1TX	001110	RPn tied to CAN1 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
SYNCO1	101101	RPn tied to PWM Primary Time Base Sync Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4
C5OUT	110011	RPn tied to Comparator Output 5
SENT1	111001	RPn tied to SENT Out 1
SENT2	111010	RPn tied to SENT Out 2

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11.6 High-Voltage Detect (HVD)

dsPIC33EVXXXGM00X/10X devices contain High-Voltage Detection (HVD) which monitors the VCAP voltage. The HVD is used to monitor the VCAP supply voltage to ensure that an external connection does not raise the value above a safe level (~2.4V). If high core voltage is detected, all I/Os are disabled and put in a tri-state condition. The device remains in this I/O tri-state condition as long as the high-voltage condition is present.

11.7 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-10 under "Injection Current", have internal protection diodes to VDD and VSS. The term, "Injection Current", is also referred to as "Clamp Current". On designated pins with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low-side internal input clamp diodes, that the resulting current being injected into the device that is clamped internally by the VDD and VSS power rails may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a '0', regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a '0'.

Note:	Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name, from left-to-right. The left most function name takes precedence over any function to its right in the naming convention; for example, AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD – 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specifications. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

   VOH = 4.4V at IOH = -8 mA and VDD = 5V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current, <12 mA, is technically permitted. For more information, refer to the VOH/IOH specifications in **Section 30.0 "Electrical Characteristics"**.

6. The PPS pin mapping rules are as follows:
   - Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
   - It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
   - If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
   - If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
   - If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a Built-In Self-Test (BIST).
   - Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
   - The TRISx registers control only the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRISx setting. The TRISx register does not control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRISx settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned
   - All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin is disabled. Only the Analog Pin Select registers control the digital input buffer, not the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin; no exceptions.

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11.8 Peripheral Pin Select Registers

REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT1R[7:0]							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **INT1R[7:0]:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2R[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **INT2R[7:0]:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2CKR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **T2CKR[7:0]:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

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REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC2R7	IC2R6	IC2R5	IC2R4	IC2R3	IC2R2	IC2R1	IC2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC1R7	IC1R6	IC1R5	IC1R4	IC1R3	IC1R2	IC1R1	IC1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **IC2R[7:0]:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **IC1R[7:0]:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC4R7	IC4R6	IC4R5	IC4R4	IC4R3	IC4R2	IC4R1	IC4R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC3R7	IC3R6	IC3R5	IC3R4	IC3R3	IC3R2	IC3R1	IC3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **IC4R[7:0]:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **IC3R[7:0]:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

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REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OCFAR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **OCFAR[7:0]:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT2R7	FLT2R6	FLT2R5	FLT2R4	FLT2R3	FLT2R2	FLT2R1	FLT2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT1R7	FLT1R6	FLT1R5	FLT1R4	FLT1R3	FLT1R2	FLT1R1	FLT1R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **FLT2R[7:0]:** Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **FLT1R[7:0]:** Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

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REGISTER 11-8: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1RXR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **U1RXR[7:0]:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-9: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U2RXR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **U2RXR[7:0]:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-10: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCK2R7	SCK2R6	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDI2R	SDI2R6	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SCK2R[7:0]:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **SDI2R[7:0]:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

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REGISTER 11-11: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SS2R[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **SS2R[7:0]:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-12: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C1RXR[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **C1RXR[7:0]:** Assign CAN1 RX Input (C1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-13: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCI1R[7:0]							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SYNCI1R[7:0]:** Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-14: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTCMP1R[7:0]							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **DTCMP1R[7:0]:** Assign PWM Dead-Time Compensation Input 1 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 11-15: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTCMP3R7	DTCMP3R6	DTCMP3R5	DTCMP3R4	DTCMP3R3	DTCMP3R2	DTCMP3R1	DTCMP3R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTCMP2R7	DTCMP2R6	DTCMP2R5	DTCMP2R4	DTCMP2R3	DTCMP2R2	DTCMP2R1	DTCMP2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **DTCMP3R[7:0]:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **DTCMP2R[7:0]:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

REGISTER 11-16: RPINR44: PERIPHERAL PIN SELECT INPUT REGISTER 44

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT1R[7:0]							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **SENT1R[7:0]:** Assign SENT Module Input 1 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-17: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SENT2R[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **SENT2R[7:0]:** Assign SENT Module Input 2 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
10110101 = Input tied to RPI181
•
•
•
00000001 = Input tied to CMP1
00000000= Input tied to Vss

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REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R5	RP20R4	RP20R3	RP20R2	RP20R1	RP20R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP35R[5:0]:** Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP20R[5:0]:** Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP37R[5:0]:** Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP36R[5:0]:** Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP39R[5:0]:** Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP38R[5:0]:** Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R[5:0]:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R[5:0]:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for peripheral function numbers)

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REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP42R5	RP42R4	RP42R3	RP42R2	RP42R1	RP42R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP43R[5:0]:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP42R[5:0]:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP49R5	RP49R4	RP49R3	RP49R2	RP49R1	RP49R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP48R5	RP48R4	RP48R3	RP48R2	RP48R1	RP48R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP49R[5:0]:** Peripheral Output Function is Assigned to RP49 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP48R[5:0]:** Peripheral Output Function is Assigned to RP48 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP55R[5:0]:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP54R[5:0]:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only

REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP57R[5:0]:** Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP56R[5:0]:** Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

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REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP70R5	RP70R4	RP70R3	RP70R2	RP70R1	RP70R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP69R5	RP69R4	RP69R3	RP69R2	RP69R1	RP69R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP70R[5:0]:** Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP69R[5:0]:** Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/104/006/106 devices only.

REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R5	RP118R4	RP118R3	RP118R2	RP118R1	RP118R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP97R5	RP97R4	RP97R3	RP97R2	RP97R1	RP97R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP118R[5:0]:** Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP97R[5:0]:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is present in dsPIC33EVXXXGM004/106 devices only.

REGISTER 11-28: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R5(1)	RP120R4(1)	RP120R3(1)	RP120R2(1)	RP120R1(1)	RP120R0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP176R[5:0]:** Peripheral Output Function is Assigned to RP176 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R[5:0]:** Peripheral Output Function is Assigned to RP120 Output Pin bits(1) (see Table 11-3 for peripheral function numbers)

Note 1: RP120R[5:0] bits are present in dsPIC33EVXXXGM006/106 devices only.

REGISTER 11-29: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP178R[5:0]:** Peripheral Output Function is Assigned to RP178 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP177R[5:0]:** Peripheral Output Function is Assigned to RP177 Output Pin bits (see Table 11-3 for peripheral function numbers)

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REGISTER 11-30: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP180R[5:0]:** Peripheral Output Function is Assigned to RP180 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP179R[5:0]:** Peripheral Output Function is Assigned to RP179 Output Pin bits (see Table 11-3 for peripheral function numbers)

REGISTER 11-31: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP181R[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **RP181R[5:0]:** Peripheral Output Function is Assigned to RP181 Output Pin bits (see Table 11-3 for peripheral function numbers)

NOTES:

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12.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (www.microchip.com/DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running, interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode from an External Clock Source
- The Timer1 External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

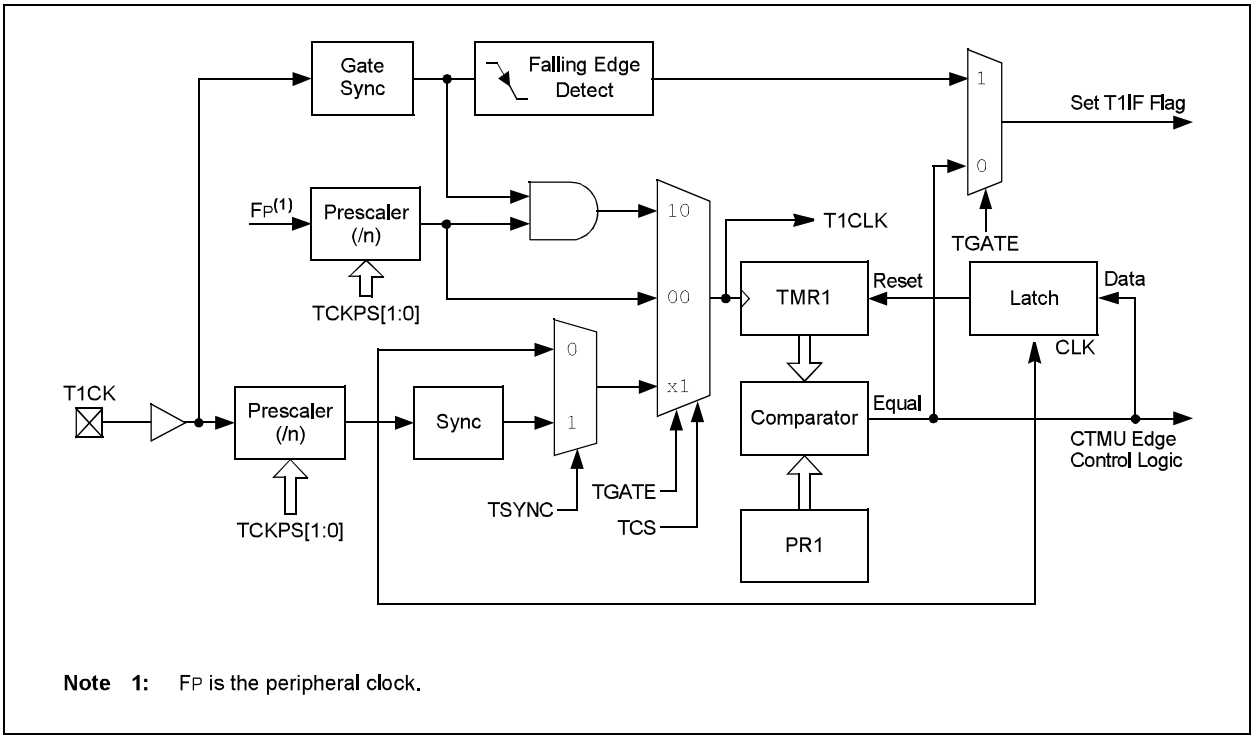
- Timer Clock Source Control bit (TCS): T1CON[1]
- Timer Synchronization Control bit (TSYNC): T1CON[2]
- Timer Gate Control bit (TGATE): T1CON[6]

Timer control bit settings for different operating modes are given in Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



Note 1: FP is the peripheral clock.

12.1 Timer1 Control Register

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC(1)	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit(1)
When TCS = 1:
1 = External clock input is synchronized
0 = External clock input is not synchronized
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock is from pin, T1CK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

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13.0 TIMER2/3 AND TIMER4/5

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (www.microchip.com/DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

These modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As a 32-bit timer, Timer2/3 and Timer4/5 operate in the following three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules
- ADC1 Event Trigger (Timer2/3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. The T3CON and T5CON registers are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw). Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

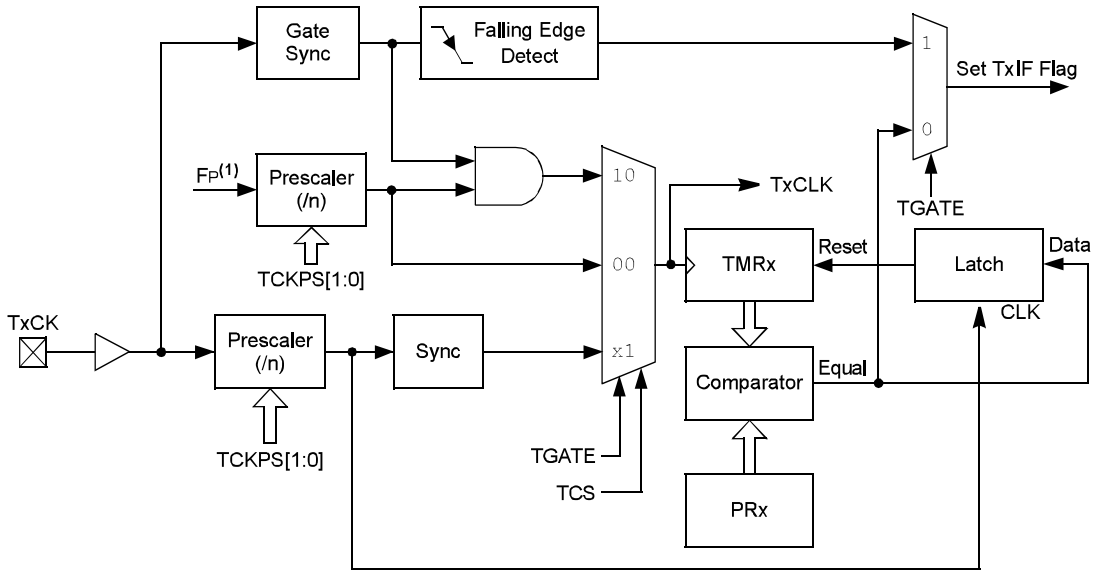
Note: For 32-bit operation, the T3CON and T5CON control bits are ignored. Only the T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

Block diagrams for the Type B and Type C timers are shown in Figure 13-1 and Figure 13-2, respectively.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

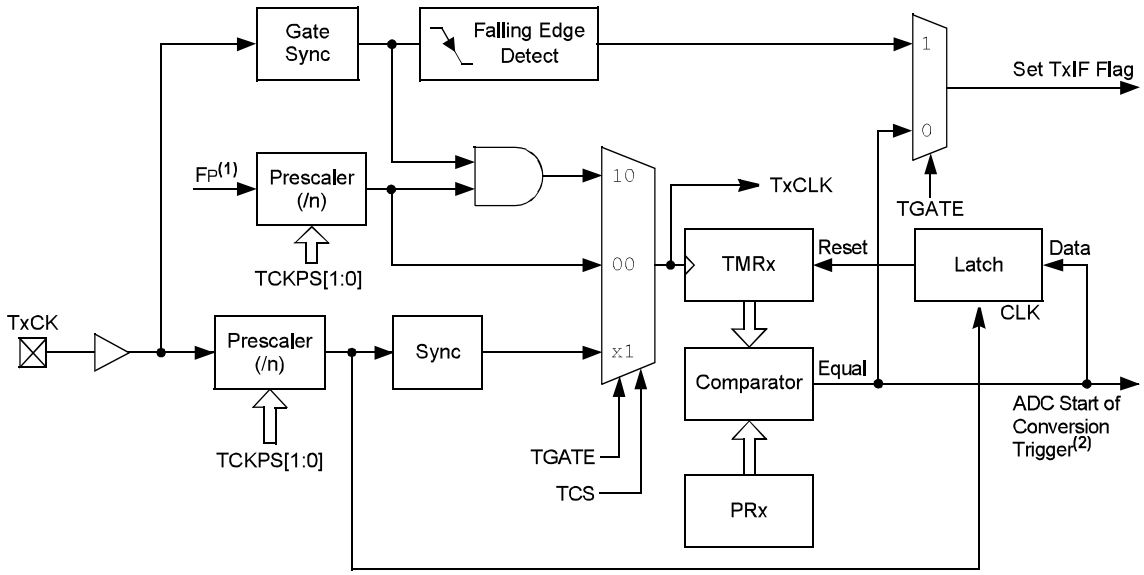
Note: Only Timer2, Timer3, Timer4 and Timer5 can trigger a DMA data transfer.

FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)



Note 1: FP is the peripheral clock.

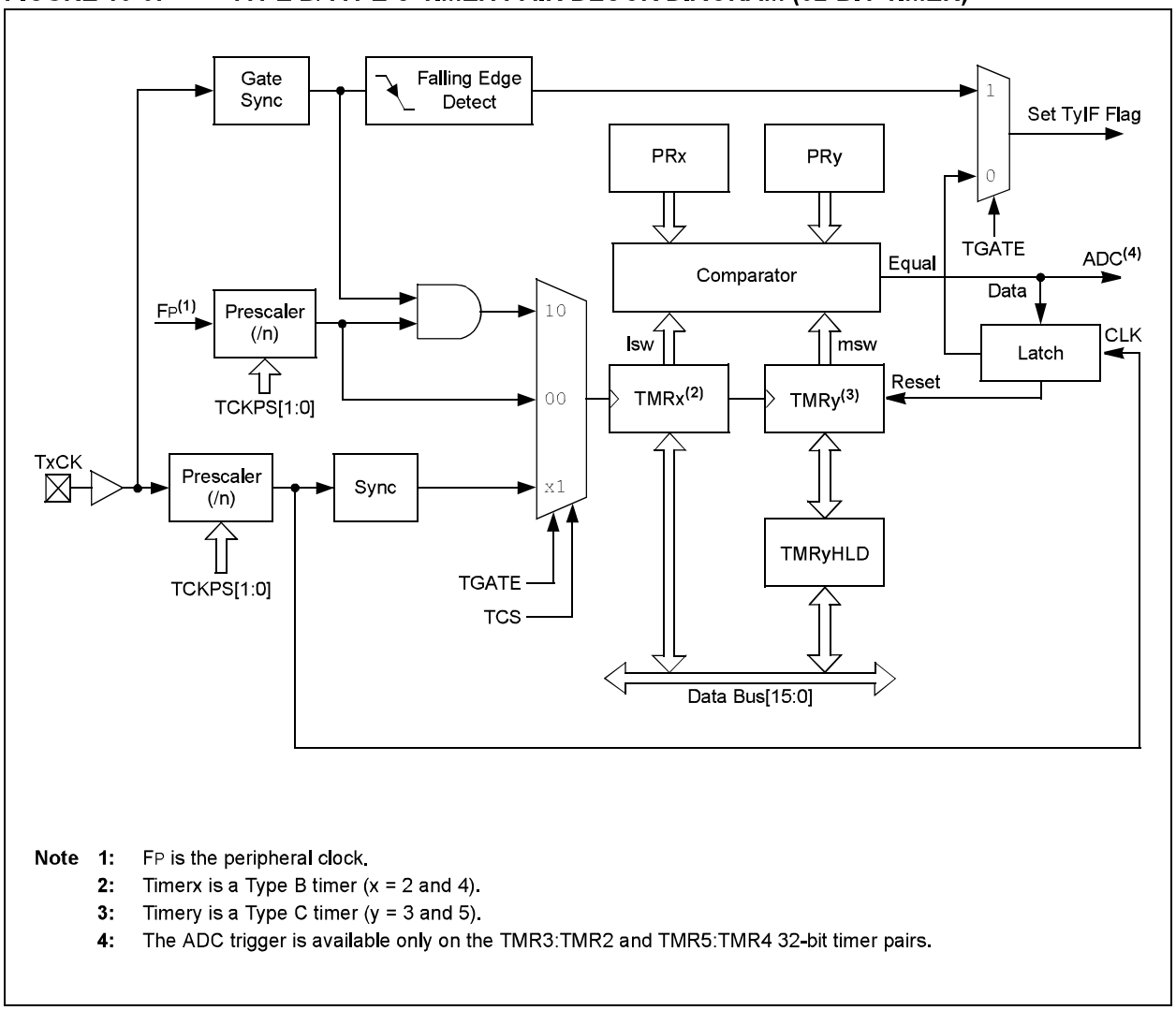
FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)



Note 1: FP is the peripheral clock.
2: The ADC trigger is available on TMR3 and TMR5 only.

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FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)



Note 1: FP is the peripheral clock.
2: Timerx is a Type B timer (x = 2 and 4).
3: Timery is a Type C timer (y = 3 and 5).
4: The ADC trigger is available only on the TMR3:TMR2 and TMR5:TMR4 32-bit timer pairs.

13.1 Timer2/3 and Timer4/5 Control Registers

REGISTER 13-1: TxCON (T2CON AND T4CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32	—	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timerx On bit
When T32 = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When T32 = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(1)
1 = External clock is from pin, TxCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: The TxCK pin is not available on all timers. Refer to the **"Pin Diagrams"** section for the available pins.

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REGISTER 13-2: TyCON (T3CON AND T5CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL(2)	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(1)	TCKPS1(1)	TCKPS0(1)	—	—	TCS(1,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when the device enters an Idle mode
0 = Continues module operation in an Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock is from pin, TyCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When 32-bit operation is enabled (T2CON[3] = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

2: When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON[3]), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

3: The TyCK pin is not available on all timers. See the **"Pin Diagrams"** section for the available pins.

NOTES:

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14.0 DEADMAN TIMER (DMT)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Deadman Timer (DMT)"** (www.microchip.com/DS70005155) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

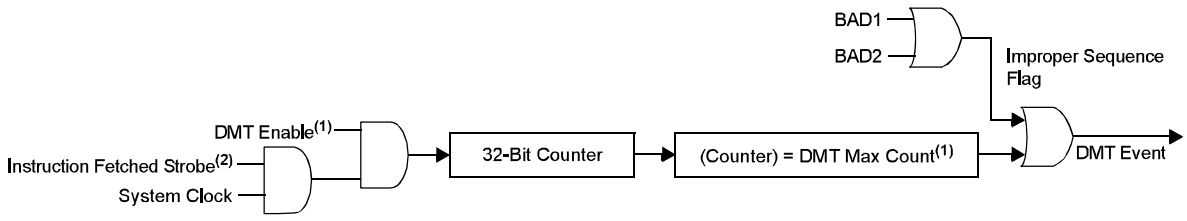
The primary function of the Deadman Timer (DMT) is to reset the processor in the event of a software malfunction. The DMT, which works on the system clock, is a free-running instruction fetch timer, which is clocked whenever an instruction fetch occurs, until a count match occurs. Instructions are not fetched when the processor is in Sleep mode.

DMT can be enabled in the Configuration fuse or by software in the DMTCON register by setting the ON bit. The DMT consists of a 32-bit counter with a time-out count match value, as specified by the two 16-bit Configuration Fuse registers: FDMTCNTL and FDMTCNTH.

A DMT is typically used in mission-critical, and safety-critical applications, where any single failure of the software functionality and sequencing must be detected.

Figure 14-1 shows a block diagram of the Deadman Timer module.

FIGURE 14-1: DEADMAN TIMER BLOCK DIAGRAM



Note 1: DMT Max Count is controlled by the initial value of the FDMTCNTL and FDMTCNTH Configuration registers.

2: DMT window interval is controlled by the value of the FDMTINTVL and FDMTINTVH Configuration registers.

14.1 Deadman Timer Control Registers

REGISTER 14-1: DMTCON: DEADMAN TIMER CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
ON(1)	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ON:** DMT Module Enable bit(1)
1 = Deadman Timer module is enabled
0 = Deadman Timer module is not enabled

bit 14-0 **Unimplemented:** Read as '0'

Note 1: This bit has control only when DMTEN = 0 in the FDMT register.

REGISTER 14-2: DMTPRECLR: DEADMAN TIMER PRECLEAR REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP1[7:0]							
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP1[7:0]:** DMT Preclear Enable bits
01000000 = Enables the Deadman Timer preclear (Step 1)
All Other
Write Patterns = Sets the BAD1 flag; these bits are cleared when a DMT Reset event occurs. STEP1[7:0] bits are also cleared if the STEP2[7:0] bits are loaded with the correct value in the correct sequence.

bit 7-0 **Unimplemented:** Read as '0'

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REGISTER 14-3: DMTCLR: DEADMAN TIMER CLEAR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP2[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STEP2[7:0]:** DMT Clear Timer bits

00001000 = Clears STEP1[7:0], STEP2[7:0] and the Deadman Timer if preceded by the correct loading of the STEP1[7:0] bits in the correct sequence. The write to these bits may be verified by reading the DMTCNTL/H register and observing the counter being reset.

All Other Write Patterns = Sets the BAD2 bit; the value of STEP1[7:0] will remain unchanged and the new value being written to STEP2[7:0] will be captured. These bits are cleared when a DMT Reset event occurs.

REGISTER 14-4: DMTSTAT: DEADMAN TIMER STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

HC/R-0	HC/R-0	HC/R-0	U-0	U-0	U-0	U-0	R-0
BAD1	BAD2	DMTEVENT	—	—	—	—	WINOPN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **BAD1:** Deadman Timer Bad STEP1[7:0] Value Detect bit
1 = Incorrect STEP1[7:0] value was detected
0 = Incorrect STEP1[7:0] value was not detected

bit 6 **BAD2:** Deadman Timer Bad STEP2[7:0] Value Detect bit
1 = Incorrect STEP2[7:0] value was detected
0 = Incorrect STEP2[7:0] value was not detected

bit 5 **DMTEVENT:** Deadman Timer Event bit
1 = Deadman Timer event was detected (counter expired, or bad STEP1[7:0] or STEP2[7:0] value was entered prior to counter increment)
0 = Deadman Timer event was not detected

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **WINOPN:** Deadman Timer Clear Window bit
1 = Deadman Timer clear window is open
0 = Deadman Timer clear window is not open

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REGISTER 14-5: DMTCNTL: DEADMAN TIMER COUNT REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COUNTER[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COUNTER[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **COUNTER[15:0]:** Read Current Contents of Lower DMT Counter bits

REGISTER 14-6: DMTCNTH: DEADMAN TIMER COUNT REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COUNTER[31:24]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
COUNTER[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **COUNTER[31:16]:** Read Current Contents of Higher DMT Counter bits

REGISTER 14-7: DMTPSCNTL: DMT POST-CONFIGURE COUNT STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT[15:0]:** Lower DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTL Configuration register.

REGISTER 14-8: DMTPSCNTH: DMT POST-CONFIGURE COUNT STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT[31:24]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSCNT[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSCNT[31:16]:** Higher DMT Instruction Count Value Configuration Status bits
This is always the value of the FDMTCNTH Configuration register.

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REGISTER 14-9: DMTPSINTVL: DMT POST-CONFIGURE INTERVAL STATUS REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSINTV[15:0]:** Lower DMT Window Interval Configuration Status bits
This is always the value of the FDMTINTVL Configuration register.

REGISTER 14-10: DMTPSINTVH: DMT POST-CONFIGURE INTERVAL STATUS REGISTER HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV[31:24]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSINTV[23:16]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PSINTV[31:16]:** Higher DMT Window Interval Configuration Status bits
This is always the value of the FDMTINTVH Configuration register.

REGISTER 14-11: DMTHOLDREG: DMT HOLD REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
UPRCNT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **UPRCNT[15:0]:** Value of the DMTCNTH Register when DMTCNTL and DMTCNTH were Last Read bits

Note 1: The DMTHOLDREG register is initialized to '0' on Reset, and is only loaded when the DMTCNTL and DMTCNTH registers are read.

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15.0 INPUT CAPTURE

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture with Dedicated Timer"** (www.microchip.com/DS70000352) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

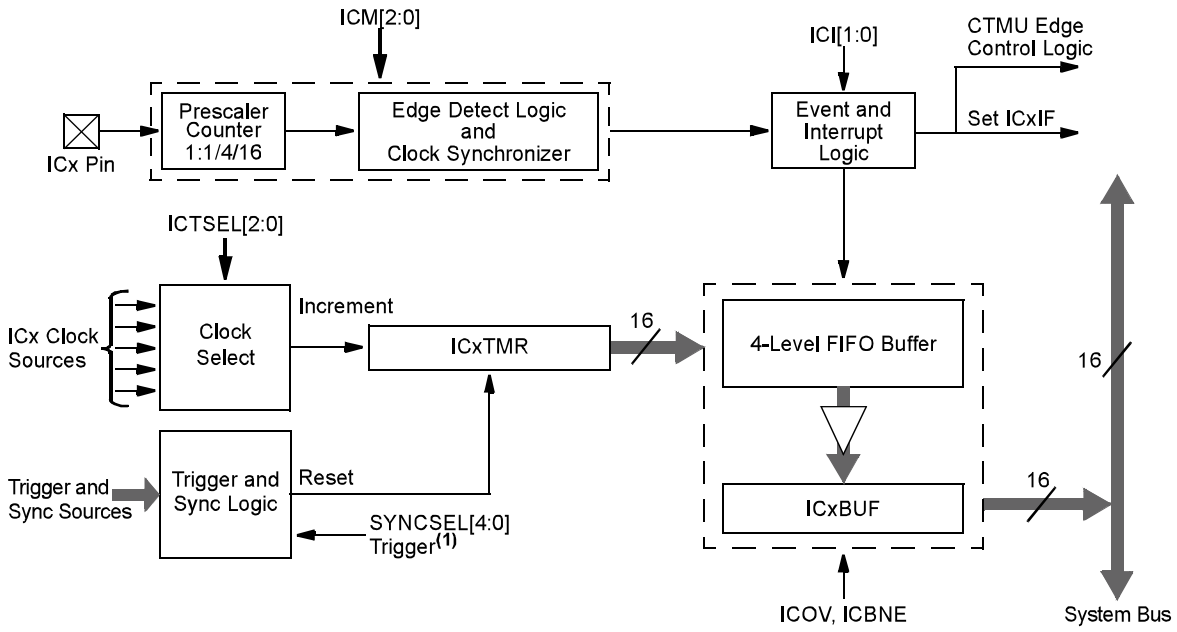
The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EVXXXGM00X/10X family devices support four input capture channels.

Key features of the input capture module include:

- Hardware-Configurable for 32-Bit Operation in All Modes by Cascading Two Adjacent modules
- Synchronous and Trigger Modes of Output Compare Operation, with up to 31 User-Selectable Trigger/Sync Sources Available
- A Four-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
- Configurable Interrupt Generation
- Up to Six Clock Sources Available for Each Module, Driving a Separate Internal 16-Bit Counter

Figure 15-1 shows a block diagram of the Input capture module.

FIGURE 15-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM



Note 1: The trigger/sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the trigger/sync source must be changed to another source option.

15.1 Input Capture Control Registers

REGISTER 15-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	HC/HS/R-0	HC/HS/R-0	R/W-0	R/W-0	R/W-0
—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture x Stop in Idle Mode Control bit
1 = Input Capture x will halt in CPU Idle mode
0 = Input Capture x will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL[2:0]:** Input Capture x Timer Select bits
111 = Peripheral clock (FP) is the clock source of the ICx
110 = Reserved
101 = Reserved
100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
011 = T5CLK is the clock source of the ICx
010 = T4CLK is the clock source of the ICx
001 = T2CLK is the clock source of the ICx
000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI[1:0]:** Number of Captures per Interrupt Select bits (this field is not used if ICM[2:0] = 001 or 111)
11 = Interrupt on every fourth capture event
10 = Interrupt on every third capture event
01 = Interrupt on every second capture event
00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture x Overflow Status Flag bit (read-only)
1 = Input Capture x buffer overflow has occurred
0 = Input Capture x buffer overflow has not occurred

bit 3 **ICBNE:** Input Capture x Buffer Not Empty Status bit (read-only)
1 = Input Capture x buffer is not empty, at least one more capture value can be read
0 = Input Capture x buffer is empty

bit 2-0 **ICM[2:0]:** Input Capture x Mode Select bits
111 = Input Capture x functions as an interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
110 = Unused (module is disabled)
101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
011 = Capture mode, every rising edge (Simple Capture mode)
010 = Capture mode, every falling edge (Simple Capture mode)
001 = Capture mode, every edge, rising and falling (Edge Detect mode (ICI[1:0]) is not used in this mode)
000 = Input Capture x module is turned off

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REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32(1)
bit 15							bit 8

R/W-0	HS/R/W-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG(2)	TRIGSTAT(3)	—	SYNCSEL4(4)	SYNCSEL3(4)	SYNCSEL2(4)	SYNCSEL1(4)	SYNCSEL0(4)
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC32:** Input Capture x 32-Bit Timer Mode Select bit (Cascade mode)(1)
- 1 = Odd ICx and even ICx form a single 32-bit input capture module
- 0 = Cascade module operation is disabled

bit 7 **ICTRIG:** Input Capture x Trigger Operation Select bit(2)
- 1 = Input source is used to trigger the input capture timer (Trigger mode)
- 0 = Input source is used to synchronize the input capture timer to the timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit(3)
- 1 = ICxTMR has been triggered and is running
- 0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL[4:0] bits of the ICxCON2 register.

3: This bit is set by the selected input source (selected by the SYNCSEL[4:0] bits); it can be read, set and cleared in software.

4: Do not use the ICx module as its own sync or trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

REGISTER 15-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL[4:0]:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = Reserved
11110 = Reserved
11101 = Reserved
11100 = CTMU trigger is the source for the capture timer synchronization
11011 = ADC1 interrupt is the source for the capture timer synchronization(5)
11010 = Analog Comparator 3 is the source for the capture timer synchronization(5)
11001 = Analog Comparator 2 is the source for the capture timer synchronization(5)
11000 = Analog Comparator 1 is the source for the capture timer synchronization(5)
10111 = Analog Comparator 5 is the source for the capture timer synchronization(5)
10110 = Analog Comparator 4 is the source for the capture timer synchronization(5)
10101 = Reserved
10100 = Reserved
10011 = Input Capture 4 interrupt is the source for the capture timer synchronization
10010 = Input Capture 3 interrupt is the source for the capture timer synchronization
10001 = Input Capture 2 interrupt is the source for the capture timer synchronization
10000 = Input Capture 1 interrupt is the source for the capture timer synchronization
01111 = GP Timer5 is the source for the capture timer synchronization
01110 = GP Timer4 is the source for the capture timer synchronization
01101 = GP Timer3 is the source for the capture timer synchronization
01100 = GP Timer2 is the source for the capture timer synchronization
01011 = GP Timer1 is the source for the capture timer synchronization
01010 = Reserved
01001 = Reserved
01000 = Input Capture 4 is the source for the capture timer synchronization(6)
00111 = Input Capture 3 is the source for the capture timer synchronization(6)
00110 = Input Capture 2 is the source for the capture timer synchronization(6)
00101 = Input Capture 1 is the source for the capture timer synchronization(6)
00100 = Output Compare 4 is the source for the capture timer synchronization
00011 = Output Compare 3 is the source for the capture timer synchronization
00010 = Output Compare 2 is the source for the capture timer synchronization
00001 = Output Compare 1 is the source for the capture timer synchronization
00000 = Reserved

Note 1: The IC32 bit in both the odd and even ICx must be set to enable Cascade mode.
2: The input source is selected by the SYNCSEL[4:0] bits of the ICxCON2 register.
3: This bit is set by the selected input source (selected by the SYNCSEL[4:0] bits); it can be read, set and cleared in software.
4: Do not use the ICx module as its own sync or trigger source.
5: This option should only be selected as a trigger source and not as a synchronization source.
6: When the source ICx timer rolls over, then in the next clock cycle, trigger or synchronization occurs.

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16.0 OUTPUT COMPARE

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Output Compare with Dedicated Timer"** (www.microchip.com/DS70005159) in the *"dsPIC33/PIC24 Family Reference Manual"*.

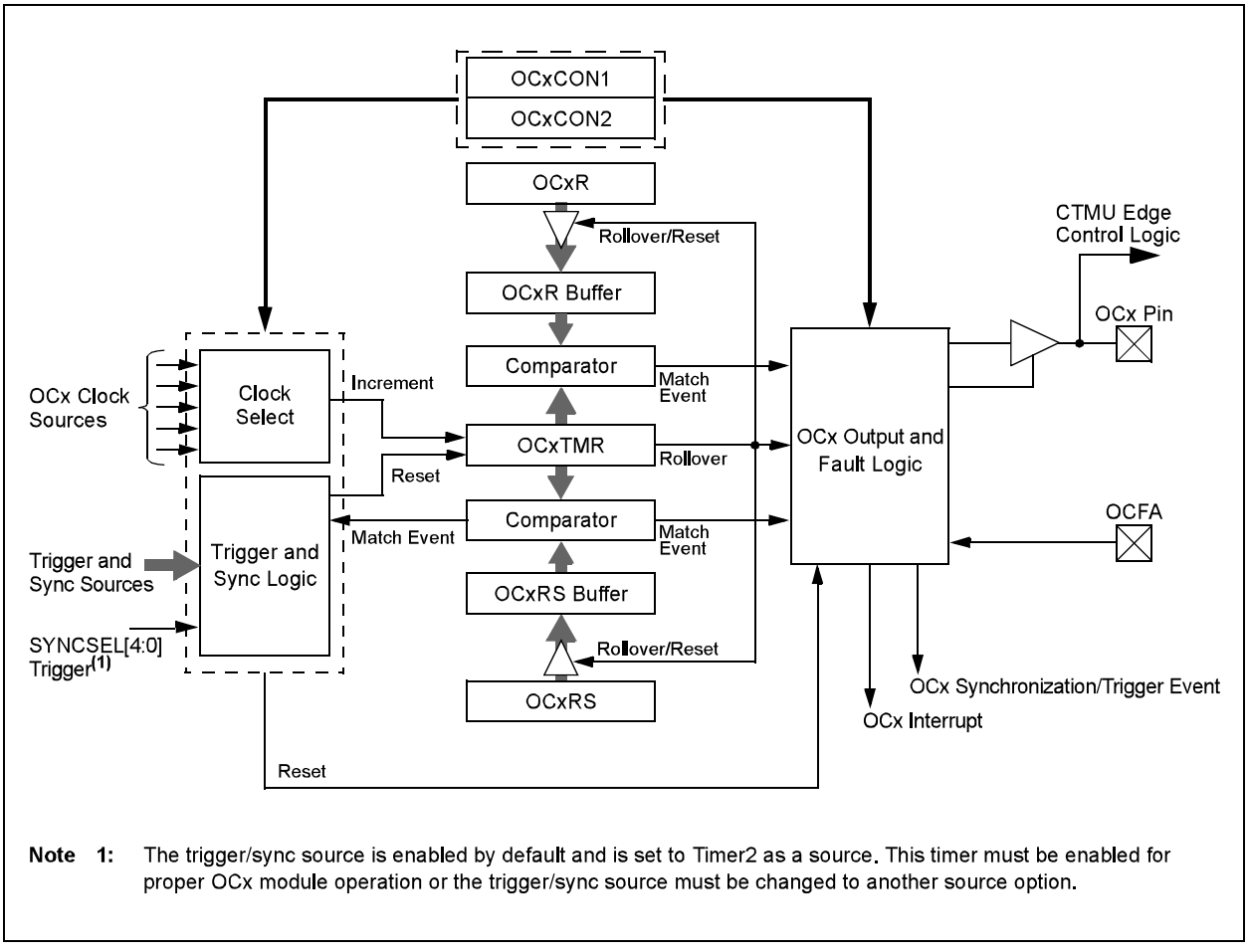
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family devices support up to four output compare modules. The output compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers, depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Figure 16-1 shows a block diagram of the output compare module.

Note: For more information on OCxR and OCxRS register restrictions, refer to **"Output Compare with Dedicated Timer"** (www.microchip.com/DS70005159) in the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 16-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM



Note 1: The trigger/sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for proper OCx module operation or the trigger/sync source must be changed to another source option.

16.1 Output Compare Control Registers

REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—
bit 15							bit 8

R/W-0	U-0	U-0	HSC/R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Output Compare x Stop in Idle Mode Control bit
- 1 = Output Compare x halts in CPU Idle mode
- 0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL[2:0]:** Output Compare x Clock Select bits
- 111 = Peripheral clock (FP)
- 110 = Reserved
- 101 = Reserved
- 100 = T1CLK is the clock source of the OCx (only the synchronous clock is supported)
- 011 = T5CLK is the clock source of the OCx
- 010 = T4CLK is the clock source of the OCx
- 001 = T3CLK is the clock source of the OCx
- 000 = T2CLK is the clock source of the OCx

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **ENFLTA:** Output Compare x Fault A Input Enable bit
- 1 = Output Compare Fault A (OCFA) input is enabled
- 0 = Output Compare Fault A (OCFA) input is disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **OCFLTA:** PWM Fault A Condition Status bit
- 1 = PWM Fault A condition on the OCFA pin has occurred
- 0 = PWM Fault A condition on the OCFA pin has not occurred

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
- 1 = TRIGSTAT (OCxCON2[6]) is cleared when OCxRS = OCxTMR or in software
- 0 = TRIGSTAT is cleared only by software

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

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REGISTER 16-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

bit 2-0 **OCM[2:0]:** Output Compare x Mode Select bits

111 = Center-Aligned PWM mode: Output sets high when OCxTMR = OCxR and sets low when OCxTMR = OCxRS(1)

110 = Edge-Aligned PWM mode: Output sets high when OCxTMR = 0 and sets low when OCxTMR = OCxR(1)

101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS

100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle

011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin

010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low

001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high

000 = Output compare channel is disabled

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	HS/R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit
- 1 = Fault mode is maintained until the Fault source is removed; the OCFLTA bit is cleared in software and a new PWM period starts
- 0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
- 1 = PWM output is driven high on a Fault
- 0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
- 1 = OCx pin is tri-stated on a Fault condition
- 0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** Output Compare x Invert bit
- 1 = OCx output is inverted
- 0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
- 1 = Cascade module operation is enabled
- 0 = Cascade module operation is disabled

bit 7 **OCTRIG:** Output Compare x Trigger/Sync Select bit
- 1 = Triggers OCx from the source designated by the SYNCSELx bits
- 0 = Synchronizes OCx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
- 1 = Timer source has been triggered and is running
- 0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** Output Compare x Output Pin Direction Select bit
- 1 = Output Compare x is tri-stated
- 0 = Output Compare x module drives the OCx pin

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

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REGISTER 16-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL[4:0]:** Trigger/Synchronization Source Selection bits

11111 = OCxRS compare event is used for synchronization
11110 = INT2 is the source for compare timer synchronization
11101 = INT1 is the source for compare timer synchronization
11100 = CTMU trigger is the source for compare timer synchronization
11011 = ADC1 interrupt is the source for compare timer synchronization
11010 = Analog Comparator 3 is the source for compare timer synchronization
11001 = Analog Comparator 2 is the source for compare timer synchronization
11000 = Analog Comparator 1 is the source for compare timer synchronization
10111 = Analog Comparator 5 is the source for compare timer synchronization
10110 = Analog Comparator 4 is the source for compare timer synchronization
10101 = Capture timer is unsynchronized
10100 = Capture timer is unsynchronized
10011 = Input Capture 4 interrupt is the source for compare timer synchronization
10010 = Input Capture 3 interrupt is the source for compare timer synchronization
10001 = Input Capture 2 interrupt is the source for compare timer synchronization
10000 = Input Capture 1 interrupt is the source for compare timer synchronization
01111 = GP Timer5 is the source for compare timer synchronization
01110 = GP Timer4 is the source for compare timer synchronization
01101 = GP Timer3 is the source for compare timer synchronization
01100 = GP Timer2 is the source for compare timer synchronization
01011 = GP Timer1 is the source for compare timer synchronization
01010 = Compare timer is unsynchronized
01001 = Compare timer is unsynchronized
01000 = Capture timer is unsynchronized
00101 = Compare timer is unsynchronized
00100 = Output Compare 4 is the source for compare timer synchronization(1,2)
00011 = Output Compare 3 is the source for compare timer synchronization(1,2)
00010 = Output Compare 2 is the source for compare timer synchronization(1,2)
00001 = Output Compare 1 is the source for compare timer synchronization(1,2)
00000 = Compare timer is unsynchronized

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

NOTES:

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17.0 HIGH-SPEED PWM MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family devices support a dedicated Pulse-Width Modulation (PWM) module with up to six outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM Generators
- Two PWM Outputs per PWM Generator
- Individual Period and Duty Cycle for each PWM Pair
- Duty Cycle, Dead Time, Phase Shift and Frequency Resolution of 8.32 ns
- Independent Fault and Current-Limit Inputs for Six PWM Outputs
- Redundant Output
- Center-Aligned PWM mode
- Output Override Control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for Input Clock
- PWMxL and PWMxH Output Pin Swapping
- Independent PWM Frequency, Duty Cycle and Phase-Shift Changes for each PWM Generator
- Dead-Time Compensation
- Enhanced Leading-Edge Blanking (LEB) Functionality
- Frequency Resolution Enhancement
- PWM Capture Functionality

Note: In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 8.32 ns at 60 MIPS.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on the master time base.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin, that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.

Figure 17-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

17.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs as follows:

- FLT1 and FLT2, available on 28-pin, 36-pin, 44-pin, 48-pin and 64-pin packages, which are remappable using the PPS feature
- FLT3, available on 44-pin, 48-pin and 64-pin packages, which is available as a fixed pin
- FLT4-FLT8, available on 64-pin packages, which are available as fixed pins
- FLT32 is available on a fixed pin on all devices

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

17.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the high-speed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

Note: The Fault mode may be changed using the FLTMOD[1:0] bits (FCLCONx[1:0]), regardless of the state of FLT32.

17.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EVXXXGM00X/10X family devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FDEVOPT[0]). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 17-1.

EXAMPLE 17-1: PWM1 WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

```
; FLT32 pin must be pulled low externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence

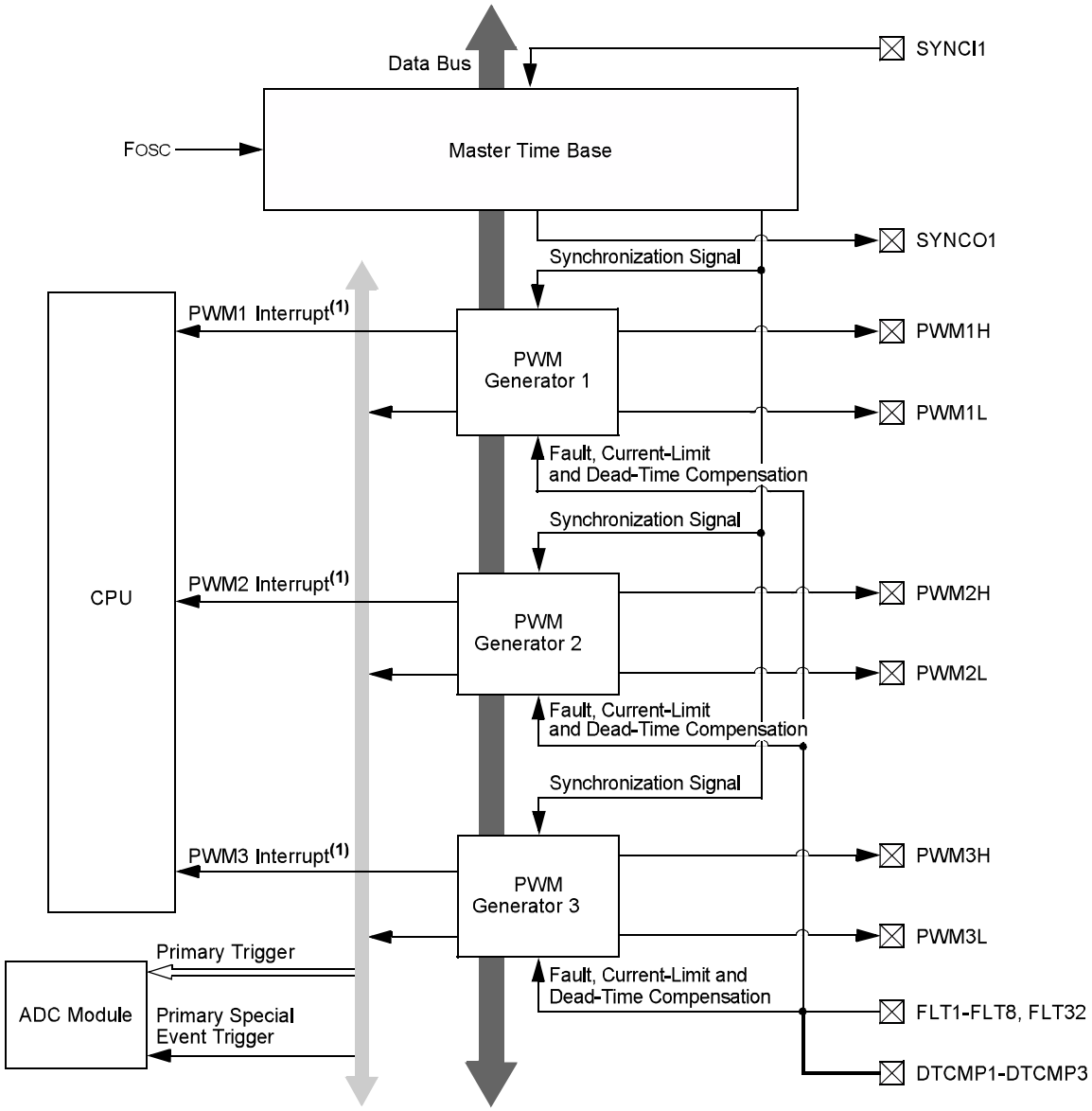
mov #0xabcd, w10       ; Load first unlock key to w10 register
mov #0x4321, w11       ; Load second unlock key to w11 register
mov #0x0000, w0        ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY        ; Write first unlock key to PWMKEY register
mov w11, PWMKEY        ; Write second unlock key to PWMKEY register
mov w0, FCLCON1        ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd, w10       ; Load first unlock key to w10 register
mov #0x4321, w11       ; Load second unlock key to w11 register
mov #0xF000, w0        ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY        ; Write first unlock key to PWMKEY register
mov w11, PWMKEY        ; Write second unlock key to PWMKEY register
mov w0, IOCON1         ; Write desired value to IOCON1 register
```

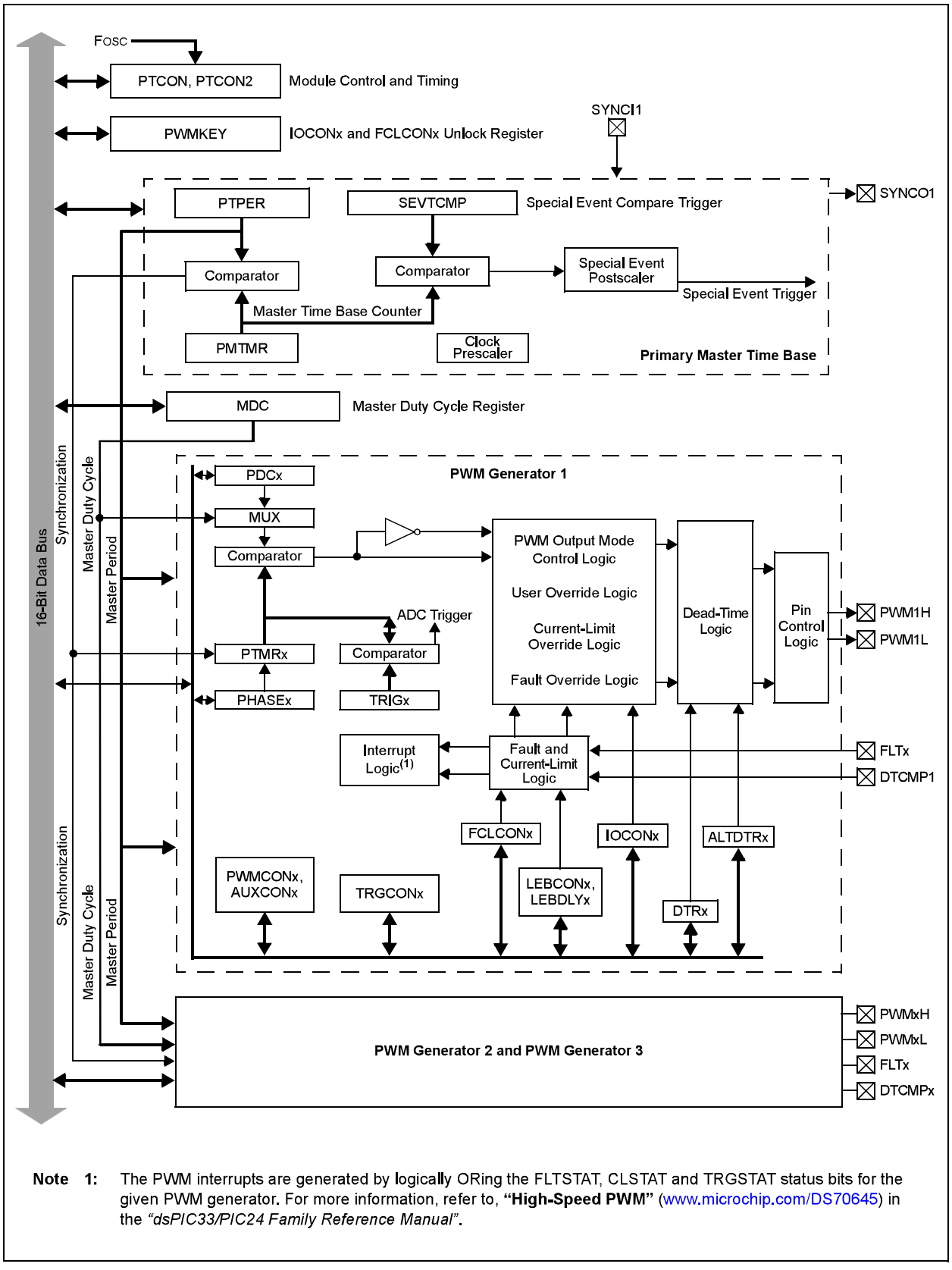

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FIGURE 17-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW



Note 1: The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. For more information, refer to **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 17-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM



Note 1: The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. For more information, refer to, **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"*.

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17.2 PWM Resources

Many useful resources are provided on the main product page on the Microchip website (www.microchip.com) for the devices listed in this data sheet. This product page contains the latest updates and additional information.

Note:	In case the above link is not accessible, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

17.2.1 KEY RESOURCES

- **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

17.3 PWMx Control Registers

REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER

R/W-0	U-0	R/W-0	HC/HS-0	R/W-0	R/W-0	R/W-0	R/W-0
PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU(1)	SYNCPOL(1)	SYNCOEN(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCEN(1)	SYNCSRC2(1)	SYNCSRC1(1)	SYNCSRC0(1)	SEVTPS3(1)	SEVTPS2(1)	SEVTPS1(1)	SEVTPS0(1)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

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REGISTER 17-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 6-4 **SYNCSRC[2:0]:** Synchronous Source Selection bits(1)
111 = Reserved
•
•
•
100 = Reserved
011 = Reserved
010 = Reserved
001 = Reserved
000 = SYNCI1 input from PPS

bit 3-0 **SEVTPS[3:0]:** Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 postscaler generates a Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 postscaler generates a Special Event Trigger on every second compare match event
0000 = 1:1 postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 17-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV[2:0](1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as '0'

bit 2-0 **PCLKDIV[2:0]:** PWMx Input Clock Prescaler (Divider) Select bits(1)
111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 17-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PTPER[15:8]							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
PTPER[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTPER[15:0]:** Primary Master Time Base (PMTMR) Period Value bits

REGISTER 17-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEVTCMP[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SEVTCMP[15:0]:** Special Event Compare Count Value bits

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REGISTER 17-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
CHPCLKEN	—	—	—	—	—	CHOPCLK9	CHOPCLK8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CHOPCLK7	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CHPCLKEN:** Enable Chop Clock Generator bit
1 = Chop clock generator is enabled
0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as '0'

bit 9-0 **CHOPCLK[9:0]:** Chop Clock Divider bits
The frequency of the chop clock signal is given by the following expression:
Chop Frequency = (FP/PCLKDIV[2:0])/(CHOPCLK[9:0] + 1)

REGISTER 17-6: MDC: PWMx MASTER DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **MDC[15:0]:** PWMx Master Duty Cycle Value bits

REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER

HC/HS-0	HC/HS-0	HC/HS-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT(1)	CLSTAT(1)	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB(2)	MDCS(2)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	DTCP(3)	—	—	CAM(2,4)	XPRES(5)	IUE(2)
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = Fault interrupt is not pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = Current-limit interrupt is not pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = Trigger interrupt is not pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = Trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx register provides duty cycle information for this PWM generator

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
3: DTC[1:0] = 11 for DTCP to be effective; else, DTCP is ignored.
4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

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REGISTER 17-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)

bit 7-6 **DTC[1:0]:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all Output modes

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When Set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When Set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWMx time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: These bits should not be changed after the PWMx is enabled (PTEN = 1).
3: DTC[1:0] = 11 for DTCP to be effective; else, DTCP is ignored.
4: The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
5: To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 17-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PDCx[15:0]:** PWMx Generator Duty Cycle Value bits

REGISTER 17-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx[15:0]:** PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

Note 1: If ITB (PWMCONx[9]) = 0, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output modes (PMOD[1:0] (IOCONx[11:10]) = 00, 01 or 10),
PHASEx[15:0] = Phase-shift value for PWMxH and PWMxL outputs.

2: If ITB (PWMCONx[9]) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output modes (PMOD[1:0] (IOCONx[11:10]) = 00, 01 or 10),
PHASEx[15:0] = Independent Time Base period value for PWMxH and PWMxL.

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REGISTER 17-10: DTRx: PWMx DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DTRx[13:8]					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DTRx[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **DTRx[13:0]:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 17-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ALTDTRx[13:8]					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ALTDTRx[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **ALTDTRx[13:0]:** Unsigned 14-Bit Alternate Dead-Time Value for PWMx Dead-Time Unit bits

REGISTER 17-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TRGSTRT5(1)	TRGSTRT4(1)	TRGSTRT3(1)	TRGSTRT2(1)	TRGSTRT1(1)	TRGSTRT0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **TRGDIV[3:0]:** Trigger Output Divider bits
1111 = Triggers output for every 16th trigger event
1110 = Triggers output for every 15th trigger event
1101 = Triggers output for every 14th trigger event
1100 = Triggers output for every 13th trigger event
1011 = Triggers output for every 12th trigger event
1010 = Triggers output for every 11th trigger event
1001 = Triggers output for every 10th trigger event
1000 = Triggers output for every 9th trigger event
0111 = Triggers output for every 8th trigger event
0110 = Triggers output for every 7th trigger event
0101 = Triggers output for every 6th trigger event
0100 = Triggers output for every 5th trigger event
0011 = Triggers output for every 4th trigger event
0010 = Triggers output for every 3rd trigger event
0001 = Triggers output for every 2nd trigger event
0000 = Triggers output for every trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT[5:0]:** Trigger Postscaler Start Enable Select bits(1)
111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

Note 1: The secondary PWM generator cannot generate PWMx trigger interrupts.

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REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER(2)

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PENH	PENL	POLH	POLL	PMOD1(1)	PMOD0(1)	OVRENH	OVRENL
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWMx module controls the PWMxH pin
0 = GPIO module controls the PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWMx module controls the PWMxL pin
0 = GPIO module controls the PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD[1:0]:** PWMx I/O Pin Mode bits(1)
11 = Reserved; do not use
10 = PWMx I/O pin pair is in the Push-Pull Output mode
01 = PWMx I/O pin pair is in the Redundant Output mode
00 = PWMx I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT1 controls the output on the PWMxH pin
0 = PWMx generator controls the PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT0 controls the output on the PWMxL pin
0 = PWMx generator controls the PWMxL pin

bit 7-6 **OVRDAT[1:0]:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT1.
If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT0.

bit 5-4 **FLTDAT[1:0]:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
If Fault is active, PWMxH is driven to the state specified by FLTDAT1.
If Fault is active, PWMxL is driven to the state specified by FLTDAT0.

bit 3-2 **CLDAT[1:0]:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits
If current limit is active, PWMxH is driven to the state specified by CLDAT1.
If current limit is active, PWMxL is driven to the state specified by CLDAT0.

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FDEVOPT[0]) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-13: IOCONx: PWMx I/O CONTROL REGISTER(2) (CONTINUED)

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to the PWMxL pin; PWMxL output signal is connected to the PWMxH pin
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides through the OVRDAT[1:0] bits are synchronized to the PWMx time base
0 = Output overrides through the OVRDAT[1:0] bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FDEVOPT[0]) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 17-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TRGCMP[15:0]:** Trigger Control Value bits
When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

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REGISTER 17-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER(1)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL(2)	CLMOD
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL(2)	FLTMOD1	FLTMOD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-10 **CLSRC[4:0]:** Current-Limit Control Signal Source Select for PWM Generator x bits
11111 = Fault 32
11110 = Reserved
•
•
•
01100 = Op Amp/Comparator 5
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Fault 8
00110 = Fault 7
00101 = Fault 6
00100 = Fault 5
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1 **(default)**

bit 9 **CLPOL:** Current-Limit Polarity for PWM Generator x bit(2)
1 = The selected current-limit source is active-low
0 = The selected current-limit source is active-high

bit 8 **CLMOD:** Current-Limit Mode Enable for PWM Generator x bit
1 = Current-Limit mode is enabled
0 = Current-Limit mode is disabled

Note 1: If the PWMLOCK Configuration bit (FDEVOPT[0]) is a '1', the FCLCONx register can only be written after the unlock sequence has been executed.

2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 17-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER(1) (CONTINUED)

bit 7-3 **FLTSRC[4:0]:** Fault Control Signal Source Select for PWM Generator x bits
11111 = Fault 32 **(default)**
11110 = Reserved
•
•
•
01100 = Op Amp/Comparator 5
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Fault 8
00110 = Fault 7
00101 = Fault 6
00100 = Fault 5
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1

bit 2 **FLTPOL:** Fault Polarity for PWM Generator x bit(2)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD[1:0]:** Fault Mode for PWM Generator x bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT[1:0] values (cycle)
00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDAT[1:0] values (latched condition)

Note 1: If the PWMLOCK Configuration bit (FDEVOPT[0]) is a '1', the FCLCONx register can only be written after the unlock sequence has been executed.

2: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

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REGISTER 17-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH(1)	BCL(1)	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected Fault input
0 = Leading-Edge Blanking is not applied to the selected Fault input

bit 10 **CLLEBEN:** Current-Limit Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected current-limit input
0 = Leading-Edge Blanking is not applied to the selected current-limit input

bit 9-6 **Unimplemented:** Read as '0'

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when the selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when the selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is high
0 = No blanking when the PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxH output is low
0 = No blanking when the PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is high
0 = No blanking when the PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when the PWMxL output is low
0 = No blanking when the PWMxL output is low

Note 1: The blanking signal is selected through the BLANKSEL[3:0] bits in the AUXCONx register.

REGISTER 17-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	LEB[11:8]			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LEB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB[11:0]:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

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REGISTER 17-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BLANKSEL[3:0]:** PWMx State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled through the BCH and BCL bits in the LEBCONx register).

1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H is selected as the state blank source
0010 = PWM2H is selected as the state blank source
0001 = PWM1H is selected as the state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL[3:0]:** PWMx Chop Clock Source Select bits

The selected signal will enable and disable (Chop) the selected PWMx outputs.

1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H is selected as the chop clock source
0010 = PWM2H is selected as the chop clock source
0001 = PWM1H is selected as the chop clock source
0000 = Chop clock generator is selected as the chop clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

NOTES:

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18.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (www.microchip.com/DS70005185) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Serial Peripheral Interface (SPI) module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces.

The dsPIC33EVXXXGM00X/10X device family offers two SPI modules on a single device, SPI1 and SPI2, that are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of this module, but results in a lower maximum speed. See **Section 30.0 "Electrical Characteristics"** for more information.

The SPIx serial interface consists of the following four pins:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SSx}$/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

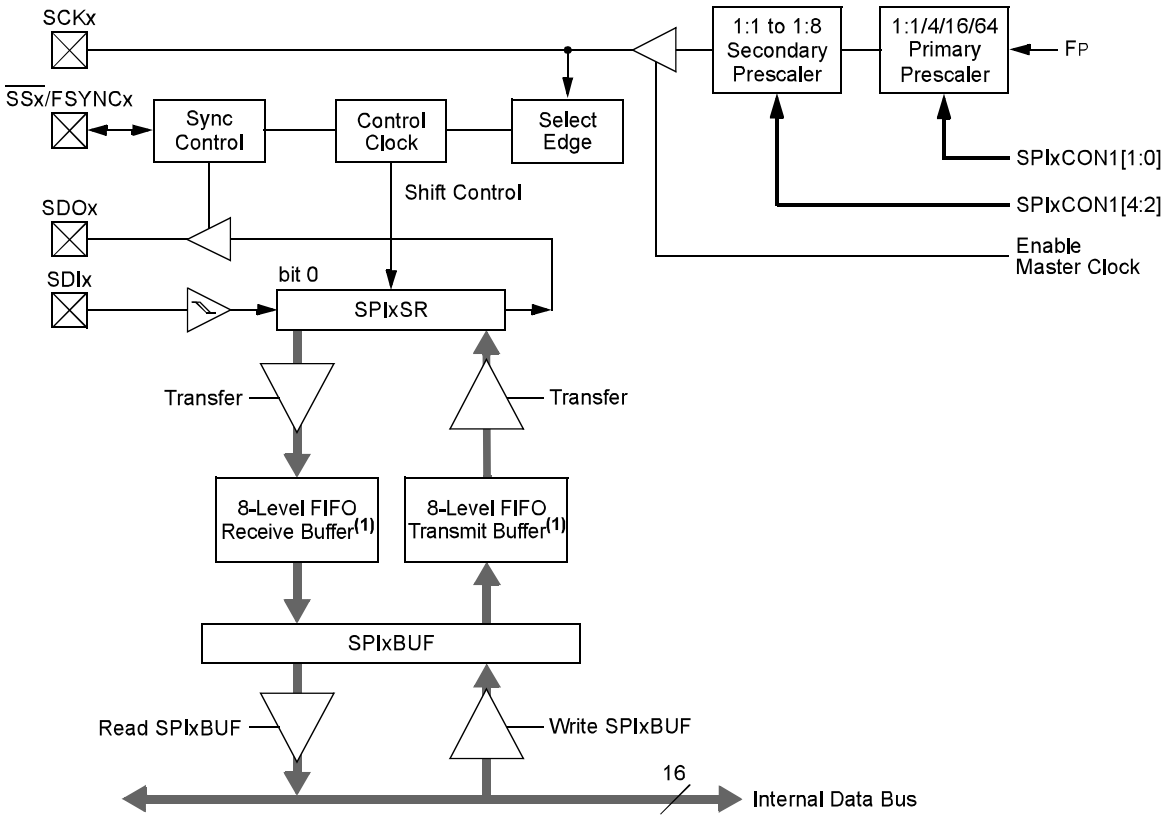
Note: All four pins of the SPIx serial interface must be configured as digital in the ANSELx registers.

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, $\overline{SSx}$ is not used. In 2-pin mode, neither SDOx nor $\overline{SSx}$ is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

Note: When SPI2 is configured as master, the SCK2 pin should be configured as both input and output.

FIGURE 18-1: SPIx MODULE BLOCK DIAGRAM



Note 1: In Standard mode, the FIFO is only one level deep.

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18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2[13]) = 1, use a pull-down resistor on SSx.
   b) If FRMPOL = 0, use a pull-up resistor on SSx.

Note:	This insures that the first frame transmission after initialization is not shifted or corrupted.

2. In Non-Framed 3-Wire mode (i.e., not using SSx from a master):
   a) If CKP (SPIxCON1[6]) = 1, always place a pull-up resistor on SSx.
   b) If CKP = 0, always place a pull-down resistor on SSx.

Note:	This will insure that during power-up and initialization, the master/slave will not lose sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors, for both transmit and receive, appearing as corrupted data.

3. FRMEN (SPIxCON2[15]) = 1 and SSEN (SPIxCON1[7]) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.

Note:	Not all third-party devices support Frame mode timing. For more information, refer to the SPI specifications in **Section 30.0 "Electrical Characteristics"**.

4. In Master mode only, set the SMP bit (SPIxCON1[9]) to a '1' for the fastest SPI data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1[5]) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

18.2 SPI Control Registers

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0
bit 15							bit 8

R/W-0	HS/R/C-0	R/W-0	R/W-0	R/W-0	R/W-0	HS/HC/R-0	HS/HC/R-0
SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	C = Clearable bit

bit 15 **SPIEN:** SPIx Enable bit
1 = Enables the SPIx module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables the SPIx module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues the SPIx module operation when the device enters Idle mode
0 = Continues the SPIx module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **SPIBEC[2:0]:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPIx transfers are pending.
Slave mode:
Number of SPIx transfers are unread.

bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
1 = The SPIx Shift register is empty and ready to send or receive the data
0 = The SPIx Shift register is not empty

bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register
0 = Overflow has not occurred

bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty

bit 4-2 **SISEL[2:0]:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
110 = Interrupt when the last bit is shifted into SPIxSR, and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
100 = Interrupt when one datum is shifted into SPIxSR, and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
010 = Interrupt when the SPIx receive buffer is 3/4 or more full
001 = Interrupt when data are available in the SPIx receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the SPIx receive buffer are read, and as a result, the buffer is empty (SRXMPT bit is set)

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REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit has not yet started, the SPIxTXB bit is full
0 = Transmit has started, the SPIxTXB bit is empty

Standard Buffer mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:
Automatically set in the hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, the SPIxRXB bit is full
0 = Receive is incomplete, the SPIxRXB bit is empty

Standard Buffer mode:
Automatically set in the hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN(2)	CKP	MSTEN	SPRE2(3)	SPRE1(3)	SPRE0(3)	PPRE1(3)	PPRE0(3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPI Master modes only)
1 = Internal SPI clock is disabled, pin functions as I/O
0 = Internal SPI clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit
1 = SDOx pin is not used by the module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
1 = Input data are sampled at the end of data output time
0 = Input data are sampled at the middle of data output time
Slave mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** Clock Edge Select bit(1)
1 = Serial output data change on transition from active clock state to Idle clock state (refer to bit 6)
0 = Serial output data change on transition from Idle clock state to active clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used for Slave mode
0 = $\overline{SSx}$ pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
2: This bit must be cleared when FRMEN = 1.
3: Do not set both primary and secondary prescalers to the value of 1:1.

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REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE[2:0]:** Secondary Prescale bits (Master mode)(3)
111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE[1:0]:** Primary Prescale bits (Master mode)(3)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).

2: This bit must be cleared when FRMEN = 1.

3: Do not set both primary and secondary prescalers to the value of 1:1.

REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
FRMEN	SPIFSD	FRMPOL	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	FRMDLY	SPIBEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled ($\overline{SSx}$ pin is used as the Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** SPIx Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with the first bit clock
0 = Frame Sync pulse precedes the first bit clock

bit 0 **SPIBEN:** SPIx Enhanced Buffer Enable bit
1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Standard mode)

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19.0 INTER-INTEGRATED CIRCUIT (I^2C)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Inter-Integrated Circuit (I^2C)"** (www.microchip.com/DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family of devices contains one Inter-Integrated Circuit (I^2C) module, I2C1.

The I^2C module provides complete hardware support for both Slave and Multi-Master modes of the I^2C serial communication standard, with a 16-bit interface.

The I^2C module has the following 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The I^2C module offers the following key features:

- I^2C Interface Supporting Both Master and Slave modes of Operation
- I^2C Slave mode Supports 7 and 10-Bit Addressing
- I^2C Master mode Supports 7 and 10-Bit Addressing
- I^2C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for I^2C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I^2C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- Support for Address Bit Masking up to Lower Seven Bits
- I^2C Slave Enhancements:
  - SDAx hold time selection of SMBus (300 ns or 150 ns)
  - Start/Stop bit interrupt enables

Figure 19-1 shows a block diagram of the I^2C module.

19.1 I^2C Baud Rate Generator

The Baud Rate Generator (BRG) used for I^2C mode operation is used to set the SCL clock frequency for 100 kHz, 400 kHz and 1 MHz. The BRG reload value is contained in the I2CxBRG register. The BRG will automatically begin counting on a write to the I2CxTRN register.

Equation 19-1 and Equation 19-2 provide the BRG reload formula and FSCL frequency, respectively.

EQUATION 19-1: BRG FORMULA

$$I2CxBRG = \left(\left(\frac{1}{F_{SCL}} - Delay\right) \times \frac{F_{CY}}{2}\right) - 2$$

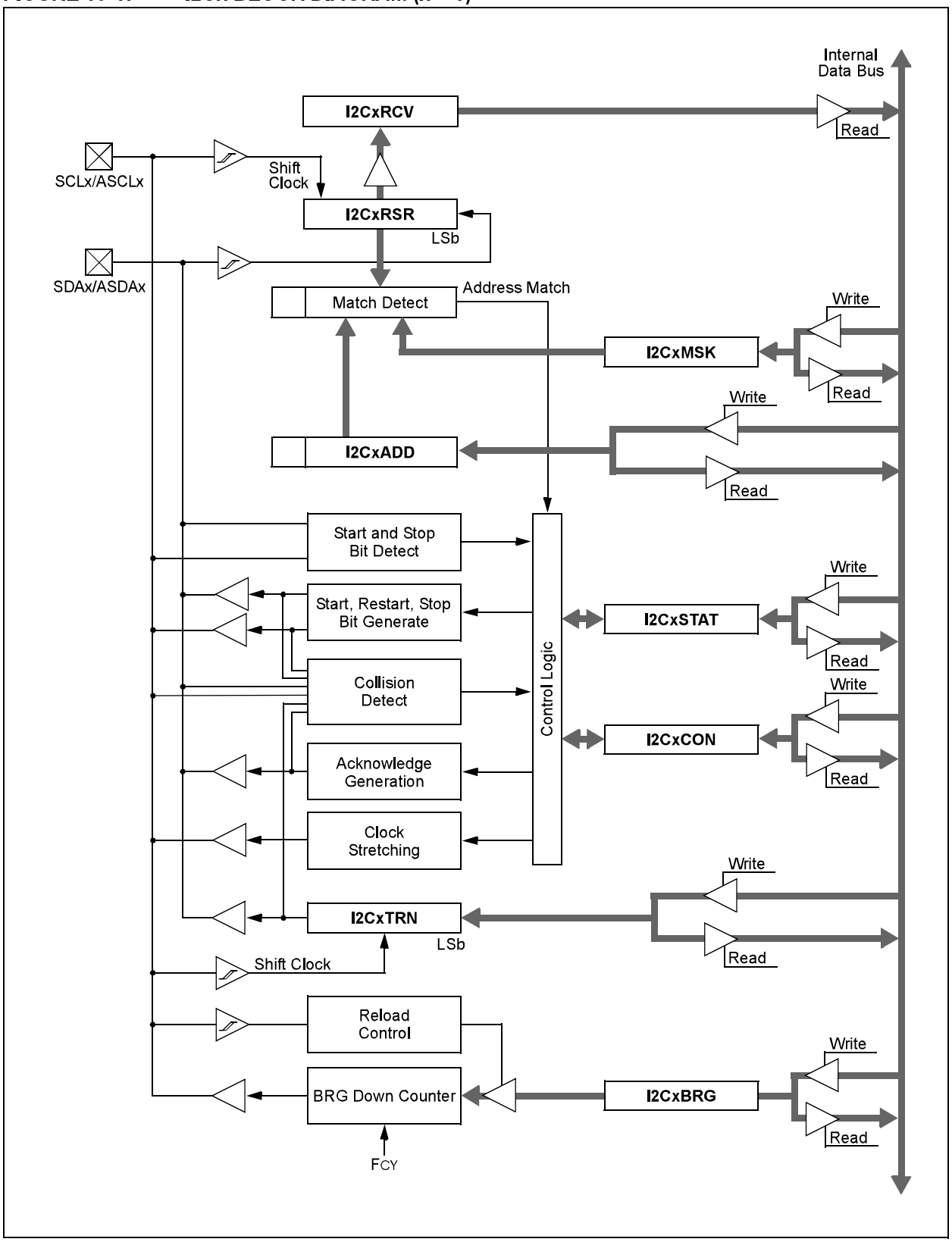
Where:

Delay varies from 110 ns to 130 ns.

EQUATION 19-2: FSCL FREQUENCY

$$F_{SCL} = F_{CY}/((I2CxBRG + 2) * 2)$$

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1)



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19.2 I²C Control Registers

REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/S-1	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL(1)	STRICT	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	HC/R/W-0	HC/R/W-0	HC/R/W-0	HC/R/W-0	HC/R/W-0
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	S = Settable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **I2CEN:** I2Cx Enable bit (writable from SW only)
1 = Enables the I²C module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I²C module and all I²C pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (I²C Slave mode only)(1)
Module resets and (I2CEN = 0) sets SCLREL = 1.
If STREN = 0:(2)
1 = Releases clock
0 = Forces clock low (clock stretch)
If STREN = 1:
1 = Releases clock
0 = Holds clock low (clock stretch); user may program this bit to '0', clock stretch at the next SCLx low

bit 11 **STRICT:** Strict I²C Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced
In Slave mode, the device does not respond to reserved address space and addresses falling in that category are NACKed.
0 = Reserved addressing would be Acknowledged
In Slave mode, the device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK.

bit 10 **A10M:** 10-Bit Slave Address Flag bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Slew Rate Control Disable bit
1 = Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode)
0 = Slew rate control is enabled for High-Speed mode (400 kHz)

bit 8 **SMEN:** SMBus Input Levels Enable bit
1 = Enables the input logic so thresholds are compliant with the SMBus specification
0 = Disables the SMBus-specific inputs

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.
2: Automatically cleared to '0' at the beginning of slave transmission.

REGISTER 19-1: I2CxCON1: I2Cx CONTROL REGISTER 1 (CONTINUED)

bit 7 **GCEN:** General Call Enable bit (I^2C Slave mode only)
1 = Enables interrupt when a general call address is received in I2CxRSR; module is enabled for reception
0 = General call address is disabled.

bit 6 **STREN:** SCLx Clock Stretch Enable bit
In I^2C Slave mode only, used in conjunction with the SCLREL bit.
1 = Enables clock stretching
0 = Disables clock stretching

bit 5 **ACKDT:** Acknowledge Data bit
In I^2C Master mode, during Master Receive mode. The value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In I^2C Slave mode when AHEN = 1 or DHEN = 1. The value that the slave will transmit when it initiates an Acknowledge sequence at the end of an address or data reception.
1 = NACK is sent
0 = ACK is sent

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
In I^2C Master mode only; applicable during Master Receive mode.
1 = Initiates Acknowledge sequence on SDAx and SCLx pins, and transmits ACKDT data bit
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (I^2C Master mode only)
1 = Enables Receive mode for I^2C, automatically cleared by hardware at the end of 8-bit receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (I^2C Master mode only)
1 = Initiates Stop condition on SDAx and SCLx pins
0 = Stop condition is Idle

bit 1 **RSEN:** Restart Condition Enable bit (I^2C Master mode only)
1 = Initiates Restart condition on SDAx and SCLx pins
0 = Restart condition is Idle

bit 0 **SEN:** Start Condition Enable bit (I^2C Master mode only)
1 = Initiates Start condition on SDAx and SCLx pins
0 = Start condition is Idle

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.

2: Automatically cleared to '0' at the beginning of slave transmission.

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REGISTER 19-2: I2CxCON2: I2Cx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = The I2CxRCV register bit is updated and an ACK is generated for a received address/data byte, ignoring the state of the I2COV bit only if the RBF bit = 0
0 = The I2CxRCV register bit is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCLx, SDAx is sampled low when the module is outputting a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.
1 = Slave bus collision interrupts are enabled
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8^{th} falling edge of SCLx for a matching received address byte; the SCLREL bit (I2CxCON1[12]) will be cleared and the SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8^{th} falling edge of SCLx for a received data byte; slave hardware clears the SCLREL bit (I2CxCON1[12]) and the SCLx is held low
0 = Data holding is disabled

REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER

HSC/R-0	HSC/R-0	HSC/R-0	U-0	U-0	HSC/R/C-0	HSC/R-0	HSC/R-0
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

HS/R/C-0	HS/R/C-0	HSC/R-0	HSC/R/C-0	HSC/R/C-0	HSC/R-0	HSC/R-0	HSC/R-0
IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 15 **ACKSTAT:** Acknowledge Status bit (updated in all Master and Slave modes)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C master; applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + $\overline{ACK}$)
0 = Master transmit is not in progress

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^2C Slave mode only)
1 = Indicates I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Bus Collision Detect bit (Master/Slave mode; cleared when I^2C module is disabled, I2CEN = 0)
1 = A bus collision has been detected during a master or slave transmit operation
0 = Bus collision has not been detected

bit 9 **GCSTAT:** General Call Status bit (cleared after Stop detection)
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-Bit Address Status bit (cleared after Stop detection)
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy; must be cleared in software
0 = Collision has not occurred

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
0 = Overflow has not occurred

bit 5 **D_A:** Data/Address bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received or transmitted was an address

bit 4 **P:** I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.
1 = Indicates that a Stop bit has been detected last
0 = Indicates that a Stop bit was not detected last

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REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 3 **S:** I2Cx Start bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Indicates that a Start bit was not detected last

bit 2 **R_W:** Read/Write Information bit (when operating as I^2C slave)
1 = Read: Indicates that the data transfer is output from the slave
0 = Write: Indicates that the data transfer is input to the slave

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, the I2CxRCV bit is full
0 = Receive is not complete, the I2CxRCV bit is empty

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit is in progress, I2CxTRN is full (8 bits of data)
0 = Transmit is complete, I2CxTRN is empty

REGISTER 19-4: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	MSK[9:8]	
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MSK[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **MSK[9:0]:** I2Cx Mask for Address Bit x Select bits
1 = Enables masking for bit x of the incoming message address; bit match is not required in this position
0 = Disables masking for bit x; bit match is required in this position

NOTES:

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20.0 SINGLE-EDGE NIBBLE TRANSMISSION (SENT)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Single-Edge Nibble Transmission (SENT) Module"** (www.microchip.com/DS70005145) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

20.1 Module Introduction

The Single-Edge Nibble Transmission (SENT) module is based on the SAE J2716, *"SENT – Single-Edge Nibble Transmission for Automotive Applications"*. The SENT protocol is a one-way, single wire time modulated serial communication, based on successive falling edges. It is intended for use in applications where high-resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU).

The SENTx module has the following major features:

- Selectable Transmit or Receive mode
- Synchronous or Asynchronous Transmit modes
- Automatic Data Rate Synchronization
- Optional Automatic Detection of CRC Errors in Receive mode
- Optional Hardware Calculation of CRC in Transmit mode
- Support for Optional Pause Pulse Period
- Data Buffering for One Message Frame
- Selectable Data Length for Transmit/Receive from Three to Six Nibbles
- Automatic Detection of Framing Errors

SENT protocol timing is based on a predetermined time unit, TTICK. Both the transmitter and receiver must be preconfigured for TTICK, which can vary from 3 to 90 µs. A SENT message frame starts with a Sync pulse. The purpose of the Sync pulse is to allow the receiver to calculate the data rate of the message encoded by the transmitter. The SENT specification allows messages to be validated with up to a 20% variation in TTICK. This allows for the transmitter and receiver to run from different clocks that may be inaccurate, and drift with time and temperature. The data nibbles are four bits in length and are encoded as the data value + 12 ticks. This yields a 0 value of 12 ticks and the maximum value, 0xF, of 27 ticks.

A SENT message consists of the following:

- A synchronization/calibration period of 56 tick times
- A status nibble of 12-27 tick times
- Up to six data nibbles of 12-27 tick times
- A CRC nibble of 12-27 tick times
- An optional pause pulse period of 12-768 tick times

Figure 20-1 shows a block diagram of the SENTx module.

Figure 20-2 shows the construction of a typical 6-nibble data frame, with the numbers representing the minimum or maximum number of tick times for each section.

FIGURE 20-1: SENTx MODULE BLOCK DIAGRAM

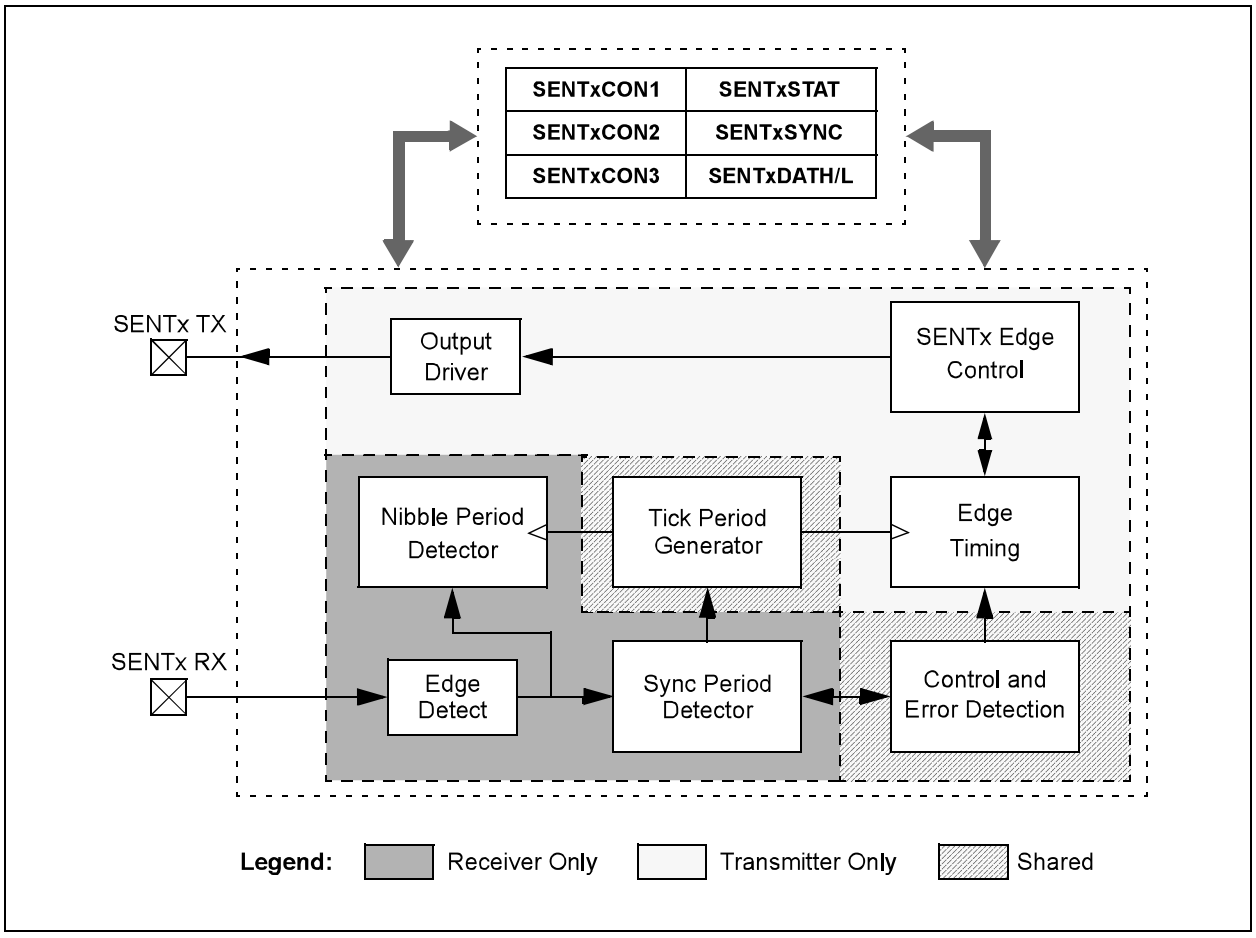
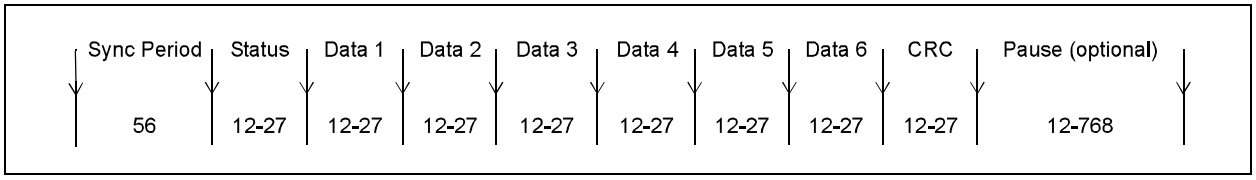


FIGURE 20-2: SENTx PROTOCOL DATA FRAMES



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20.2 Transmit Mode

By default, the SENTx module is configured for transmit operation. The module can be configured for continuous asynchronous message frame transmission, or alternatively, for Synchronous mode triggered by software. When enabled, the transmitter will send a Sync followed by the appropriate number of data nibbles, an optional CRC and optional pause pulse. The tick period used by the SENTx transmitter is set by writing a value to the TICKTIME[15:0] (SENTxCON2[15:0]) bits. The tick period calculations are shown in Equation 20-1.

EQUATION 20-1: TICK PERIOD CALCULATION

$$TICKTIME[15:0] = \frac{T_{TICK}}{T_{CLK}} - 1$$

An optional pause pulse can be used in Asynchronous mode to provide a fixed message frame time period. The frame period used by the SENTx transmitter is set by writing a value to the FRAMETIME[15:0] (SENTxCON3[15:0]) bits. The formulas used to calculate the value of frame time are shown in Equation 20-2.

EQUATION 20-2: FRAME TIME CALCULATIONS

$$FRAMETIME[15:0] = T_{TICK}/T_{FRAME}$$

$$FRAMETIME[15:0] \geq 122 + 27N$$

$$FRAMETIME[15:0] \geq 848 + 12N$$

Where:

T_{FRAME} = Total time of the message from ms

N = The number of data nibbles in message, 1-6

Note: The module will not produce a pause period with less than 12 ticks, regardless of the FRAMETIME[15:0] value. FRAMETIME[15:0] values beyond 2047 will have no effect on the length of a data frame.

20.2.1 TRANSMIT MODE CONFIGURATION

20.2.1.1 Initializing the SENTx Module:

Perform the following steps to initialize the module:

1. Write RCVEN (SENTxCON1[11]) = 0 for Transmit mode.
2. Write TXM (SENTxCON1[10]) = 0 for Asynchronous Transmit mode or TXM = 1 for Synchronous mode.
3. Write NIBCNT[2:0] (SENTxCON1[2:0]) for the desired data frame length.
4. Write CRCEN (SENTxCON1[8]) for hardware or software CRC calculation.
5. Write PPP (SENTxCON1[7]) for optional pause pulse.
6. If PPP = 1, write TFRAME to SENTxCON3.
7. Write SENTxCON2 with the appropriate value for desired tick period.
8. Enable interrupts and set interrupt priority.
9. Write initial status and data values to SENTxDATH/L.
10. If CRCEN = 0, calculate CRC and write the value to CRC[3:0] (SENTxDATL[3:0]).
11. Set the SNTEN (SENTxCON1[15]) bit to enable the module.

User software updates to SENTxDATH/L must be performed after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt to trigger data writes.

20.3 Receive Mode

The module can be configured for receive operation by setting the RCVEN (SENTxCON1[11]) bit. The time between each falling edge is compared to SYNCMIN[15:0] (SENTxCON3[15:0]) and SYNCMAX[15:0] (SENTxCON2[15:0]), and if the measured time lies between the minimum and maximum limits, the module begins to receive data. The validated Sync time is captured in the SENTxSYNC register and the tick time is calculated. Subsequent falling edges are verified to be within the valid data width and the data are stored in the SENTxDATH/L register. An interrupt event is generated at the completion of the message and the user software should read the SENTx Data register before the reception of the next nibble. The equation for SYNCMIN[15:0] and SYNCMAX[15:0] is shown in Equation 20-3.

EQUATION 20-3: SYNCMIN[15:0] AND SYNCMAX[15:0] CALCULATIONS

$$T_{TICK} = T_{CLK} \bullet (TICKTIME[15:0] + 1)$$

$$FRAMETIME[15:0] = T_{TICK}/T_{FRAME}$$

$$SyncCount = 8 \times F_{RCV} \times T_{TICK}$$

$$SYNCMIN[15:0] = 0.8 \times SyncCount$$

$$SYNCMAX[15:0] = 1.2 \times SyncCount$$

$$FRAMETIME[15:0] \geq 122 + 27N$$

$$FRAMETIME[15:0] \geq 848 + 12N$$

Where:

T_{FRAME} = Total time of the message from ms

N = The number of data nibbles in message, 1-6

F_{RCV} = FCY x prescaler

T_{CLK} = FCY/Prescaler

For TTICK = 3.0 µs and FCLK = 4 MHz, SYNCMIN[15:0] = 76.

Note: To ensure a Sync period can be identified, the value written to SYNCMIN[15:0] must be less than the value written to SYNCMAX[15:0].

20.3.1 RECEIVE MODE CONFIGURATION

20.3.1.1 Initializing the SENTx Module:

Perform the following steps to initialize the module:

1. Write RCVEN (SENTxCON1[11]) = 1 for Receive mode.
2. Write NIBCNT[2:0] (SENTxCON1[2:0]) for the desired data frame length.
3. Write CRCEN (SENTxCON1[8]) for hardware or software CRC validation.
4. Write PPP (SENTxCON1[7]) = 1 if pause pulse is present.
5. Write SENTxCON2 with the value of SYNCMAXx (Nominal Sync Period + 20%).
6. Write SENTxCON3 with the value of SYNCMINx (Nominal Sync Period – 20%).
7. Enable interrupts and set interrupt priority.
8. Set the SNTEN (SENTxCON1[15]) bit to enable the module.

The data should be read from the SENTxDATH/L register after the completion of the CRC and before the next message frame's status nibble. The recommended method is to use the message frame completion interrupt trigger.

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REGISTER 20-1: SENTxCON1: SENTx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SNTEN	—	SNTSIDL	—	RCVEN	TXM(1)	TXPOL(1)	CRCEN
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PPP	SPCEN(2)	—	PS	—	NIBCNT2	NIBCNT1	NIBCNT0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **SNTEN:** SENTx Enable bit
1 = SENTx is enabled
0 = SENTx is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **SNTSIDL:** SENTx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **Unimplemented:** Read as '0'

bit 11 **RCVEN:** SENTx Receive Enable bit
1 = SENTx operates as a receiver
0 = SENTx operates as a transmitter (sensor)

bit 10 **TXM:** SENTx Transmit Mode bit(1)
1 = SENTx transmits data frame only when triggered using the SYNCTXEN status bit
0 = SENTx transmits data frames continuously while SNTEN = 1

bit 9 **TXPOL:** SENTx Transmit Polarity bit(1)
1 = SENTx data output pin is low in the Idle state
0 = SENTx data output pin is high in the Idle state

bit 8 **CRCEN:** CRC Enable bit
Module in Receive Mode (RCVEN = 1):
1 = SENTx performs CRC verification on received data using the preferred J2716 method
0 = SENTx does not perform CRC verification on received data
Module in Transmit Mode (RCVEN = 1):
1 = SENTx automatically calculates CRC using the preferred J2716 method
0 = SENTx does not calculate CRC

bit 7 **PPP:** Pause Pulse Present bit
1 = SENTx is configured to transmit/receive SENT messages with pause pulse
0 = SENTx is configured to transmit/receive SENT messages without pause pulse

bit 6 **SPCEN:** Short PWM Code Enable bit(2)
1 = SPC control from external source is enabled
0 = SPC control from external source is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **PS:** SENTx Module Clock Prescaler (divider) bits
1 = Divide-by-4
0 = Divide-by-1

Note 1: This bit has no function in Receive mode (RCVEN = 1).
2: This bit has no function in Transmit mode (RCVEN = 0).

REGISTER 20-1: SENTxCON1: SENTx CONTROL REGISTER 1 (CONTINUED)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **NIBCNT[2:0]:** Nibble Count Control bits

111 = Reserved; do not use
110 = Module transmits/receives six data nibbles in a SENT data pocket
101 = Module transmits/receives five data nibbles in a SENT data pocket
100 = Module transmits/receives four data nibbles in a SENT data pocket
011 = Module transmits/receives three data nibbles in a SENT data pocket
010 = Module transmits/receives two data nibbles in a SENT data pocket
001 = Module transmits/receives one data nibble in a SENT data pocket
000 = Reserved; do not use

Note 1: This bit has no function in Receive mode (RCVEN = 1).

2: This bit has no function in Transmit mode (RCVEN = 0).

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REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R/C-0	R-0	HC/R/W-0
PAUSE	NIB2	NIB1	NIB0	CRCERR	FRMERR	RXIDLE	SYNCTXEN(1)
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **PAUSE:** Pause Period Status bit
1 = The module is transmitting/receiving a pause period
0 = The module is not transmitting/receiving a pause period

bit 6-4 **NIB[2:0]:** Nibble Status bit
Module in Transmit Mode (RCVEN = 0):
111 = Module is transmitting a CRC nibble
110 = Module is transmitting Data Nibble 6
101 = Module is transmitting Data Nibble 5
100 = Module is transmitting Data Nibble 4
011 = Module is transmitting Data Nibble 3
010 = Module is transmitting Data Nibble 2
001 = Module is transmitting Data Nibble 1
000 = Module is transmitting a status nibble or pause period, or is not transmitting
Module in Receive Mode (RCVEN = 1):
111 = Module is receiving a CRC nibble or was receiving this nibble when an error occurred
110 = Module is receiving Data Nibble 6 or was receiving this nibble when an error occurred
101 = Module is receiving Data Nibble 5 or was receiving this nibble when an error occurred
100 = Module is receiving Data Nibble 4 or was receiving this nibble when an error occurred
011 = Module is receiving Data Nibble 3 or was receiving this nibble when an error occurred
010 = Module is receiving Data Nibble 2 or was receiving this nibble when an error occurred
001 = Module is receiving Data Nibble 1 or was receiving this nibble when an error occurred
000 = Module is receiving a status nibble or waiting for Sync

bit 3 **CRCERR:** CRC Status bit (Receive mode only)
1 = A CRC error occurred for the 1-6 data nibbles in SENTxDATH/L
0 = A CRC error has not occurred

bit 2 **FRMERR:** Framing Error Status bit (Receive mode only)
1 = A data nibble was received with less than 12 tick periods or greater than 27 tick periods
0 = Framing error has not occurred

bit 1 **RXIDLE:** SENTx Receiver Idle Status bit (Receive mode only)
1 = The SENTx data bus has been Idle (high) for a period of SYNCMAX[15:0] or greater
0 = The SENTx data bus is not Idle

Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

REGISTER 20-2: SENTxSTAT: SENTx STATUS REGISTER (CONTINUED)

bit 0 **SYNCTXEN:** SENTx Synchronization Period Status/Transmit Enable bit(1)

Module in Receive Mode (RCVEN = 1):

1 = A valid synchronization period was detected; the module is receiving nibble data

0 = No synchronization period has been detected; the module is not receiving nibble data

Module in Asynchronous Transmit Mode (RCVEN = 0, TXM = 0):

The bit always reads as '1' when the module is enabled, indicating the module transmits SENTx data frames continuously. The bit reads '0' when the module is disabled.

Module in Synchronous Transmit Mode (RCVEN = 0, TXM = 1):

1 = The module is transmitting a SENTx data frame

0 = The module is not transmitting a data frame, user software may set SYNCTXEN to start another data frame transmission

Note 1: In Receive mode (RCVEN = 1), the SYNCTXEN bit is read-only.

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REGISTER 20-3: SENTxDATL: SENTx RECEIVE DATA REGISTER LOW(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA4[3:0]				DATA5[3:0]			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA6[3:0]				CRC[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **DATA4[3:0]:** Data Nibble 4 Data bits

bit 11-8 **DATA5[3:0]:** Data Nibble 5 Data bits

bit 7-4 **DATA6[3:0]:** Data Nibble 6 Data bits

bit 3-0 **CRC[3:0]:** CRC Nibble Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC[3:0] bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

REGISTER 20-4: SENTxDATH: SENTx RECEIVE DATA REGISTER HIGH(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STAT[3:0]				DATA1[3:0]			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DATA2[3:0]				DATA3[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **STAT[3:0]:** Status Nibble Data bits

bit 11-8 **DATA1[3:0]:** Data Nibble 1 Data bits

bit 7-4 **DATA2[3:0]:** Data Nibble 2 Data bits

bit 3-0 **DATA3[3:0]:** Data Nibble 3 Data bits

Note 1: Register bits are read-only in Receive mode (RCVEN = 1). In Transmit mode, the CRC[3:0] bits are read-only when automatic CRC calculation is enabled (RCVEN = 0, CRCEN = 1).

NOTES:

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21.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EVXXXGM00X/10X family of devices contains two UART modules.

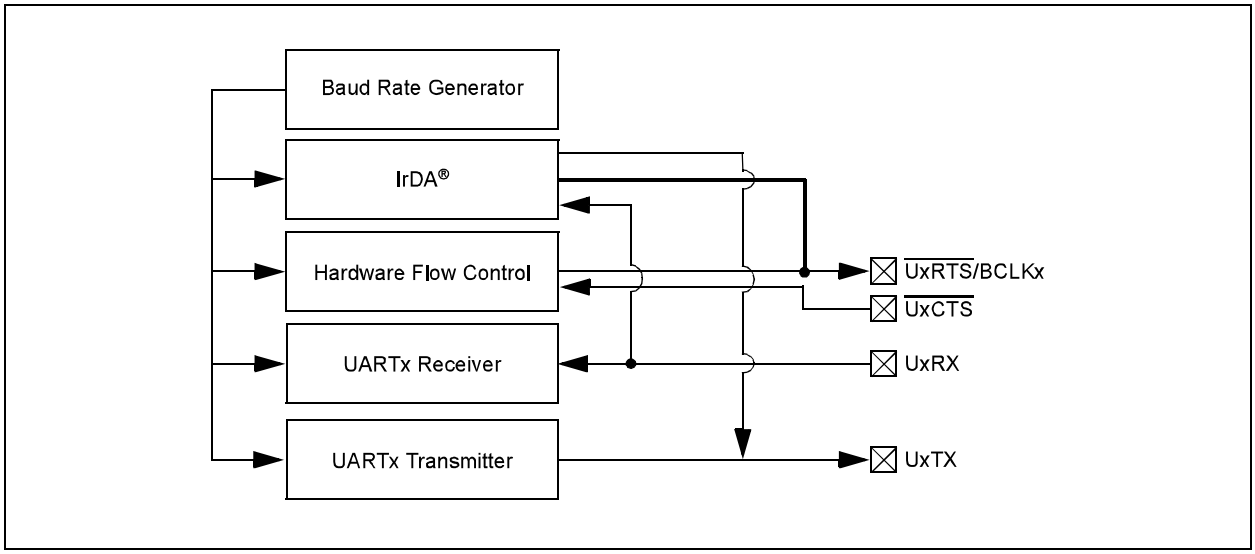
The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EVXXXGM00X/10X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

Note: Hardware flow control using $\overline{\text{UxRTS}}$ and $\overline{\text{UxCTS}}$ is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- Four-Deep First-In First-Out (FIFO) Transmit Data Buffer
- Four-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9^{th} bit = 1)
- Transmit and Receive Interrupts

FIGURE 21-1: UARTx SIMPLIFIED BLOCK DIAGRAM



21.1 UART Helpful Tips

1. In multi-node direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE[4]), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin, depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on wake-up from Sleep mode, caused by activity on the UxRX pin of the UART module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid. This is to be expected.

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21.2 UART Control Registers

REGISTER 21-1: UxMODE: UARTx MODE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
UARTEN(1)	—	USIDL	IREN(2)	RTSMD	—	UEN1	UEN0
bit 15							bit 8

HC/R/W-0	R/W-0	HC/R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN[1:0]
- 0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when the device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN[1:0]:** UARTx Pin Enable bits
- 11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(3)
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used(4)
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(4)
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLKx pins are controlled by PORT latches

bit 7 **WAKE:** UARTx Wake-up on Start bit Detect During Sleep Mode Enable bit
- 1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge, bit is cleared in hardware on the following rising edge
- 0 = Wake-up is not enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Loopback mode is enabled
- 0 = Loopback mode is disabled

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.

2: This feature is only available for the 16x BRG mode (BRGH = 0).

3: This feature is only available on 44-pin, 48-pin and 64-pin devices.

4: This feature is only available on 64-pin devices.

REGISTER 21-1: UxMODE: UARTx MODE REGISTER (CONTINUED)

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Baud rate measurement on the next character is enabled – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or has completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates four clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates sixteen clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL[1:0]:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for receive or transmit operation.
2: This feature is only available for the 16x BRG mode (BRGH = 0).
3: This feature is only available on 44-pin, 48-pin and 64-pin devices.
4: This feature is only available on 64-pin devices.

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REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	HC/R/W-0	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN(1)	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 **UTXISEL[1:0]:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA® encoded UxTX Idle state is '1'
- 0 = IrDA encoded UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or has completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and the buffer is reset; UxTX pin is controlled by the PORT

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register (TSR) Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL[1:0]:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has four data characters)
- 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has three data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for transmit operation.

REGISTER 21-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receive buffer and the UxRSR to the empty state

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UART module for transmit operation.

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22.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EVXXXGM10X DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Enhanced Controller Area Network (ECAN™)"** (www.microchip.com/DS70353) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

22.1 Overview

The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EVXXXGM10X devices contain one CAN module.

The CAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

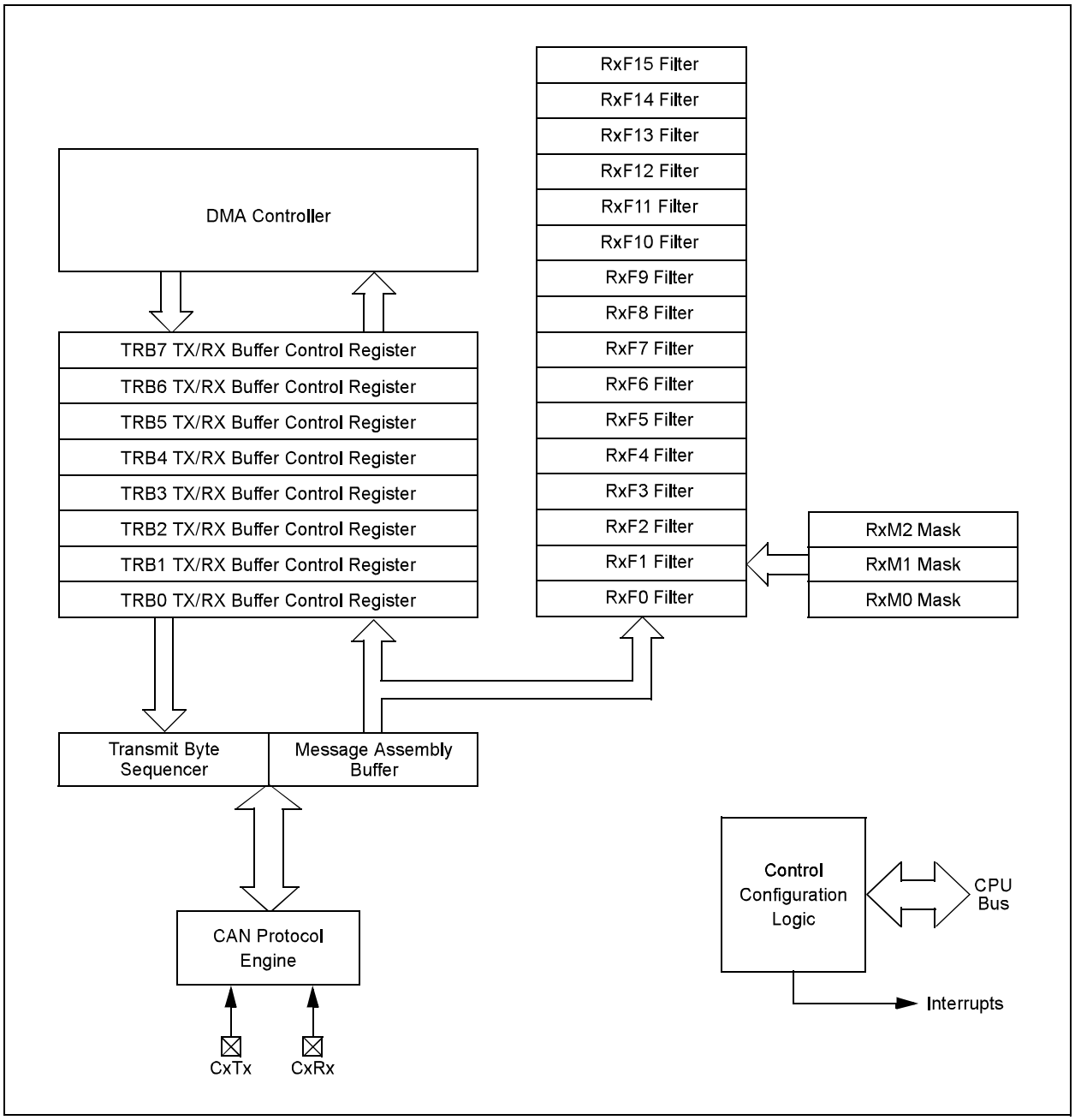
The CAN module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0 to 8-Byte Data Length
- Programmable Bit Rate, up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to Eight Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet™ Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback Mode Supports Self-Test Operation
- Signaling through Interrupt Capabilities for All CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
- Low-Power Sleep and Idle Modes

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors, and then matched against filters to see if it should be received and stored in one of the Receive registers.

Figure 22-1 shows a block diagram of the CANx module.

FIGURE 22-1: CANx MODULE BLOCK DIAGRAM



22.2 Modes of Operation

The CANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP[2:0] bits (CxCTRL1[10:8]). Entry into a mode is Acknowledged by monitoring the OPMODE[2:0] bits (CxCTRL1[7:5]). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least eleven consecutive recessive bits.

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22.3 CAN Control Registers

REGISTER 22-1: CxCTRL1: CANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CANx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** CANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to 2 * FP
0 = FCAN is equal to FP

bit 10-8 **REQOP[2:0]:** Request Operation Mode bits
111 = Sets Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Sets Configuration mode
011 = Sets Listen Only mode
010 = Sets Loopback mode
001 = Sets Disable mode
000 = Sets Normal Operation mode

bit 7-5 **OPMODE[2:0]**: Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CANx Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

REGISTER 22-2: CxCTRL2: CANx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	DNCNT[4:0]				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **DNCNT[4:0]:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection
10001 = Compare up to Data Byte 3, bit 6 with EID[17]
•
•
•
00001 = Compare up to Data Byte 1, bit 7 with EID[0]
00000 = Do not compare data bytes

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REGISTER 22-3: CxVEC: CANx INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT[4:0]:** Filter Hit Number bits
10000-11111 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE[6:0]:** Interrupt Flag Code bits
1000101-1111111 = Reserved
1000100 = FIFO almost full interrupt
1000011 = Receiver overflow interrupt
1000010 = Wake-up interrupt
1000001 = Error interrupt
1000000 = No interrupt
•
•
•
0010000-0111111 = Reserved
0001111 = RB15 buffer interrupt
•
•
•
0001001 = RB9 buffer interrupt
0001000 = RB8 buffer interrupt
0000111 = TRB7 buffer interrupt
0000110 = TRB6 buffer interrupt
0000101 = TRB5 buffer interrupt
0000100 = TRB4 buffer interrupt
0000011 = TRB3 buffer interrupt
0000010 = TRB2 buffer interrupt
0000001 = TRB1 buffer interrupt
0000000 = TRB0 Buffer interrupt

REGISTER 22-4: CxFCTRL: CANx FIFO CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
DMABS2	DMABS1	DMABS0	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	FSA5	FSA4	FSA3	FSA2	FSA1	FSA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **DMABS[2:0]:** DMA Buffer Size bits
111 = Reserved
110 = 32 buffers in RAM
101 = 24 buffers in RAM
100 = 16 buffers in RAM
011 = 12 buffers in RAM
010 = 8 buffers in RAM
001 = 6 buffers in RAM
000 = 4 buffers in RAM

bit 12-6 **Unimplemented:** Read as '0'

bit 5-0 **FSA[5:0]:** FIFO Area Starts with Buffer bits
11111 = Receive Buffer RB31
11110 = Receive Buffer RB30
•
•
•
00001 = TX/RX Buffer TRB1
00000 = TX/RX Buffer TRB0

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REGISTER 22-5: CxFIFO: CANx FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **FBP[5:0]:** FIFO Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **FNRB[5:0]:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

REGISTER 22-6: CxINTF: CANx INTERRUPT FLAG REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN
bit 15							bit 8

R/C-0	R/C-0	R/C-0	U-0	R/C-0	R/C-0	R/C-0	R/C-0
IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **TXBO:** Transmitter in Error State Bus Off bit
1 = Transmitter is in Bus Off state
0 = Transmitter is not in Bus Off state

bit 12 **TXBP:** Transmitter in Error State Bus Passive bit
1 = Transmitter is in Bus Passive state
0 = Transmitter is not in Bus Passive state

bit 11 **RXBP:** Receiver in Error State Bus Passive bit
1 = Receiver is in Bus Passive state
0 = Receiver is not in Bus Passive state

bit 10 **TXWAR:** Transmitter in Error State Warning bit
1 = Transmitter is in Error Warning state
0 = Transmitter is not in Error Warning state

bit 9 **RXWAR:** Receiver in Error State Warning bit
1 = Receiver is in Error Warning state
0 = Receiver is not in Error Warning state

bit 8 **EWARN:** Transmitter or Receiver in Error State Warning bit
1 = Transmitter or receiver is in Error Warning state
0 = Transmitter or receiver is not in Error Warning state

bit 7 **IVRIF:** Invalid Message Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **WAKIF:** Bus Wake-up Activity Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **ERRIF:** Error Interrupt Flag bit (multiple sources in CxINTF[13:8] register)
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as '0'

bit 3 **FIFOIF:** FIFO Almost Full Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **RBOVIF:** RX Buffer Overflow Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

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REGISTER 22-6: CxINTF: CANx INTERRUPT FLAG REGISTER (CONTINUED)

bit 1 **RBIF:** RX Buffer Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **TBIF:** TX Buffer Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 22-7: CxINTE: CANx INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IVRIE:** Invalid Message Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **WAKIE:** Bus Wake-up Activity Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **ERRIE:** Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

REGISTER 22-8: CxEC: CANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT[7:0]							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **TERRCNT[7:0]:** Transmit Error Count bits

bit 7-0 **RERRCNT[7:0]:** Receive Error Count bits

REGISTER 22-9: CxCFG1: CANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW[1:0]:** Synchronization Jump Width bits

11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP[5:0]:** Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN
•
•
•
00 0010 = TQ = 2 x 3 x 1/FCAN
00 0001 = TQ = 2 x 2 x 1/FCAN
00 0000 = TQ = 2 x 1 x 1/FCAN

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REGISTER 22-10: CxCFG2: CANx BAUD RATE CONFIGURATION REGISTER 2

U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit
1 = Uses CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH[2:0]:** Phase Segment 2 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit
1 = Freely programmable
0 = Maximum of SEG1PH[2:0] bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH[2:0]:** Phase Segment 1 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 2-0 **PRSEG[2:0]:** Propagation Time Segment bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

REGISTER 22-11: CxFEN1: CANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN[15:8]							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FLTEN[15:0]:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

REGISTER 22-12: CxBUFPNT1: CANx FILTERS 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F3BP[3:0]:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP[3:0]:** RX Buffer Mask for Filter 2 bits (same values as bits 15-12)

bit 7-4 **F1BP[3:0]:** RX Buffer Mask for Filter 1 bits (same values as bits 15-12)

bit 3-0 **F0BP[3:0]:** RX Buffer Mask for Filter 0 bits (same values as bits 15-12)

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REGISTER 22-13: CxBUFPNT2: CANx FILTERS 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP[3:0]:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP[3:0]:** RX Buffer Mask for Filter 6 bits (same values as bits 15-12)

bit 7-4 **F5BP[3:0]:** RX Buffer Mask for Filter 5 bits (same values as bits 15-12)

bit 3-0 **F4BP[3:0]:** RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

REGISTER 22-14: CxBUFPNT3: CANx FILTERS 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP[3:0]:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP[3:0]:** RX Buffer Mask for Filter 10 bits (same values as bits 15-12)

bit 7-4 **F9BP[3:0]:** RX Buffer Mask for Filter 9 bits (same values as bits 15-12)

bit 3-0 **F8BP[3:0]:** RX Buffer Mask for Filter 8 bits (same values as bits 15-12)

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REGISTER 22-15: CxBUFPNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP[3:0]:** RX Buffer Mask for Filter 15 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP[3:0]:** RX Buffer Mask for Filter 14 bits (same values as bits 15-12)

bit 7-4 **F13BP[3:0]:** RX Buffer Mask for Filter 13 bits (same values as bits 15-12)

bit 3-0 **F12BP[3:0]:** RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

REGISTER 22-16: CxRXFnSID: CANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	EXIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID[10:0]:** Standard Identifier bits
1 = Message address bit, SIDx, must be '1' to match filter
0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses
If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID[17:16]:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

REGISTER 22-17: CxRXFnEID: CANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID[15:0]:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

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REGISTER 22-18: CxFMSKSEL1: CANx FILTERS 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **F7MSK[1:0]:** Mask Source for Filter 7 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain the mask
01 = Acceptance Mask 1 registers contain the mask
00 = Acceptance Mask 0 registers contain the mask

bit 13-12 **F6MSK[1:0]:** Mask Source for Filter 6 bit (same values as bits 15-14)

bit 11-10 **F5MSK[1:0]:** Mask Source for Filter 5 bit (same values as bits 15-14)

bit 9-8 **F4MSK[1:0]:** Mask Source for Filter 4 bit (same values as bits 15-14)

bit 7-6 **F3MSK[1:0]:** Mask Source for Filter 3 bit (same values as bits 15-14)

bit 5-4 **F2MSK[1:0]:** Mask Source for Filter 2 bit (same values as bits 15-14)

bit 3-2 **F1MSK[1:0]:** Mask Source for Filter 1 bit (same values as bits 15-14)

bit 1-0 **F0MSK[1:0]:** Mask Source for Filter 0 bit (same values as bits 15-14)

REGISTER 22-19: CxFMSKSEL2: CANx FILTERS 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK‘	F13MSK0	F12MSK1	F12MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **F15MSK[1:0]:** Mask Source for Filter 15 bit
11 = Reserved
10 = Acceptance Mask 2 registers contain the mask
01 = Acceptance Mask 1 registers contain the mask
00 = Acceptance Mask 0 registers contain the mask

bit 13-12 **F14MSK[1:0]:** Mask Source for Filter 14 bit (same values as bits 15-14)

bit 11-10 **F13MSK[1:0]:** Mask Source for Filter 13 bit (same values as bits 15-14)

bit 9-8 **F12MSK[1:0]:** Mask Source for Filter 12 bit (same values as bits 15-14)

bit 7-6 **F11MSK[1:0]:** Mask Source for Filter 11 bit (same values as bits 15-14)

bit 5-4 **F10MSK[1:0]:** Mask Source for Filter 10 bit (same values as bits 15-14)

bit 3-2 **F9MSK[1:0]:** Mask Source for Filter 9 bit (same values as bits 15-14)

bit 1-0 **F8MSK[1:0]:** Mask Source for Filter 8 bit (same values as bits 15-14)

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REGISTER 22-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID[10:0]:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = Bit, SIDx, is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match, i.e., if:
(Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID)

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID[17:16]:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 22-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID[15:0]:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 22-22: CxRXFUL1: CANx RECEIVE BUFFER FULL REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL[15:8]							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL[7:0]							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL[15:0]:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

REGISTER 22-23: CxRXFUL2: CANx RECEIVE BUFFER FULL REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL[31:24]							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXFUL[23:16]							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXFUL[31:16]:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

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REGISTER 22-24: CxRXOVF1: CANx RECEIVE BUFFER OVERFLOW REGISTER 1

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF[15:8]							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF[7:0]							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF[15:0]:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-25: CxRXOVF2: CANx RECEIVE BUFFER OVERFLOW REGISTER 2

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF[31:24]							
bit 15							bit 8

R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0	R/C-0
RXOVF[23:16]							
bit 7							bit 0

Legend:	C = Writable bit, but only '0' can be written to clear the bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **RXOVF[31:16]:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

REGISTER 22-26: CxTRmnCON: CANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENn	TXABTn	TXLARBn	TXERRn	TXREQn	RTRENn	TXnPRI1	TXnPRI0
bit 15							bit 8

R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
TXENm	TXABTm(1)	TXLARBm(1)	TXERRm(1)	TXREQm	RTRENm	TXmPRI1	TXmPRI0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 See Definition for bits 7-0, controls Buffer n.

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer, TRBm, is a transmit buffer
0 = Buffer, TRBm, is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI[1:0]:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

Note 1: This bit is cleared when TXREQm is set.

Note: The buffers, SID, EID, DLC, Data Field and Receive Status registers, are located in DMA RAM.

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22.4 CAN Message Buffers

CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

BUFFER 22-1: CANx MESSAGE BUFFER WORD 0

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	SID10	SID9	SID8	SID7	SID6
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID5	SID4	SID3	SID2	SID1	SID0	SRR	IDE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-2 **SID[10:0]:** Standard Identifier bits

bit 1 **SRR:** Substitute Remote Request bit

When IDE = 0:
1 = Message will request remote transmission
0 = Normal message

When IDE = 1:
The SRR bit must be set to '1'.

bit 0 **IDE:** Extended Identifier bit

1 = Message will transmit an Extended Identifier
0 = Message will transmit a Standard Identifier

BUFFER 22-2: CANx MESSAGE BUFFER WORD 1

U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	—	EID[17:14]			
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID[13:6]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **EID[17:6]:** Extended Identifier bits

BUFFER 22-3: CANx MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **EID[5:0]:** Extended Identifier bits

bit 9 **RTR:** Remote Transmission Request bit
When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.

bit 8 **RB1:** Reserved Bit 1
User must set this bit to '0' per CAN protocol.

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **RB0:** Reserved Bit 0
User must set this bit to '0' per CAN protocol.

bit 3-0 **DLC[3:0]:** Data Length Code bits

BUFFER 22-4: CANx MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 1[15:8]:** CANx Message Byte 1 bits

bit 7-0 **Byte 0[7:0]:** CANx Message Byte 0 bits

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BUFFER 22-5: CANx MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 3[15:8]:** CANx Message Byte 3 bits

bit 7-0 **Byte 2[7:0]:** CANx Message Byte 2 bits

BUFFER 22-6: CANx MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 5[15:8]:** CANx Message Byte 5 bits

bit 7-0 **Byte 4[7:0]:** CANx Message Byte 4 bits

BUFFER 22-7: CANx MESSAGE BUFFER WORD 6

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 7[15:8]							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 6[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 7[15:8]:** CANx Message Byte 7 bits

bit 7-0 **Byte 6[7:0]:** CANx Message Byte 6 bits

BUFFER 22-8: CANx MESSAGE BUFFER WORD 7

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	FILHIT[4:0](1)				
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT[4:0]:** Filter Hit Code bits(1)
Encodes number of filter that resulted in writing this buffer.

bit 7-0 **Unimplemented:** Read as '0'

Note 1: Only written by module for receive buffers, unused for transmit buffers.

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23.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect"** (www.microchip.com/DS30009743) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

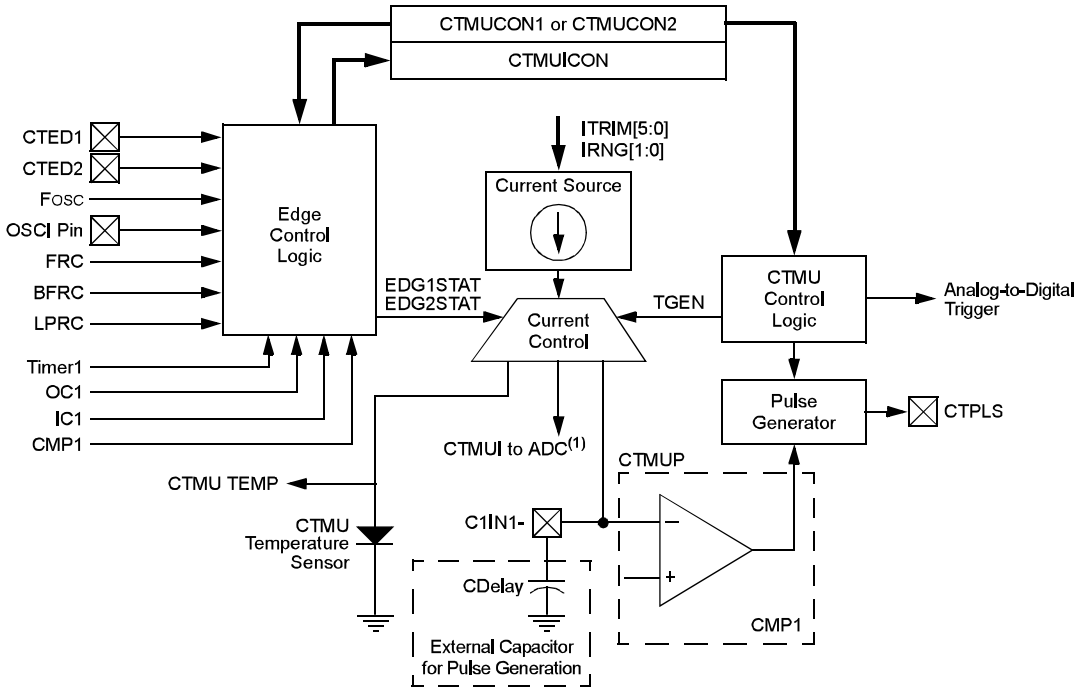
The Charge Time Measurement Unit (CTMU) is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Nine Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Time Measurement Resolution Down to 200 ps
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode
- Pulse Generation Generates a Pulse using the C1INB Comparator Input and Outputs the Pulse onto the CTPLS Remappable Output

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

FIGURE 23-1: CTMU BLOCK DIAGRAM



Current Control Selection	TGEN	EDG1STAT, EDG2STAT
CTMU TEMP	0	EDG1STAT = EDG2STAT
CTMUI to ADC	0	EDG1STAT ≠ EDG2STAT
CTMUP	1	EDG1STAT ≠ EDG2STAT
No Connect	1	EDG1STAT = EDG2STAT

Note 1: Current source to particular ANx pins is provided only when 10-Bit ADC mode is chosen.

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23.1 CTMU Control Registers

REGISTER 23-1: CTMUCON1: CTMU CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CTMUEN	—	CTMUSIDL	TGEN(2)	EDGEN	EDGSEQEN	IDISSEN(1)	CTTRIG
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit(2)
1 = Edge delay generation is enabled
0 = Edge delay generation is disabled

bit 11 **EDGEN:** Edge Enable bit
1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(1)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** ADC Trigger Control bit
1 = CTMU triggers the ADC start of conversion
0 = CTMU does not trigger the ADC start of conversion

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADC module Sample-and-Hold (S&H) capacitor is not automatically discharged between sample/conversion cycles. Any software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

2: If the TGEN bit is set to '1', then the CMP1 module should be selected as the Edge 2 source in the EDG2SELx bits field; otherwise, the module will not function.

REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit
1 = Edge 1 is edge-sensitive
0 = Edge 1 is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL[3:0]:** Edge 1 Source Select bits
1111 = FCY
1110 = OSCI pin
1101 = FRC Oscillator
1100 = BFRC Oscillator
1011 = Internal LPRC Oscillator
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = Reserved
0100 = Reserved
0011 = CTED1 pin
0010 = CTED2 pin
0001 = OC1 module
0000 = TMR1 module

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the edge source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the edge source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit
1 = Edge 2 is edge-sensitive
0 = Edge 2 is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge response
0 = Edge 2 is programmed for a negative edge response

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REGISTER 23-2: CTMUCON2: CTMU CONTROL REGISTER 2 (CONTINUED)

bit 5-2 **EDG2SEL[3:0]:** Edge 2 Source Select bits
1111 = FCY
1110 = OSCI pin
1101 = FRC Oscillator
1100 = BFRC Oscillator
1011 = Internal LPRC Oscillator
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = Reserved
0100 = CMP1 module
0011 = CTED2 pin
0010 = CTED1 pin
0001 = OCMP1 module
0000 = IC1 module

bit 1-0 **Unimplemented:** Read as '0'

REGISTER 23-3: CTMUICON: CTMU CURRENT CONTROL REGISTER(3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5(4)	ITRIM4(4)	ITRIM3(4)	ITRIM2(4)	ITRIM1(4)	ITRIM0(4)	IRNG1(2)	IRNG0(2)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **ITRIM[5:0]:** Current Source Trim bits(4)
011111 = Maximum positive change from nominal current + 62%
011110 = Maximum positive change from nominal current + 60%
•
•
•
000010 = Minimum positive change from nominal current + 4%
000001 = Minimum positive change from nominal current + 2%
000000 = Nominal current output specified by IRNG[1:0]
111111 = Minimum negative change from nominal current – 2%
111110 = Minimum negative change from nominal current – 4%
•
•
•
100010 = Maximum negative change from nominal current – 60%
100001 = Maximum negative change from nominal current – 62%

bit 9-8 **IRNG[1:0]:** Current Source Range Select bits(2)
11 = 100 × Base Current
10 = 10 × Base Current
01 = Base Current Level
00 = 1000 × Base Current(1)

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This current range is not available for use with the internal temperature measurement diode.

2: Refer to the CTMU Current Source Specifications (Table 30-53) in **Section 30.0 "Electrical Characteristics"** for the current range selection values.

3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

4: The current step generated by the Current Source Trim bits is not always linear.

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24.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Analog-to-Digital (ADC) module in the dsPIC33EVXXXGM00X/10X family devices supports up to 36 analog input channels.

The ADC module can be configured by the user as either a 10-bit, four Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, one S&H ADC.

Note: The ADC module needs to be disabled before modifying the AD12B bit.

24.1 Key Features

24.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) Conversion
- Conversion Speeds of up to 1.1 Msps
- Up to 36 Analog Input Pins
- Connections to Four Internal Op Amps
- Connections to the Charge Time Measurement Unit (CTMU) and Temperature Measurement Diode
- Simultaneous Sampling of:
  - Up to four analog input pins
  - Four op amp outputs
- Combinations of Analog Inputs and Op Amp Outputs
- Automatic Channel Scan mode
- Selectable Conversion Trigger Source
- Selectable Buffer Fill modes
- Four Result Alignment Options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle Modes

24.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed previously, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration. Therefore, simultaneous sampling of multiple channels is not supported.

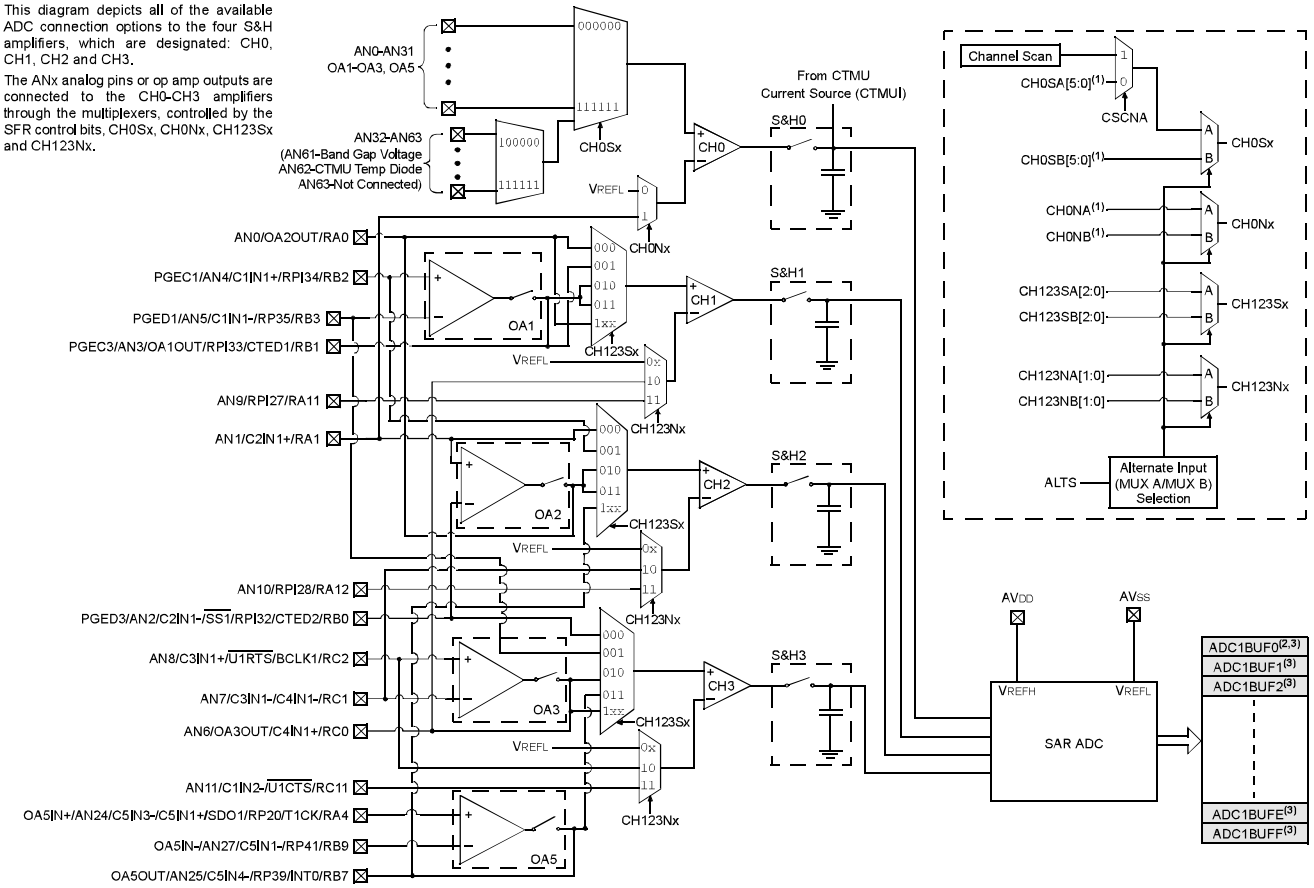
The ADC has up to 36 analog inputs. The analog inputs, AN32 through AN63, are multiplexed, thus providing flexibility in using any of these analog inputs in addition to the analog inputs, AN0 through AN31. Since AN32 through AN63 are multiplexed, do not use two channels simultaneously, since it may result in erroneous output from the module. These analog inputs are shared with op amp inputs and outputs, comparator inputs and external voltage references. When op amp/comparator functionality is enabled, the analog input that shares that pin is no longer available. The actual number of analog input pins and op amps depends on the specific device.

A block diagram of the ADC module with connection options is shown in Figure 24-1. Figure 24-2 shows a block diagram of the ADC conversion clock period.

FIGURE 24-1: ADCx MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

This diagram depicts all of the available ADC connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

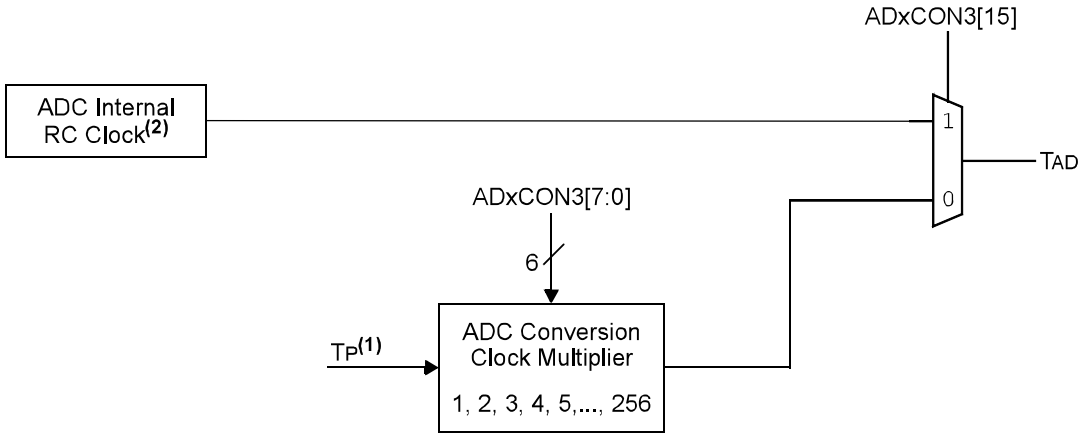
The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CH0Nx, CH123Sx and CH123Nx.



Note 1: Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
2: When ADDMAEN (ADxCON4[8]) = 0, ADC1BUF0-ADC1BUFF are used.
3: When ADDMAEN (ADxCON4[8]) = 1 enabling DMA, only ADC1BUF0 is used.

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FIGURE 24-2: ADCx CONVERSION CLOCK PERIOD BLOCK DIAGRAM



Note 1: TP = 1/FP.

2: Refer to the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

24.2 ADC Helpful Tips

1. The SMPIx control bits in the ADxCON2 registers:
   a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
   b) When the CSCNA bit in the ADxCON2 register is set to '1', this determines when the ADC analog scan channel list, defined in the ADxCSSL/ADxCSSH registers, starts over from the beginning.
   c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
   d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using the DMA peripheral.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1.c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only 1 ADC result buffer (i.e., ADCxBUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (ADxCON1[0]) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (ADxCON1[1]), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUX A selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. For configuration examples, refer to **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

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24.3 ADC Control Registers

REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	HC/HS/R/W-0	HC/HS/R/C-0
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE(1)
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	HC = Hardware Clearable bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADON:** ADCx Operating Mode bit
1 = ADCx module is operating
0 = ADCx is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** ADCx Stop in Idle Mode bit
1 = Discontinues module operation when the device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ADDMABM:** ADCx DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather mode address to the DMA channel based on the index of the analog input and the size of the DMA buffer

bit 11 **Unimplemented:** Read as '0'

bit 10 **AD12B:** ADCx 10-Bit or 12-Bit Operation Mode bit
1 = 12-bit, 1-channel ADC operation
0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM[1:0]:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d[9])
10 = Fractional (DOUT = dddd dddd dd00 0000)
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d[9])
00 = Integer (DOUT = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d[11])
10 = Fractional (DOUT = dddd dddd dddd 0000)
01 = Signed integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d[11])
00 = Integer (DOUT = 0000 dddd dddd dddd)

Note 1: Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

REGISTER 24-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)

bit 7-5 **SSRC[2:0]:** Sample Clock Source Select bits

If SSRCG = 1:

111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = Reserved
010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion
001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion
000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion

If SSRCG = 0:

111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = CTMU ends sampling and starts conversion
101 = Reserved
100 = Timer5 compare ends sampling and starts conversion
011 = PWM primary Special Event Trigger ends sampling and starts conversion
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on the INT0 pin ends sampling and starts conversion
000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)

bit 4 **SSRCG:** Sample Trigger Source Group bit

See SSRC[2:0] for details.

bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS[1:0] = 01 or 1x)

In 12-Bit Mode (AD12B = 1), SIMSAM is Unimplemented and is Read as '0':

1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS[1:0] = 1x) or samples CH0 and CH1 simultaneously (when CHPS[1:0] = 01)
0 = Samples multiple channels individually in sequence

bit 2 **ASAM:** ADCx Sample Auto-Start bit

1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADCx Sample Enable bit

1 = ADCx Sample-and-Hold amplifiers are sampling
0 = ADCx Sample-and-Hold amplifiers are holding

If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC[2:0] = 000, software can write '0' to end sampling and start conversion. If SSRC[2:0] ≠ 000, automatically cleared by hardware to end sampling and start conversion.

bit 0 **DONE:** ADCx Conversion Status bit(1)

1 = ADCx conversion cycle is completed.
0 = ADCx conversion has not started or is in progress

Automatically set by hardware when conversion is complete. Software can write '0' to clear DONE bit status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

Note 1: Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

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REGISTER 24-2: ADxCON2: ADCx CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
VCFG2(1)	VCFG1(1)	VCFG0(1)	—	—	CSCNA	CHPS1	CHPS0
bit 15							bit 8

R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BUFS	SMPI4	SMPI3	SMPI2	SMPI1	SMPI0	BUFM	ALTS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **VCFG[2:0]:** Converter Voltage Reference Configuration bits(1)

Value	VREFH	VREFL
xxx	AVDD	AVSS

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit
1 = Scans inputs for CH0+ during Sample MUX A
0 = Does not scan inputs

bit 9-8 **CHPS[1:0]:** Channel Select bits
In 12-Bit Mode (AD21B = 1), CHPS[1:0] bits are Unimplemented and are Read as '0':
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)
1 = ADCx is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
0 = ADCx is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI[4:0]:** Increment Rate bits
When ADDMAEN = 0:
x1111 = Generates interrupt after completion of every 16th sample/conversion operation
x1110 = Generates interrupt after completion of every 15th sample/conversion operation
•
•
•
x0001 = Generates interrupt after completion of every 2nd sample/conversion operation
x0000 = Generates interrupt after completion of every sample/conversion operation
When ADDMAEN = 1:
11111 = Increments the DMA address after completion of every 32nd sample/conversion operation
11110 = Increments the DMA address after completion of every 31st sample/conversion operation
•
•
•
00001 = Increments the DMA address after completion of every 2nd sample/conversion operation
00000 = Increments the DMA address after completion of every sample/conversion operation

Note 1: The ADCx VREFH Input is connected to AVDD and the VREFL input is connected to AVSS.

REGISTER 24-2: ADxCON2: ADCx CONTROL REGISTER 2 (CONTINUED)

bit 1 **BUFM:** Buffer Fill Mode Select bit
1 = Starts buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on the next interrupt
0 = Always starts filling the buffer from the Start address

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample MUX A on the first sample and Sample MUX B on the next sample
0 = Always uses channel input selects for Sample MUX A

Note 1: The ADCx VREFH Input is connected to AVDD and the VREFL input is connected to AVSS.

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REGISTER 24-3: ADxCON3: ADCx CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4(1)	SAMC3(1)	SAMC2(1)	SAMC1(1)	SAMC0(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS7(2)	ADCS6(2)	ADCS5(2)	ADCS4(2)	ADCS3(2)	ADCS2(2)	ADCS1(2)	ADCS0(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ADRC:** ADCx Conversion Clock Source bit
1 = ADCx internal RC clock
0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC[4:0]:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS[7:0]:** ADCx Conversion Clock Select bits(2)
11111111 = TP • (ADCS[7:0] + 1) = TP • 256 = TAD
•
•
•
00000010 = TP • (ADCS[7:0] + 1) = TP • 3 = TAD
00000001 = TP • (ADCS[7:0] + 1) = TP • 2 = TAD
00000000 = TP • (ADCS[7:0] + 1) = TP • 1 = TAD

Note 1: These bits are only used if SSRC[2:0] (ADxCON1[7:5]) = 111 and SSRCG (ADxCON1[4]) = 0.
2: These bits are not used if ADRC (ADxCON3[15]) = 1.

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REGISTER 24-4: ADxCON4: ADCx CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	ADDMAEN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	DMABL2	DMABL1	DMABL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **ADDMAEN:** ADCx DMA Enable bit
1 = Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA
0 = Conversion results are stored in the ADC1BUF0 through ADC1BUFF registers; DMA will not be used

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **DMABL[2:0]:** Selects Number of DMA Buffer Locations per Analog Input bits
111 = Allocates 128 words of buffer to each analog input
110 = Allocates 64 words of buffer to each analog input
101 = Allocates 32 words of buffer to each analog input
100 = Allocates 16 words of buffer to each analog input
011 = Allocates 8 words of buffer to each analog input
010 = Allocates 4 words of buffer to each analog input
001 = Allocates 2 words of buffer to each analog input
000 = Allocates 1 word of buffer to each analog input

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REGISTER 24-5: ADxCHS123: ADCx INPUT CHANNELS 1, 2, 3 SELECT REGISTER

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CH123SB2	CH123SB1	CH123NB1	CH123NB0	CH123SB0
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	CH123SA2	CH123SA1	CH123NA1	CH123NA0	CH123SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-11 **CH123SB[2:1]:** Channels 1, 2, 3 Positive Input Select for Sample B bits
- 1xx = CH1 positive input is AN0 (Op Amp 2), CH2 positive input is AN25 (Op Amp 5), CH3 positive input is AN6 (Op Amp 3)
- 011 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN25 (Op Amp 5)
- 010 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN6 (Op Amp 3)
- 001 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5
- 000 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

bit 10-9 **CH123NB[1:0]:** Channels 1, 2, 3 Negative Input Select for Sample B bits
- 11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11
- 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8
- 0x = CH1, CH2, CH3 negative inputs are VREFL

bit 8 **CH123SB0:** Channels 1, 2, 3 Positive Input Select for Sample B bit

See bits[12:11] for bit selections.

bit 7-5 **Unimplemented:** Read as '0'

bit 4-3 **CH123SA[2:1]:** Channels 1, 2, 3 Positive Input Select for Sample A bits
- 1xx = CH1 positive input is AN0 (Op Amp 2), CH2 positive input is AN25 (Op Amp 5), CH3 positive input is AN6 (Op Amp 3)
- 011 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN25 (Op Amp 5)
- 010 = CH1 positive input is AN3 (Op Amp 1), CH2 positive input is AN0 (Op Amp 2), CH3 positive input is AN6 (Op Amp 3)
- 001 = CH1 positive input is AN3, CH2 positive input is AN4, CH3 positive input is AN5
- 000 = CH1 positive input is AN0, CH2 positive input is AN1, CH3 positive input is AN2

bit 2-1 **CH123NA[1:0]:** Channels 1, 2, 3 Negative Input Select for Sample A bits
- 11 = CH1 negative input is AN9, CH2 negative input is AN10, CH3 negative input is AN11
- 10 = CH1 negative input is AN6, CH2 negative input is AN7, CH3 negative input is AN8
- 0x = CH1, CH2, CH3 negative inputs are VREFL

bit 0 **CH123SA0:** Channels 1, 2, 3 Positive Input Select for Sample A bit

See bits[4:3] for bit selections.

REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	CH0SB5(1,3)	CH0SB4(1,3)	CH0SB3(1,3)	CH0SB2(1,3)	CH0SB1(1,3)	CH0SB0(1,3)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	CH0SA5(1,3)	CH0SA4(1,3)	CH0SA3(1,3)	CH0SA2(1,3)	CH0SA1(1,3)	CH0SA0(1,3)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUX B bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **CH0SB[5:0]:** Channel 0 Positive Input Select for Sample MUX B bits(1,3)
111111 = Channel 0 positive input is AN63 (unconnected)
111110 = Channel 0 positive input is AN62 (CTMU temperature diode)
111101 = Channel 0 positive input is AN61 (internal band gap voltage)
•
•
•
011111 = Channel 0 positive input is AN31
011110 = Channel 0 positive input is AN30
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 (Op Amp 2)(2)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUX A bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6 **Unimplemented:** Read as '0'

Note 1: AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: If the op amp is selected (OPAEN bit (CMxCON[10]) = 1), the OAx input is used; otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

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REGISTER 24-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)

bit 5-0 **CH0SA[5:0]:** Channel 0 Positive Input Select for Sample MUX A bits(1,3)

111111 = Channel 0 positive input is AN63 (unconnected)
111110 = Channel 0 positive input is AN62 (CTMU temperature diode)
111101 = Channel 0 positive input is AN61 (internal band gap voltage)
•
•
•
011111 = Channel 0 positive input is AN31
011110 = Channel 0 positive input is AN30
•
•
•
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 (Op Amp 2)(2)

Note 1: AN0 to AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 24-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: If the op amp is selected (OPAEN bit (CMxCON[10]) = 1), the OAx input is used; otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

REGISTER 24-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH(2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	CSS29	CSS28	CSS27	CSS26(1)	CSS25(1)	CSS24(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	CSS19	CSS18	CSS17	CSS16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSS31:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 14 **CSS30:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 13 **CSS29:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 12 **CSS28:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 11 **CSS27:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 10 **CSS26:** ADCx Input Scan Selection bit(1)
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 9 **CSS25:** ADCx Input Scan Selection bit(1)
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 8 **CSS24:** ADCx Input Scan Selection bit(1)
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **CSS19:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 2 **CSS18:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1: If the op amp is selected (OPAEN bit (CMxCON[10]) = 1), the OAx input is used; otherwise, the ANx input is used.

2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

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REGISTER 24-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH(2) (CONTINUED)

bit 1 **CSS17:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 0 **CSS16:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1: If the op amp is selected (OPAEN bit (CMxCON[10]) = 1), the OAx input is used; otherwise, the ANx input is used.

2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

REGISTER 24-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS[15:8]							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CSS[15:0]:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

2: CSSx = ANx, where x = 0-5.

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25.0 OP AMP/COMPARATOR MODULE

Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Op Amp/Comparator"** (www.microchip.com/DS70000357) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

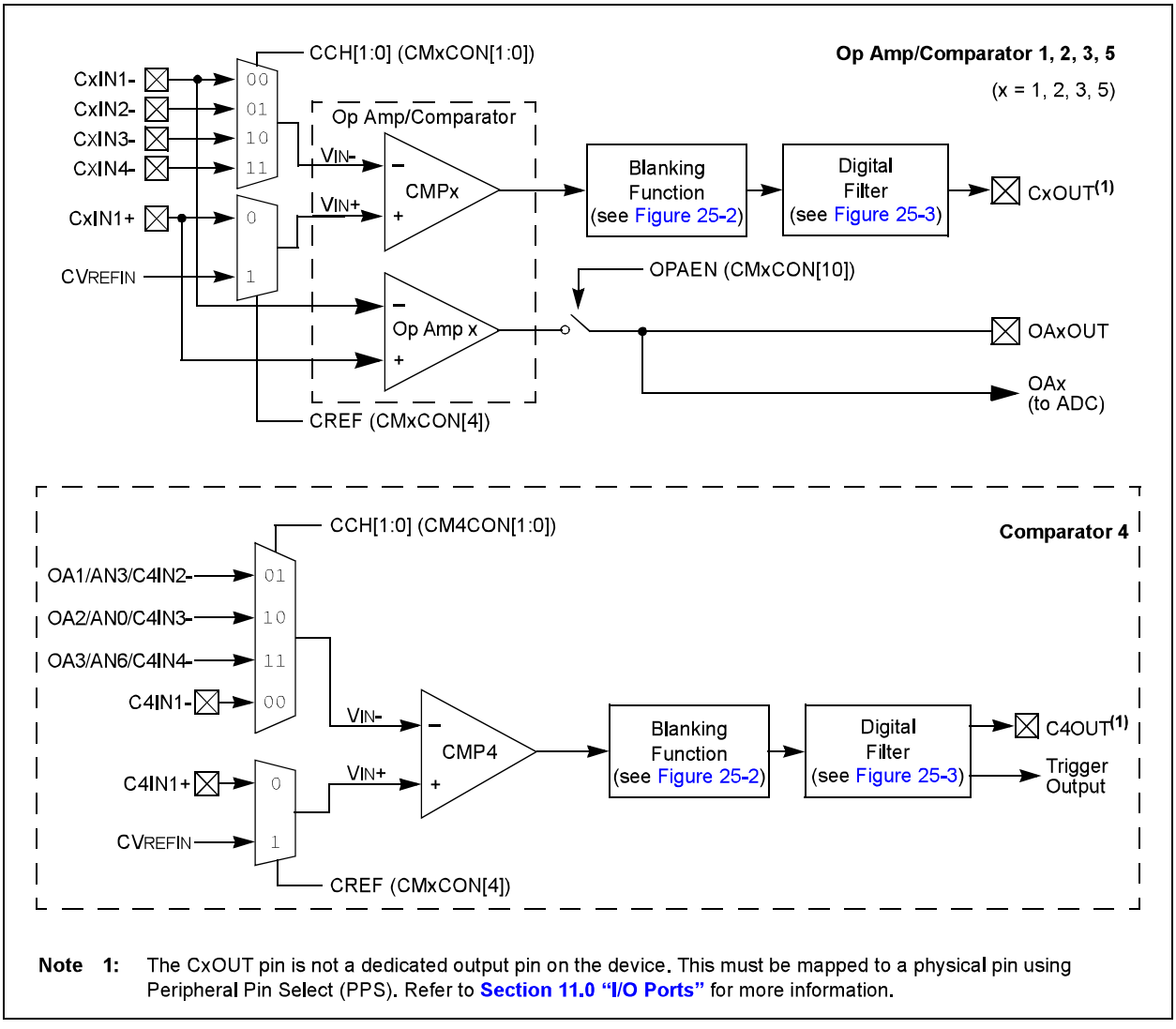
The dsPIC33EVXXXGM00X/10X family devices contain up to five comparators that can be configured in various ways. CMP1, CMP2, CMP3 and CMP5 also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

The following options allow users to:

- Select the Edge for Trigger and Interrupt Generation
- Configure the Comparator Voltage Reference
- Configure Output Blanking and Masking
- Configure as a Comparator or Op Amp (CMP1, CMP2, CMP3 and CMP5 only)

Note: Not all op amp/comparator input/output connections are available on all devices. See the **"Pin Diagrams"** section for available connections.

FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM



Note 1: The CxOUT pin is not a dedicated output pin on the device. This must be mapped to a physical pin using Peripheral Pin Select (PPS). Refer to **Section 11.0 "I/O Ports"** for more information.

Figure 25-2, shows the user-programmable blanking function block diagram.

FIGURE 25-2: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

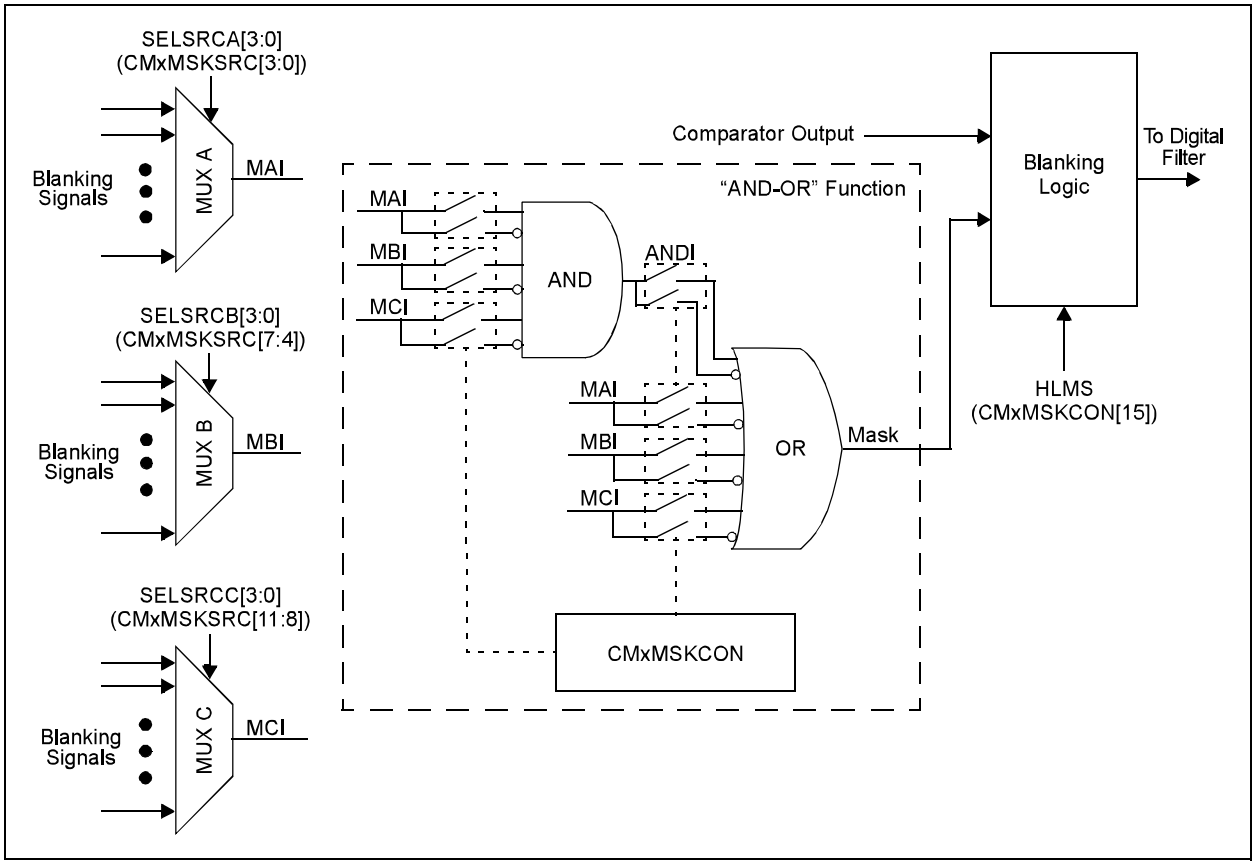
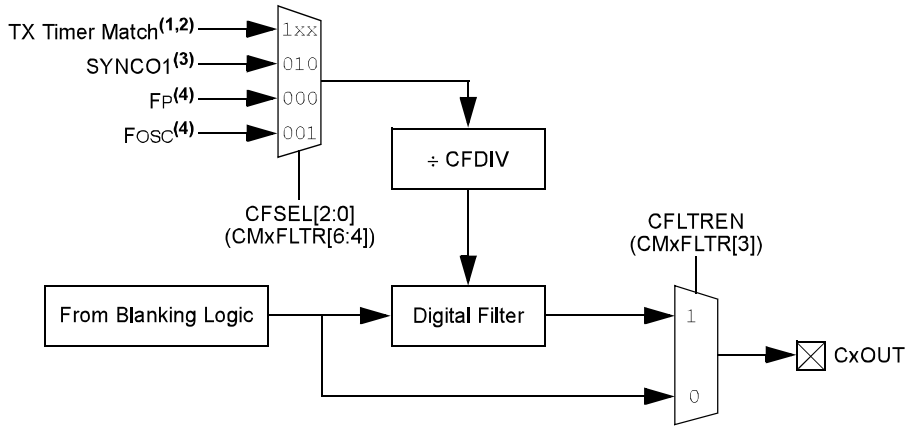


Figure 25-3, shows the digital filter interconnect block diagram.

FIGURE 25-3: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



Note 1: See the Type C Timer Block Diagram (Figure 13-2).
2: See the Type B Timer Block Diagram (Figure 13-1).
3: See the PWMx Module Register Interconnect Diagram (Figure 17-2).
4: See the Oscillator System Diagram (Figure 9-1).

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25.1 Op Amp/Comparator Control Registers

REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER

R/W-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
PSIDL	—	—	C5EVT(1)	C4EVT(1)	C3EVT(1)	C2EVT(1)	C1EVT(1)
bit 15							bit 8

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	C5OUT(2)	C4OUT(2)	C3OUT(2)	C2OUT(2)	C1OUT(2)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PSIDL:** Op Amp/Comparator Stop in Idle Mode bit
1 = Discontinues operation of all op amps/comparators when device enters Idle mode
0 = Continues operation of all op amps/comparators in Idle mode

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **C[5:1]EVT:** Op Amp/Comparator 1-5 Event Status bits(1)
1 = Op amp/comparator event occurred
0 = Op amp/comparator event did not occur

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **C[5:1]OUT:** Op Amp/Comparator 1-5 Output Status bits(2)
When CPOL = 0:
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1:
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

Note 1: Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON[9].

2: Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON[8].

REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5)

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R-0
CON	COE	CPOL	—	—	OPAEN(2)	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(3)	EVPOL0(3)	—	CREF(1)	—	—	CCH1(1)	CCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Op Amp/Comparator x Enable bit
1 = Op Amp/Comparator x is enabled
0 = Op Amp/Comparator x is disabled

bit 14 **COE:** Comparator x Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator x Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPAEN:** Op Amp x Enable bit(2)
1 = Op Amp x is enabled
0 = Op Amp x is disabled

bit 9 **CEVT:** Comparator x Event bit
1 = Comparator event, according to EVPOL[1:0] settings, occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator x Output bit
When CPOL = 0 (non-inverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

Note 1: Inputs that are selected and not available will be tied to Vss. See the **"Pin Diagrams"** section for available inputs for each package.

2: The op amp and the comparator can be used simultaneously in these devices. The OPAEN bit only enables the op amp while the comparator is still functional.

3: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL[1:0] (CMxCON[7:6]) = 10 or 01), the Comparator x Event bit, CEVT (CMxCON[9]), and the Comparator Interrupt Flag, CMPIF (IFS1[2]), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1[2]).

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REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5) (CONTINUED)

bit 7-6 **EVPOL[1:0]:** Trigger/Event/Interrupt Polarity Select bits(3)
- 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
- 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    Low-to-high transition of the comparator output.
  - If CPOL = 0 (non-inverted polarity):
    High-to-low transition of the comparator output.
- 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    High-to-low transition of the comparator output.
  - If CPOL = 0 (non-inverted polarity):
    Low-to-high transition of the comparator output.
- 00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator x Reference Select bit (V_{IN+} input)(1)
- 1 = V_{IN+} input connects to the internal CV_{REFIN} voltage
- 0 = V_{IN+} input connects to the CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH[1:0]:** Op Amp/Comparator x Channel Select bits(1)
- 11 = Inverting input of op amp/comparator connects to the CxIN4- pin
- 10 = Inverting input of op amp/comparator connects to the CxIN3- pin
- 01 = Inverting input of op amp/comparator connects to the CxIN2- pin
- 00 = Inverting input of op amp/comparator connects to the CxIN1- pin

Note 1: Inputs that are selected and not available will be tied to Vss. See the **"Pin Diagrams"** section for available inputs for each package.

2: The op amp and the comparator can be used simultaneously in these devices. The OPAEN bit only enables the op amp while the comparator is still functional.

3: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL[1:0] (CMxCON[7:6]) = 10 or 01), the Comparator x Event bit, CEVT (CMxCON[9]), and the Comparator Interrupt Flag, CMPIF (IFS1[2]), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1[2]).

REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0	R-0
CON	COE	CPOL	—	—	—	CEVT	COUT
bit 15							bit 8

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EVPOL1(2)	EVPOL0(2)	—	CREF(1)	—	—	CCH1(1)	CCH0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CON:** Op Amp/Comparator 4 Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator 4 Output Enable bit
1 = Comparator output is present on the C4OUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator 4 Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator 4 Event bit
1 = Comparator event, according to EVPOL[1:0] settings, occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator 4 Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

Note 1: Inputs that are selected and not available will be tied to Vss. See the **"Pin Diagrams"** section for available inputs for each package.

2: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL[1:0] (CMxCON[7:6]) = 10 or 01), the comparator Event bit, CEVT (CMxCON[9]), and the Comparator Combined Interrupt Flag, CMPIF (IFS1[2]), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1[2]).

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REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)

bit 7-6 **EVPOL[1:0]:** Trigger/Event/Interrupt Polarity Select bits(2)

11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator 4 Reference Select bit (V_{IN+} input)(1)

1 = V_{IN+} input connects to the internal CV_{REFIN} voltage
0 = V_{IN+} input connects to the C4IN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH[1:0]:** Comparator 4 Channel Select bits(1)

11 = V_{IN-} input of comparator connects to the C4IN4- pin
10 = V_{IN-} input of comparator connects to the C4IN3- pin
01 = V_{IN-} input of comparator connects to the C4IN2- pin
00 = V_{IN-} input of comparator connects to the C4IN1- pin

Note 1: Inputs that are selected and not available will be tied to V_{SS}. See the **"Pin Diagrams"** section for available inputs for each package.

2: After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL[1:0] (CMxCON[7:6]) = 10 or 01), the comparator Event bit, CEVT (CMxCON[9]), and the Comparator Combined Interrupt Flag, CMPIF (IFS1[2]), must be cleared before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1[2]).

REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	RW-0
—	—	—	—	SELSRCC3	SELSRCC2	SELSRCC1	SELSRCC0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SELSRCB3	SELSRCB2	SELSRCB1	SELSRCB0	SELSRCA3	SELSRCA2	SELSRCA1	SELSRCA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SELSRCC[3:0]:** Mask C Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB[3:0]:** Mask B Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

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REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)

bit 3-0 **SELSRCA[3:0]:** Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = Reserved
1100 = Reserved
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **HLMS:** High or Low-Level Masking Select bit
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

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REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)

bit 3 **ABEN:** AND Gate B Input Enable bit
1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

bit 2 **ABNEN:** AND Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1 **AAEN:** AND Gate A Input Enable bit
1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0 **AANEN:** AND Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate

REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CFSEL2	CFSEL1	CFSEL0	CFLTREN	CFDIV2	CFDIV1	CFDIV0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL[2:0]:** Comparator x Filter Input Clock Select bits
111 = T5CLK(1)
110 = T4CLK(2)
101 = T3CLK(1)
100 = T2CLK(2)
011 = Reserved
010 = SYNCO1(3)
001 = Fosc(4)
000 = FP(4)

bit 3 **CFLTREN:** Comparator x Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 2-0 **CFDIV[2:0]:** Comparator x Filter Clock Divide Select bits
111 = Clock divide 1:128
110 = Clock divide 1:64
101 = Clock divide 1:32
100 = Clock divide 1:16
011 = Clock divide 1:8
010 = Clock divide 1:4
001 = Clock divide 1:2
000 = Clock divide 1:1

Note 1: See the Type C Timer Block Diagram (Figure 13-2).
2: See the Type B Timer Block Diagram (Figure 13-1).
3: See the High-Speed PWMx Module Register Interconnection Diagram (Figure 17-2).
4: See the Oscillator System Diagram (Figure 9-1).

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26.0 COMPARATOR VOLTAGE REFERENCE

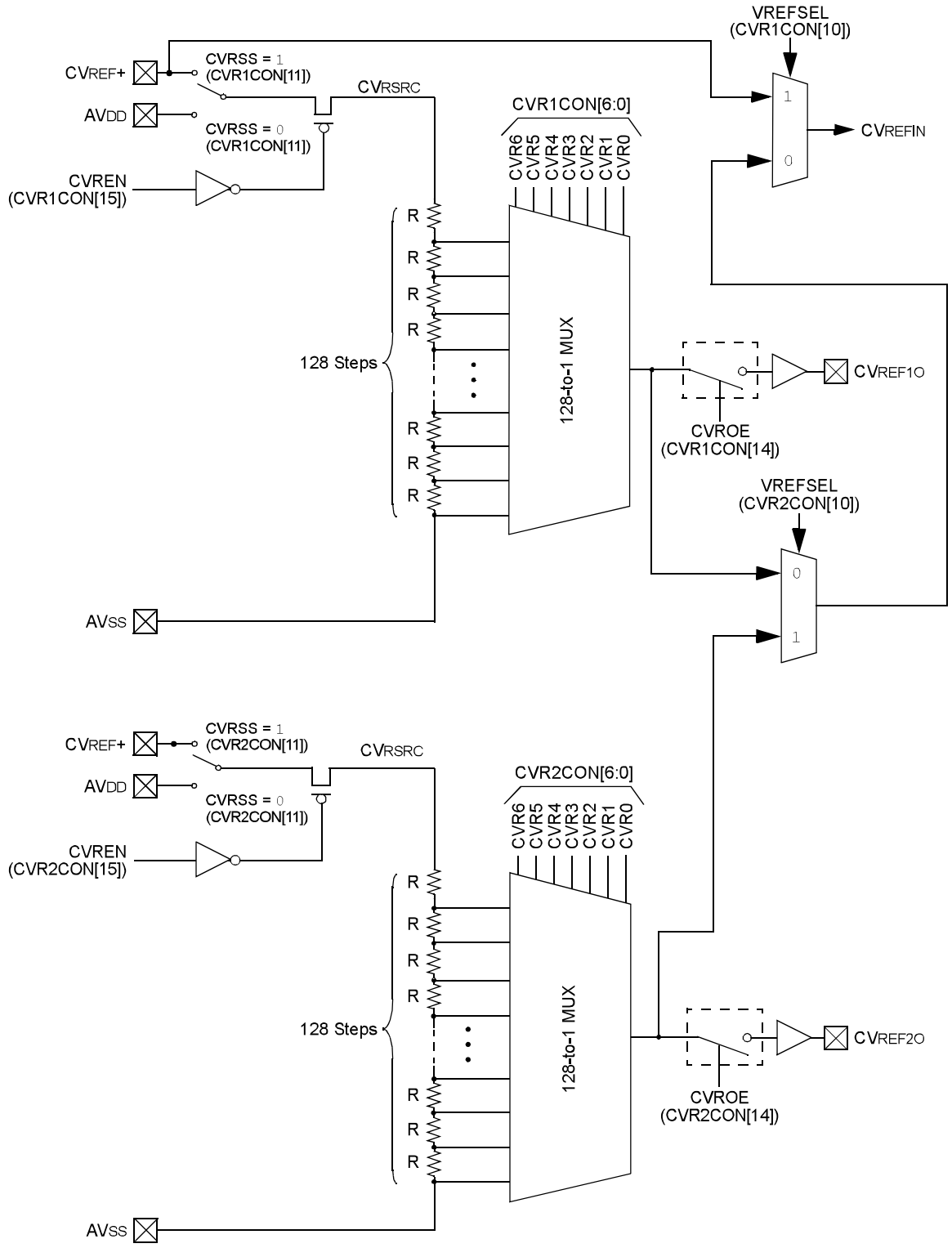
Note 1: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Op Amp/Comparator"** (www.microchip.com/DS70000357) in the *"dsPIC33/PIC24 Family Reference Manual"*.

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

26.1 Configuring the Comparator Voltage Reference

The comparator voltage reference module is controlled through the CVRxCON registers (Register 26-1 and Register 26-2). The comparator voltage reference provides a range of output voltages with 128 distinct levels. The comparator reference supply voltage can come from either VDD and VSS, or the external CVREF+ and AVSS pins. The voltage source is selected by the CVRSS bit (CVRxCON[11]). The settling time of the comparator voltage reference must be considered when changing the CVREF output.

FIGURE 26-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



Note 1: CVREF2O and CVROE (CVR2CON[14]) are not available on the 28-pin and 36-pin devices.

2: Set the respective TRISx bit to '1' to get the CVREF1O/CVREF2O output voltage on the pins.

3: CVREF+ is not available on the 28-pin or 36-pin package devices.

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26.2 Comparator Voltage Reference Registers

REGISTER 26-1: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE	—	—	CVRSS	VREFSEL	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF1O Pin) bit
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from the CVREF1O pin

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = CVREFIN = CVREF+
0 = CVREFIN is generated by the resistor network

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR[6:0]:** Comparator Voltage Reference Value Selection bits
1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

REGISTER 26-2: CVR2CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 2

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
CVREN	CVROE(1)	—	—	CVRSS	VREFSEL	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVR6	CVR5	CVR4	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 14 **CVROE:** Comparator Voltage Reference Output Enable (CVREF2O Pin) bit(1)
1 = Voltage level is output on the CVREF2O pin
0 = Voltage level is disconnected from the CVREF2O pin

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator reference source, CVRSRC = CVREF+ – AVSS
0 = Comparator reference source, CVRSRC = AVDD – AVSS

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = Comparator Reference Source 2 (CVR2) provides inverting input voltage when VREFSEL (CVR1CON[10]) = 0
0 = Comparator Reference Source 1 (CVR1) provides inverting input voltage when VREFSEL (CVR1CON[10]) = 0

bit 9-7 **Unimplemented:** Read as '0'

bit 6-0 **CVR[6:0]:** Comparator Voltage Reference Value Selection bits
1111111 = 127/128 x VREF input voltage
•
•
•
0000000 = 0.0 volts

Note 1: CVROE (CVR2CON[14]) is not available on the 28-pin and 36-pin devices.

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27.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip website (www.microchip.com).

The dsPIC33EVXXXGM00X/10X family devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

27.1 Configuration Bits

In dsPIC33EVXXXGM00X/10X family devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data are stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data are automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data are reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to ensure that program code is not stored in this address when the code is compiled.

The upper two bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

TABLE 27-1: CONFIGURATION WORD REGISTER MAP

File Name	Address	Device Memory Size (Kbytes)	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSEC	005780	32	—	AIVTDIS	—	—	—	CSS2	CSS1	CSS0	CWRP	GSS1	GSS0	GWRP	—	BSEN	BSS1	BSS0	BWRP
	00AB80	64																	
	015780	128																	
	02AB80	256																	
FBSLIM	005790	32	—	—	—	—	BSLIM[12:0]												
	00AB90	64																	
	015790	128																	
	02AB90	256																	
Reserved	005794	32	—	Reserved(1)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	00AB94	64																	
	015794	128																	
	02AB94	256																	
FOSCSEL	005798	32	—	—	—	—	—	—	—	—	—	$\overline{\text{IESO}}$	—	—	—	—	FNOSC2	FNOSC1	FNOSC0
	00AB98	64																	
	015798	128																	
	02AB98	256																	
FOSC	00579C	32	—	—	—	—	—	—	—	—	PLLKEN	FCKSM1	FCKSM0	IOL1WAY	—	—	OSCIOFNC	POSCMD1	POSCMD0
	00AB9C	64																	
	01579C	128																	
	02AB9C	256																	
FWDT	0057A0	32	—	—	—	—	—	—	—	WDTWIN1	WDTWIN0	WINDIS	FWDTEN1	FWDTEN0	WDTPRE	WDTPS3	WDTPS2	WDTPS1	WDTPS0
	00ABA0	64																	
	0157A0	128																	
	02ABA0	256																	
FPOR	0057A4	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BOREN
	00ABA4	64																	
	0157A4	128																	
	02ABA4	256																	
FICD	0057A8	32	—	—	—	—	—	—	—	—	—	Reserved(2)	—	—	—	—	—	ICS1	ICS0
	00ABA8	64																	
	0157A8	128																	
	02ABA8	256																	

Legend: — = unimplemented, read as '1'.
Note 1: This bit is reserved and must be programmed as '0'.
2: This bit is reserved and must be programmed as '1'.

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TABLE 27-1: CONFIGURATION WORD REGISTER MAP (CONTINUED)

File Name	Address	Device Memory Size (Kbytes)	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FDMTINTVL	0057AC	32	—	DMTIVT[15:0]															
	00ABAC	64																	
	0157AC	128																	
	02ABAC	256																	
FDMTINTVH	0057B0	32	—	DMTIVT[31:16]															
	00ABB0	64																	
	0157B0	128																	
	02ABB0	256																	
FDMTCNTL	0057B4	32	—	DMTCNT[15:0]															
	00ABB4	64																	
	0157B4	128																	
	02ABB4	256																	
FDMTCNTH	0057B8	32	—	DMTCNT[31:16]															
	00AB8	64																	
	0157B8	128																	
	02ABB8	256																	
FDMT	0057BC	32	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMTEN
	00ABBC	64																	
	0157BC	128																	
	02ABBC	256																	
FDEVOPT	0057C0	32	—	—	—	—	—	—	—	—	—	—	—	—	—	ALTI2C1	Reserved(2)	—	PWMLOCK
	00ABC0	64																	
	0157C0	128																	
	02ABC0	256																	
FALTREG	0057C4	32	—	—	—	—	—	—	—	—	—	—	CTXT2[2:0]			—	CTXT1[2:0]		
	00ABC4	64																	
	0157C4	128																	
	02ABC4	256																	

Legend: — = unimplemented, read as '1'.
Note 1: This bit is reserved and must be programmed as '0'.
2: This bit is reserved and must be programmed as '1'.

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TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION

Bit Field	Register	Description
BWRP	FSEC	Boot Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
BSS[1:0]	FSEC	Boot Segment Code Flash Protection Level bits 11 = No protection (other than BWRP write protection) 10 = Standard security 0x = High security
BSEN	FSEC	Boot Segment Control bit 1 = No Boot Segment 0 = Boot Segment size is determined by BSLIM[12:0]
GWRP	FSEC	General Segment Write-Protect bit 1 = User program memory is not write-protected 0 = User program memory is write-protected
GSS[1:0]	FSEC	General Segment Code Flash Protection Level bits 11 = No protection (other than GWRP write protection) 10 = Standard security 0x = High security
CWRP	FSEC	Configuration Segment Write-Protect bit 1 = Configuration Segment is not write-protected 0 = Configuration Segment is write-protected
CSS[2:0]	FSEC	Configuration Segment Code Flash Protection Level bits 111 = No protection (other than CWRP write protection) 110 = Standard security 10x = Enhanced security 0xx = High security
AIVTDIS	FSEC	Alternate Interrupt Vector Table Disable bit 1 = Disables AIVT 0 = Enables AIVT
BSLIM[12:0]	FBSLIM	Boot Segment Code Flash Page Address Limit bits Contains the page address of the first active General Segment page. The value to be programmed is the inverted page address, such that programming additional '0's can only increase the Boot Segment size. For example, 0x1FFD = 2 pages or 1024 instruction words.
FNOSC[2:0]	FOSCSEL	Initial Oscillator Source Selection bits 111 = Internal Fast RC (FRC) Oscillator with Postscaler 110 = Internal Fast RC (FRC) Oscillator with Divide-by-16 101 = LPRC Oscillator 100 = Reserved 011 = Primary (XT, HS, EC) Oscillator with PLL 010 = Primary (XT, HS, EC) Oscillator 001 = Internal Fast RC (FRC) Oscillator with PLL 000 = FRC Oscillator
$\overline{\text{IESO}}$	FOSCSEL	Two-Speed Oscillator Start-up Enable bit 1 = Starts up device with FRC, then automatically switches to the user-selected oscillator source when ready 0 = Starts up device with user-selected oscillator source
POSCMD[1:0]	FOSC	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode

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TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	Description
OSCIOFNC	FOSC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is the general purpose digital I/O pin
IOL1WAY	FOSC	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
FCKSM[1:0]	FOSC	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
PLLKEN	FOSC	PLL Lock Wait Enable bit 1 = Clock switches to the PLL source; will wait until the PLL lock signal is valid 0 = Clock switch will not wait for PLL lock
WDTPS[3:0]	FWDT	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
WDTPRE	FWDT	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
FWDTEN[1:0]	FWDT	Watchdog Timer Enable bits 11 = WDT is enabled in hardware 10 = WDT is controlled through the SWDTEN bit 01 = WDT is enabled only while device is active and disabled in Sleep; the SWDTEN bit is disabled 00 = WDT and the SWDTEN bit are disabled
WINDIS	FWDT	Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode
WDTWIN[1:0]	FWDT	Watchdog Timer Window Select bits 11 = WDT window is 25% of WDT period 10 = WDT window is 37.5% of WDT period 01 = WDT window is 50% of WDT period 00 = WDT window is 75% of WDT period
BOREN	FPOR	Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled
ICS[1:0]	FICD	ICD Communication Channel Select bits 11 = Communicates on PGEC1 and PGED1 10 = Communicates on PGEC2 and PGED2 01 = Communicates on PGEC3 and PGED3 00 = Reserved, do not use
DMTIVT[15:0]	FDMTINTVL	Lower 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits
DMTIVT[31:16]	FDMTINTVH	Upper 16 Bits of 32-Bit Field that Configures the DMT Window Interval bits
DMTCNT[15:0]	FDMTCNTL	Lower 16 Bits of 32-Bit Field that Configures the DMT Instruction Count Time-out Value bits

TABLE 27-2: dsPIC33EVXXXGM00X/10X CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Register	Description
DMTCNT[31:16]	FDMCNTH	Upper 16 Bits of 32-Bit Field that Configures the DMT Instruction Count Time-out Value bits
DMTEN	FDMT	Deadman Timer Enable bit 1 = Deadman Timer is enabled and cannot be disabled by software 0 = Deadman Timer is disabled and can be enabled by software
PWMLOCK	FDEVOPT	PWM Lock Enable bit 1 = Certain PWM registers may only be written after a key sequence 0 = PWM registers may be written without a key sequence
ALTI2C1	FDEVOPT	Alternate I^2C Pins for I2C1 bit 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
CTXT1[2:0]	FALTREG	Specifies the Alternate Working Register Set 1 Association with Interrupt Priority Level (IPL) bits 111 = Not assigned 110 = Alternate Register Set 1 is assigned to IPL Level 7 101 = Alternate Register Set 1 is assigned to IPL Level 6 100 = Alternate Register Set 1 is assigned to IPL Level 5 011 = Alternate Register Set 1 is assigned to IPL Level 4 010 = Alternate Register Set 1 is assigned to IPL Level 3 001 = Alternate Register Set 1 is assigned to IPL Level 2 000 = Alternate Register Set 1 is assigned to IPL Level 1
CTXT2[2:0]	FALTREG	Specifies the Alternate Working Register Set 2 Association with Interrupt Priority Level (IPL) bits 111 = Not assigned 110 = Alternate Register Set 2 is assigned to IPL Level 7 101 = Alternate Register Set 2 is assigned to IPL Level 6 100 = Alternate Register Set 2 is assigned to IPL Level 5 011 = Alternate Register Set 2 is assigned to IPL Level 4 010 = Alternate Register Set 2 is assigned to IPL Level 3 001 = Alternate Register Set 2 is assigned to IPL Level 2 000 = Alternate Register Set 2 is assigned to IPL Level 1

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REGISTER 27-1: DEVID: DEVICE ID REGISTER

R	R	R	R	R	R	R	R
DEVID[23:16](1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVID[15:8](1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVID[7:0](1)							
bit 7							bit 0

Legend:	R = Read-Only bit	U = Unimplemented bit

bit 23-0 **DEVID[23:0]:** Device Identifier bits(1)

Note 1: Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for the list of Device ID values.

REGISTER 27-2: DEVREV: DEVICE REVISION REGISTER

R	R	R	R	R	R	R	R
DEVREV[23:16](1)							
bit 23							bit 16

R	R	R	R	R	R	R	R
DEVREV[15:8](1)							
bit 15							bit 8

R	R	R	R	R	R	R	R
DEVREV[7:0](1)							
bit 7							bit 0

Legend:	R = Read-only bit	U = Unimplemented bit

bit 23-0 **DEVREV[23:0]:** Device Revision bits(1)

Note 1: Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for the list of device revision values.

27.2 User OTP Memory

Locations, 800F80h-800FFEh, are a One-Time-Programmable (OTP) memory area. The user OTP words can be used for storing product information, such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

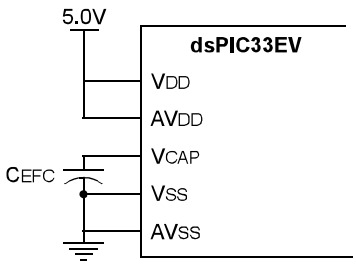
27.3 On-Chip Voltage Regulator

All of the dsPIC33EVXXXGM00X/10X family devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 5.0V. To simplify system design, all devices in the dsPIC33EVXXXGM00X/10X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (see Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5, located in **Section 30.0 "Electrical Characteristics"**.

Note:	It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)



Note 1: These are typical operating voltages. Refer to Table 30-4 located in **Section 30.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

2: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

3: Typical VCAP pin voltage = 1.8V when VDD ≥ VDDMIN.

27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source based on the device Configuration bit values (FNOSC[2:0] and POSCMD[1:0]).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON[5]) is '1'.

Concurrently, the Power-up Timer (PWRT) Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON[1]) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle mode and resets the device should VDD fall below the BOR threshold voltage.

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27.5 Watchdog Timer (WDT)

For dsPIC33EVXXXGM00X/10X family devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out Period (T_{WDT}), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST[3:0] Configuration bits (FWDT[3:0]), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON[3:2]) needs to be cleared in software after the device wakes up.

27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN[1:0] Configuration bits in the FWDT Configuration register. When the FWDTEN[1:0] Configuration bits are set, the WDT is always enabled.

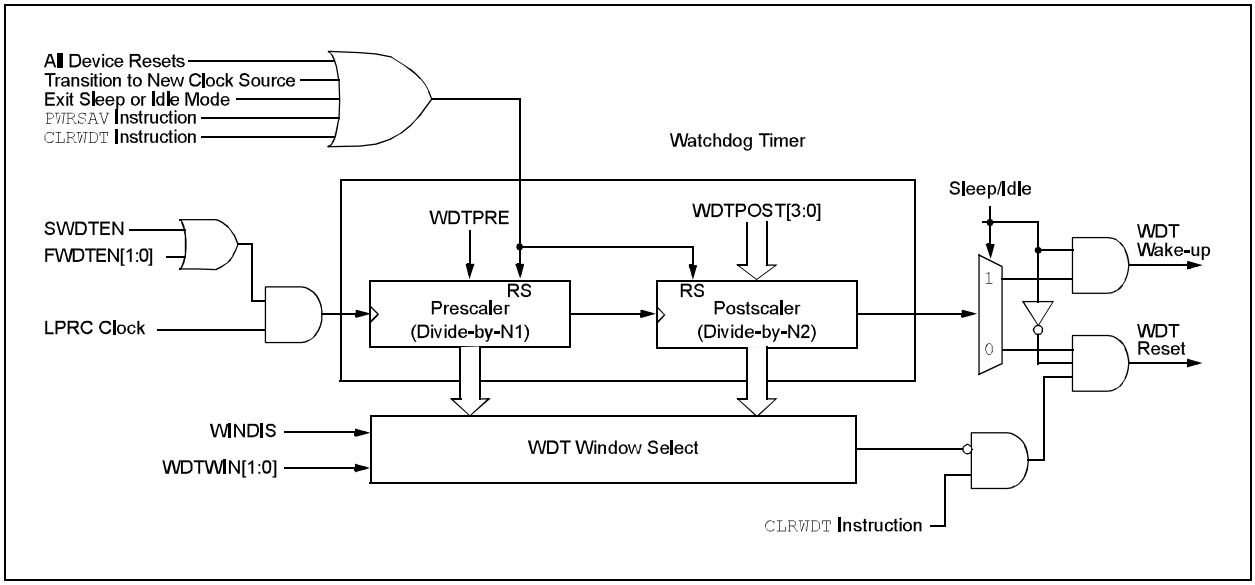
The WDT can be optionally controlled in software when the FWDTENx Configuration bits have been programmed to '00'. The WDT is enabled in software by setting the SWDTEN control bit (RCON[5]). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON[4]), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode enabled by programming the WINDIS bit in the WDT Configuration register (FWDT[7]). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window (WDTWIN[1:0]) select bits.

FIGURE 27-2: WDT BLOCK DIAGRAM



27.6 In-Circuit Serial Programming

The dsPIC33EVXXXGM00X/10X family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to *"dsPIC33EVXXXGM00X/10X Families Flash Programming Specification"* (DS70005137) for details about In-Circuit Serial Programming™ (ICSP™).

Any of the following three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

27.7 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB X IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the following three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, VDD, VSS and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

27.8 Code Protection and CodeGuard™ Security

The dsPIC33EVXXXGM00X/10X family devices offer Intermediate CodeGuard Security that supports General Segment (GS) security, Boot Segment (BS) security and Configuration Segment (CS) security. This feature helps protect individual Intellectual Properties.

Note:	Refer to **"CodeGuard™ Intermediate Security"** (www.microchip.com/DS70005182) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

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28.0 INSTRUCTION SET SUMMARY

Note: This data sheet summarizes the features of the dsPIC33EVXXXGM00X/10X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The dsPIC33EV instruction set is almost identical to that of the dsPIC30F and dsPIC33F.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into following five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the Status Flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have the following three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write-back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the eight MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (DS70000157).

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
[n:m]	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word-addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

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TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)

Field	Description
Wm*Wm	Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7}
Wm*Wn	Multiplicand and Multiplier Working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7}
Wn	One of 16 Working registers ∈ {W0...W15}
Wnd	One of 16 Destination Working registers ∈ {W0...W15}
Wns	One of 16 Source Working registers ∈ {W0...W15}
WREG	W0 (Working register used in file register instructions)
Ws	Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] }
Wso	Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] }
Wx	X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none}
Wxd	X Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}
Wy	Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none}
Wyd	Y Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7}

TABLE 28-2: INSTRUCTION SET OVERVIEW

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
1	ADD	ADD Acc	Add Accumulators	1	1	OA,OB,SA, SB
		ADD f	f = f + WREG	1	1	C,DC,N,OV,Z
		ADD f,WREG	WREG = f + WREG	1	1	C,DC,N,OV,Z
		ADD #lit10,Wn	Wd = lit10 + Wd	1	1	C,DC,N,OV,Z
		ADD Wb,Ws,Wd	Wd = Wb + Ws	1	1	C,DC,N,OV,Z
		ADD Wb,#lit5,Wd	Wd = Wb + lit5	1	1	C,DC,N,OV,Z
		ADD Wso,#Slit4,Acc	16-bit Signed Add to Accumulator	1	1	OA,OB,SA, SB
2	ADDC	ADDC f	f = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC f,WREG	WREG = f + WREG + (C)	1	1	C,DC,N,OV,Z
		ADDC #lit10,Wn	Wd = lit10 + Wd + (C)	1	1	C,DC,N,OV,Z
		ADDC Wb,Ws,Wd	Wd = Wb + Ws + (C)	1	1	C,DC,N,OV,Z
		ADDC Wb,#lit5,Wd	Wd = Wb + lit5 + (C)	1	1	C,DC,N,OV,Z
3	AND	AND f	f = f .AND. WREG	1	1	N,Z
		AND f,WREG	WREG = f .AND. WREG	1	1	N,Z
		AND #lit10,Wn	Wd = lit10 .AND. Wd	1	1	N,Z
		AND Wb,Ws,Wd	Wd = Wb .AND. Ws	1	1	N,Z
		AND Wb,#lit5,Wd	Wd = Wb .AND. lit5	1	1	N,Z
4	ASR	ASR f	f = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR f,WREG	WREG = Arithmetic Right Shift f	1	1	C,N,OV,Z
		ASR Ws,Wd	Wd = Arithmetic Right Shift Ws	1	1	C,N,OV,Z
		ASR Wb,Wns,Wnd	Wnd = Arithmetic Right Shift Wb by Wns	1	1	N,Z
		ASR Wb,#lit5,Wnd	Wnd = Arithmetic Right Shift Wb by lit5	1	1	N,Z
5	BCLR	BCLR f,#bit4	Bit Clear f	1	1	None
		BCLR Ws,#bit4	Bit Clear Ws	1	1	None
6	BRA	BRA C,Expr	Branch if Carry	1	1 (4)	None
		BRA GE,Expr	Branch if Greater Than or Equal	1	1 (4)	None
		BRA GEU,Expr	Branch if Unsigned Greater Than or Equal	1	1 (4)	None
		BRA GT,Expr	Branch if Greater Than	1	1 (4)	None
		BRA GTU,Expr	Branch if Unsigned Greater Than	1	1 (4)	None
		BRA LE,Expr	Branch if Less Than or Equal	1	1 (4)	None
		BRA LEU,Expr	Branch if Unsigned Less Than or Equal	1	1 (4)	None
		BRA LT,Expr	Branch if Less Than	1	1 (4)	None
		BRA LTU,Expr	Branch if Unsigned Less Than	1	1 (4)	None
		BRA N,Expr	Branch if Negative	1	1 (4)	None
		BRA NC,Expr	Branch if Not Carry	1	1 (4)	None
		BRA NN,Expr	Branch if Not Negative	1	1 (4)	None
		BRA NOV,Expr	Branch if Not Overflow	1	1 (4)	None
		BRA NZ,Expr	Branch if Not Zero	1	1 (4)	None
		BRA OA,Expr	Branch if Accumulator A Overflow	1	1 (4)	None
		BRA OB,Expr	Branch if Accumulator B Overflow	1	1 (4)	None
		BRA OV,Expr	Branch if Overflow	1	1 (4)	None
		BRA SA,Expr	Branch if Accumulator A Saturated	1	1 (4)	None
		BRA SB,Expr	Branch if Accumulator B Saturated	1	1 (4)	None
		BRA Expr	Branch Unconditionally	1	4	None
		BRA Z,Expr	Branch if Zero	1	1 (4)	None
		BRA Wn	Computed Branch	1	4	None
7	BSET	BSET f,#bit4	Bit Set f	1	1	None
		BSET Ws,#bit4	Bit Set Ws	1	1	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
8	BSW	BSW.C Ws,Wb	Write C bit to Ws[Wb]	1	1	None
		BSW.Z Ws,Wb	Write Z bit to Ws[Wb]	1	1	None
9	BTG	BTG f,#bit4	Bit Toggle f	1	1	None
		BTG Ws,#bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC f,#bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC Ws,#bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS f,#bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS Ws,#bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST f,#bit4	Bit Test f	1	1	Z
		BTST.C Ws,#bit4	Bit Test Ws to C	1	1	C
		BTST.Z Ws,#bit4	Bit Test Ws to Z	1	1	Z
		BTST.C Ws,Wb	Bit Test Ws[Wb] to C	1	1	C
		BTST.Z Ws,Wb	Bit Test Ws[Wb] to Z	1	1	Z
13	BTSTS	BTSTS f,#bit4	Bit Test then Set f	1	1	Z
		BTSTS.C Ws,#bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z Ws,#bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call Subroutine	2	4	SFA
		CALL Wn	Call Indirect Subroutine	1	4	SFA
		CALL.L Wn	Call Indirect Subroutine (long address)	1	4	SFA
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR Ws	Ws = 0x0000	1	1	None
		CLR Acc,Wx,Wxd,Wy,Wyd,AWB	Clear Accumulator	1	1	OA,OB,SA, SB
16	CLRWDT	CLRWDT	Clear Watchdog Timer	1	1	WDTO,Sleep
17	COM	COM f	$f = \overline{f}$	1	1	N,Z
		COM f,WREG	$WREG = \overline{f}$	1	1	N,Z
		COM Ws,Wd	$Wd = \overline{Ws}$	1	1	N,Z
18	CP	CP f	Compare f with WREG	1	1	C,DC,N,OV,Z
		CP Wb,#lit8	Compare Wb with lit8	1	1	C,DC,N,OV,Z
		CP Wb,Ws	Compare Wb with Ws (Wb – Ws)	1	1	C,DC,N,OV,Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C,DC,N,OV,Z
		CP0 Ws	Compare Ws with 0x0000	1	1	C,DC,N,OV,Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,#lit8	Compare Wb with lit8, with Borrow	1	1	C,DC,N,OV,Z
		CPB Wb,Ws	Compare Wb with Ws, with Borrow (Wb – Ws – $\overline{C}$)	1	1	C,DC,N,OV,Z
21	CPSEQ	CPSEQ Wb,Wn	Compare Wb with Wn, Skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ Wb,Wn,Expr	Compare Wb with Wn, Branch if =	1	1 (5)	None
22	CPSGT	CPSGT Wb,Wn	Compare Wb with Wn, Skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT Wb,Wn,Expr	Compare Wb with Wn, Branch if >	1	1 (5)	None
23	CPSLT	CPSLT Wb,Wn	Compare Wb with Wn, Skip if <	1	1 (2 or 3)	None
	CPBLT	CPBLT Wb,Wn,Expr	Compare Wb with Wn, Branch if <	1	1 (5)	None
24	CPSNE	CPSNE Wb,Wn	Compare Wb with Wn, Skip if ≠	1	1 (2 or 3)	None
	CPBNE	CPBNE Wb,Wn,Expr	Compare Wb with Wn, Branch if ≠	1	1 (5)	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
25	CTXTSWP	CTXTSWP #lit3	Switch CPU Register Context to Context Defined by lit3	1	2	None
		CTXTSWP Wn	Switch CPU Register Context to Context Defined by Wn	1	2	None
26	DAW	DAW Wn	Wn = Decimal Adjust Wn	1	1	C
27	DEC	DEC f	f = f – 1	1	1	C,DC,N,OV,Z
		DEC f,WREG	WREG = f – 1	1	1	C,DC,N,OV,Z
		DEC Ws,Wd	Wd = Ws – 1	1	1	C,DC,N,OV,Z
28	DEC2	DEC2 f	f = f – 2	1	1	C,DC,N,OV,Z
		DEC2 f,WREG	WREG = f – 2	1	1	C,DC,N,OV,Z
		DEC2 Ws,Wd	Wd = Ws – 2	1	1	C,DC,N,OV,Z
29	DISI	DISI #lit14	Disable Interrupts for k Instruction Cycles	1	1	None
30	DIV	DIV.S Wm,Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm,Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm,Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm,Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
31	DIVF	DIVF Wm,Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
32	DO	DO #lit15,Expr	Do Code to PC + Expr, lit15 + 1 Times	2	2	None
		DO Wn,Expr	Do Code to PC + Expr, (Wn) + 1 Times	2	2	None
33	ED	ED Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB, SA,SB,SAB
34	EDAC	EDAC Wm*Wm,Acc,Wx,Wy,Wxd	Euclidean Distance	1	1	OA,OB,OAB, SA,SB,SAB
35	EXCH	EXCH Wns,Wnd	Swap Wns with Wnd	1	1	None
36	FBCL	FBCL Ws,Wnd	Find Bit Change from Left (MSb) Side	1	1	C
37	FF1L	FF1L Ws,Wnd	Find First One from Left (MSb) Side	1	1	C
38	FF1R	FF1R Ws,Wnd	Find First One from Right (LSb) Side	1	1	C
39	GOTO	GOTO Expr	Go to Address	2	4	None
		GOTO Wn	Go to Indirect	1	4	None
		GOTO.L Wn	Go to Indirect (long address)	1	4	None
40	INC	INC f	f = f + 1	1	1	C,DC,N,OV,Z
		INC f,WREG	WREG = f + 1	1	1	C,DC,N,OV,Z
		INC Ws,Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
41	INC2	INC2 f	f = f + 2	1	1	C,DC,N,OV,Z
		INC2 f,WREG	WREG = f + 2	1	1	C,DC,N,OV,Z
		INC2 Ws,Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
42	IOR	IOR f	f = f .IOR. WREG	1	1	N,Z
		IOR f,WREG	WREG = f .IOR. WREG	1	1	N,Z
		IOR #lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N,Z
43	LAC	LAC Wso,#Slit4,Acc	Load Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
44	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
45	LSR	LSR f	f = Logical Right Shift f	1	1	C,N,OV,Z
		LSR f,WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws,Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles(1)	Status Flags Affected
46	MAC	MAC	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
		MAC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square and Accumulate	1	1	OA,OB,OAB, SA,SB,SAB
47	MOV	MOV	f,Wn	Move f to Wn	1	1	None
		MOV	f	Move f to f	1	1	None
		MOV	f,WREG	Move f to WREG	1	1	None
		MOV	#lit16,Wn	Move 16-bit Literal to Wn	1	1	None
		MOV.b	#lit8,Wn	Move 8-bit Literal to Wn	1	1	None
		MOV	Wn,f	Move Wn to f	1	1	None
		MOV	Wso,Wdo	Move Ws to Wd	1	1	None
		MOV	WREG,f	Move WREG to f	1	1	None
		MOV.D	Wns,Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D	Ws,Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
48	MOVPAG	MOVPAG	#lit10,DSRPAG	Move 10-bit Literal to DSRPAG	1	1	None
		MOVPAG	#lit9,DSWPAG	Move 9-bit Literal to DSWPAG	1	1	None
		MOVPAG	#lit8,TBLPAG	Move 8-bit Literal to TBLPAG	1	1	None
		MOVPAGW	Ws, DSRPAG	Move Ws[9:0] to DSRPAG	1	1	None
		MOVPAGW	Ws, DSWPAG	Move Ws[8:0] to DSWPAG	1	1	None
		MOVPAGW	Ws, TBLPAG	Move Ws[7:0] to TBLPAG	1	1	None
49	MOVSAC	MOVSAC	Acc,Wx,Wxd,Wy,Wyd,AWB	Prefetch and Store Accumulator	1	1	None
50	MPY	MPY	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		MPY	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
51	MPY.N	MPY.N	Wm*Wn,Acc,Wx,Wxd,Wy,Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
52	MSC	MSC	Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB, SA,SB,SAB

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
53	MUL	MUL.SS Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb,Ws,Acc	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb,Ws,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,Ws,Acc	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Acc	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb,Ws,Acc	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb,Ws,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb,#lit5,Acc	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,Ws,Acc	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb,Ws,Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb,Ws,Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb,Ws,Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb,Ws,Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb,#lit5,Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb,#lit5,Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None
54	NEG	NEG Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG f	f = $\bar{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG f,WREG	WREG = $\bar{f}$ + 1	1	1	C,DC,N,OV,Z
		NEG Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C,DC,N,OV,Z
55	NOP	NOP	No Operation	1	1	None
		NOPR	No Operation	1	1	None
56	POP	POP f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S	Pop Shadow Registers	1	1	All
57	PUSH	PUSH f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S	Push Shadow Registers	1	1	None
58	PWRSAV	PWRSAV #lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
59	RCALL	RCALL Expr	Relative Call	1	4	SFA
		RCALL Wn	Computed Call	1	4	SFA
60	REPEAT	REPEAT #lit15	Repeat Next Instruction lit15 + 1 Times	1	1	None
		REPEAT Wn	Repeat Next Instruction (Wn) + 1 Times	1	1	None
61	RESET	RESET	Software Device Reset	1	1	None
62	RETFIE	RETFIE	Return from Interrupt	1	6 (5)	SFA

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
63	RETLW	RETLW #lit10,Wn	Return with Literal in Wn	1	6 (5)	SFA
64	RETURN	RETURN	Return from Subroutine	1	6 (5)	SFA
65	RLC	RLC f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
66	RLNC	RLNC f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
67	RRC	RRC f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
		RRC Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
68	RRNC	RRNC f	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC f,WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
		RRNC Ws,Wd	Wd = Rotate Right (No Carry) Ws	1	1	N,Z
69	SAC	SAC Acc,#Slit4,Wdo	Store Accumulator	1	1	None
		SAC.R Acc,#Slit4,Wdo	Store Rounded Accumulator	1	1	None
70	SE	SE Ws,Wnd	Wnd = Sign-Extended Ws	1	1	C,N,Z
71	SETM	SETM f	f = 0xFFFF	1	1	None
		SETM WREG	WREG = 0xFFFF	1	1	None
		SETM Ws	Ws = 0xFFFF	1	1	None
72	SFTAC	SFTAC Acc,Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB, SA,SB,SAB
		SFTAC Acc,#Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB
73	SL	SL f	f = Left Shift f	1	1	C,N,OV,Z
		SL f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
74	SUB	SUB Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB #lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
75	SUBB	SUBB f	f = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB f,WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB #lit10,Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
76	SUBR	SUBR f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
77	SUBBR	SUBBR f	f = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR f,WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles(1)	Status Flags Affected
78	SWAP	SWAP.b Wn	Wn = Nibble Swap Wn	1	1	None
		SWAP Wn	Wn = Byte Swap Wn	1	1	None
79	TBLRDH	TBLRDH Ws,Wd	Read Prog[23:16] to Wd[7:0]	1	5	None
80	TBLRDL	TBLRDL Ws,Wd	Read Prog[15:0] to Wd	1	5	None
81	TBLWTH	TBLWTH Ws,Wd	Write Ws[7:0] to Prog[23:16]	1	2	None
82	TBLWTL	TBLWTL Ws,Wd	Write Ws to Prog[15:0]	1	2	None
83	ULNK	ULNK	Unlink Frame Pointer	1	1	SFA
84	XOR	XOR f	f = f .XOR. WREG	1	1	N,Z
		XOR f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR #lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
85	ZE	ZE Ws,Wnd	Wnd = Zero-Extend Ws	1	1	C,Z,N

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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29.0 DEVELOPMENT SUPPORT

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NOTES:

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30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EVXXXGM00X/10X family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.0V
Voltage on V_{CAP} with respect to V_{SS} ..... 1.62V to 1.98V
Maximum current out of V_{SS} pin ..... 350 mA
Maximum current into V_{DD} pin(2) ..... 350 mA
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sourced/sunk by all ports(2) ..... 200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

30.1 DC Characteristics

TABLE 30-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Maximum MIPS
			dsPIC33EVXXXGM00X/10X Family
I-Temp	4.5V to 5.5V(1,2)	-40°C to 0°C	60
		0°C to +85°C	70
E-Temp	4.5V to 5.5V(1,2)	-40°C to +125°C	60

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: When BOR is enabled, the device will work from 4.7V to 5.5V.

Note 1: Customer operating voltage range is specified as: 4.5V to 5.5V.

TABLE 30-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices:					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices:					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: $P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$ I/O Pin Power Dissipation: $I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 64-Pin QFN, 9x9x0.9 mm	θJA	28.0	—	°C/W	1
Package Thermal Resistance, 64-Pin TQFP, 10x10x1 mm	θJA	48.3	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN, 8x8 mm	θJA	29.0	—	°C/W	1
Package Thermal Resistance, 44-Pin TQFP, 10x10x1 mm	θJA	49.8	—	°C/W	1
Package Thermal Resistance, 48-pin TQFP, 7x7x1 mm	θJA	62.76	—	°C/W	1
Package Thermal Resistance, 36-Pin UQFN, 5x5 mm	θJA	29.2	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S, 6x6x0.9 mm	θJA	30.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC, 7.50 mm	θJA	69.7	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP, 5.30 mm	θJA	71.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP, 300 mil	θJA	60.0	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

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TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage(3)**	VBOR	—	5.5	V	
DC12	VDR	**RAM Data Retention Voltage(2)**	1.8	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0V-5.0V in 5 ms
DC18	VCORE	**VDD Core** Internal Regulator Voltage	1.62	1.8	1.98	V	Voltage is dependent on load, temperature and VDD

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: VDD voltage must remain at VSS for a minimum of 200 µs to ensure POR.

TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended							
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
	CEFC	External Filter Capacitor Value(1)	4.7	10	—	µF	Capacitor must have a low series resistance (< 1Ω)

Note 1: Typical VCAP Voltage = 1.8 volts when VDD ≥ VDDMIN.

TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param.	**Typ.(2)**	**Max.**	**Units**	**Conditions**		
Operating Current (IDD)(1)						
DC20d	4.5	5.5	mA	-40°C	5.0V	10 MIPS
DC20a	4.65	5.6	mA	+25°C		
DC20b	4.85	6.0	mA	+85°C		
DC20c	5.6	7.2	mA	+125°C		
DC22d	8.6	10.6	mA	-40°C	5.0V	20 MIPS
DC22a	8.8	10.8	mA	+25°C		
DC22b	9.1	11.1	mA	+85°C		
DC22c	9.8	12.6	mA	+125°C		
DC23d	16.8	18.5	mA	-40°C	5.0V	40 MIPS
DC23a	17.2	19.0	mA	+25°C		
DC23b	17.55	19.2	mA	+85°C		
DC23c	18.3	21.0	mA	+125°C		
DC24d	25.15	28.0	mA	-40°C	5.0V	60 MIPS
DC24a	25.5	28.0	mA	+25°C		
DC24b	25.5	28.0	mA	+85°C		
DC24c	25.55	28.5	mA	+125°C		
DC25d	29.0	31.0	mA	-40°C	5.0V	70 MIPS
DC25a	28.5	31.0	mA	+25°C		
DC25b	28.3	31.0	mA	+85°C		

Note 1: IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing

```
while(1)
{
NOP();
}
```

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

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TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typ.(2)**	**Max.**	**Units**	**Conditions**		
Idle Current (IIDLE)(1)						
DC40d	1.25	2	mA	-40°C	5.0V	10 MIPS
DC40a	1.25	2	mA	+25°C		
DC40b	1.5	2.6	mA	+85°C		
DC40c	1.5	2.6	mA	+125°C		
DC42d	2.3	3	mA	-40°C	5.0V	20 MIPS
DC42a	2.3	3	mA	+25°C		
DC42b	2.6	3.45	mA	+85°C		
DC42c	2.6	3.85	mA	+125°C		
DC44d	6.9	8	mA	-40°C	5.0V	70 MIPS
DC44a	6.9	8	mA	+25°C		
DC44b	7.25	8.6	mA	+85°C		

Note 1: Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- The NVMSIDL bit (NVMCON[12]) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON[11]) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Typ.**	**Max.**	**Units**	**Conditions**			
Power-Down Current (I_{PD}) – dsPIC33EVXXXGM00X/10X							
DC60d	9.25	35	µA	-40°C	5.0V	Grade 3 Mission Profile	Base Power-Down Current
	9.25	60	µA			Grade 1 Mission Profile	
DC60a	15.75	40	µA	+25°C	5.0V	Grade 3 Mission Profile	
	15.75	75	µA			Grade 1 Mission Profile	
DC60b	67.75	300	µA	+85°C	5.0V	Grade 3 Mission Profile	
	67.75	425	µA			Grade 1 Mission Profile	
DC60c	270	820	µA	+125°C	5.0V	Grade 1 Mission Profile	
DC61d	1	7	µA	-40°C	5.0V	Watchdog Timer Current: ΔI_{WDT}	
DC61a	1.25	8	µA	+25°C			
DC61b	3.5	12	µA	+85°C			
DC61c	5	15	µA	+125°C			

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TABLE 30-9: DC CHARACTERISTICS: DOZE CURRENT (I_{DOZE})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Typ.(2)**	**Max.**	**Doze Ratio**	**Units**	**Conditions**		
Doze Current (I_{DOZE})(1)							
DC73a	16.0	18.25	1:2	mA	-40°C	5.0V	70 MIPS
DC73g	7.1	8.0	1:128	mA			
DC70a	16.25	18.5	1:2	mA	+25°C	5.0V	70 MIPS
DC70g	7.3	8.2	1:128	mA			
DC71a	17.0	19.0	1:2	mA	+85°C	5.0V	70 MIPS
DC71g	7.5	8.9	1:128	mA			
DC72a	17.75	19.95	1:2	mA	+125°C	5.0V	60 MIPS
DC72g	8.25	9.32	1:128	mA			

Note 1: I_{DOZE} is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all I_{DOZE} measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{MCLR}$ = V_{DD}, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing

```
while(1)
{
NOP();
}
```

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

TABLE 30-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI10	VIL	**Input Low Voltage** I/O Pins	VSS	—	0.2 VDD	V	
DI20	VIH	**Input High Voltage** I/O Pins	0.75 VDD	—	5.5	V	
DI30	ICNPU	**Change Notification Pull-up Current**	200	375	600	µA	VDD = 5.0V, VPIN = VSS
DI31	ICNPD	**Change Notification Pull-Down Current(7)**	175	400	625	µA	VDD = 5.0V, VPIN = VDD
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Pins	-100	—	100	nA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		MCLR	-700	—	700	nA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	-200	—	200	nA	VSS ≤ VPIN ≤ VDD, XT and HS modes
DI60a	IICL	**Input Low Injection Current**	0	—	-5(4,6)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7
DI60b	IICH	**Input High Injection Current**	0	—	+5(5,6)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins(5)
DI60c	∑IICT	**Total Input Injection Current** (sum of all I/O and control pins)	-20(7)	—	+20(7)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL |+ | IICH |) ≤ ∑IICT

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: VIL source < (VSS – 0.3). Characterized but not tested.

5: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

6: Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

7: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

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TABLE 30-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
DO16	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	IOL = 8.8 mA, VDD = 5.0V
DO10	VOL	**Output Low Voltage** 8x Sink Driver Pins(3)	—	—	0.4	V	IOL = 10.8 mA, VDD = 5.0V
DO26	VOH	**Output High Voltage** 4x Sink Driver Pins(2)	VDD – 0.6	—	—	V	IOH = -8.3 mA, VDD = 5.0V
DO20	VOH	**Output High Voltage** 8x Sink Driver Pins	VDD – 0.6	—	—	V	IOH = -12.3 mA, VDD = 5.0V

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x sink driver pins (see below).

3: Includes pins, such as RA3, RA4 and RB[15:10] for 28-pin and 36-pin devices, RA3, RA4, RA9 and RB[15:10] for 44-pin and 48-pin devices, RA4, RA7, RA9, RB[15:10] and RC15 for 64-pin devices.

TABLE 30-12: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	4.15	4.285	4.4	V	VDD (see **Note 2**, **Note 3** and **Note 4**)

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The VBOR specification is relative to the VDD.

3: The device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized.

4: The start-up VDD must rise above 4.6V.

TABLE 30-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	4.5	—	5.5	V	
D132b	VPEW	VDD for Self-Timed Write	4.5	—	5.5	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current During Programming	—	10	—	mA	
D136a	TRW	Row Write Cycle Time	0.657	—	0.691	ms	TRW = 4965 FRC cycles, TA = +85°C (see **Note 2**)
D136b	TRW	Row Write Cycle Time	0.651	—	0.698	ms	TRW = 4965 FRC cycles, TA = +125°C (see **Note 2**)
D137a	TPE	Page Erase Time	19.44	—	20.44	ms	TPE = 146893 FRC cycles, TA = +85°C (see **Note 2**)
D137b	TPE	Page Erase Time	19.24	—	20.65	ms	TPE = 146893 FRC cycles, TA = +125°C (see **Note 2**)
D138a	TWW	Word Write Cycle Time	45.78	—	48.15	µs	TWW = 346 FRC cycles, TA = +85°C (see **Note 2**)
D138b	TWW	Word Write Cycle Time	45.33	—	48.64	µs	TWW = 346 FRC cycles, TA = +125°C (see **Note 2**)

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.3728 MHz, TUN[5:0] = `b'011111` (for Min), TUN[5:0] = `b'100000` (for Max). This parameter depends on the FRC accuracy (see Table 30-20) and the value of the FRC Oscillator Tuning register.

TABLE 30-14: ELECTRICAL CHARACTERISTICS: INTERNAL BAND GAP REFERENCE VOLTAGE

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DVR10	VBG	Internal Band Gap Reference Voltage	1.14	1.2	1.26	V	

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30.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**.

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

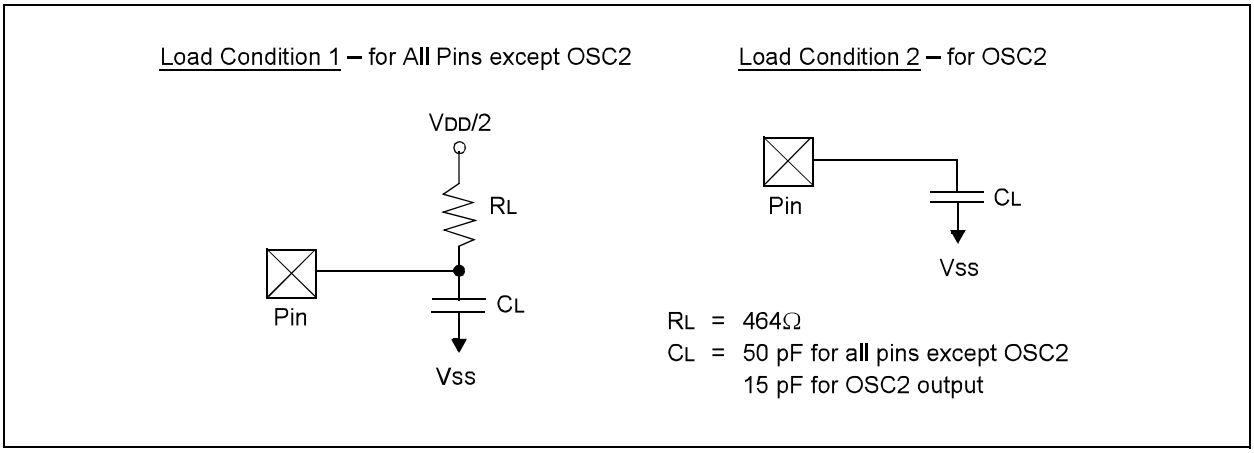


TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	COSCO	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	CIO	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I^2C mode

FIGURE 30-2: EXTERNAL CLOCK TIMING

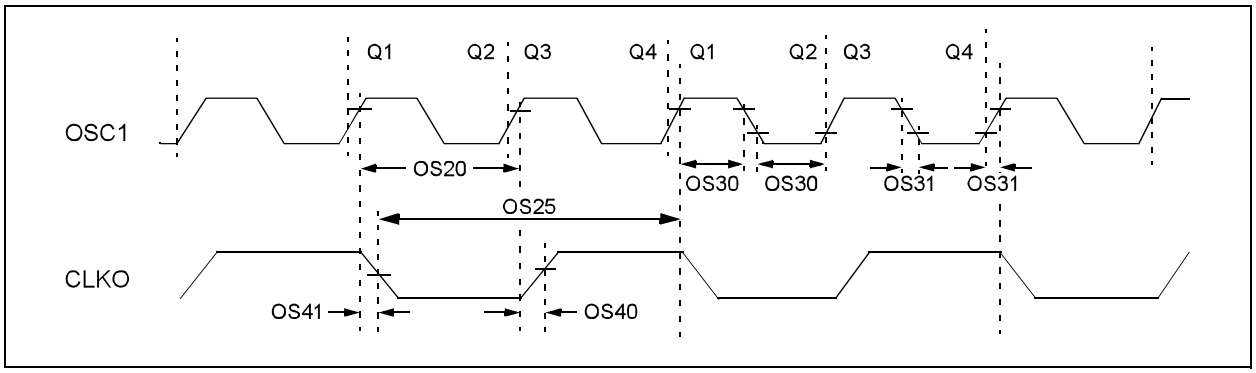


TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Sym**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS10	FIN	External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)	DC	—	40	MHz	EC
		Oscillator Crystal Frequency	3.5 10	— —	10 25	MHz MHz	XT HS
OS20	TOSC	TOSC = 1/FOSC	12.5	—	DC	ns	TA = +125°C
OS25	TCY	Instruction Cycle Time(2)	25	—	DC	ns	TA = +125°C
OS30	TosL, TosH	External Clock in (OSC1) High or Low Time	0.375 x TOSC	—	0.625 x TOSC	ns	EC
OS31	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	20	ns	EC
OS40	TckR	CLKO Rise Time(3)	—	5.2	—	ns	
OS41	TckF	CLKO Fall Time(3)	—	5.2	—	ns	
OS42	GM	External Oscillator Transconductance(4)	—	12	—	mA/V	HS, VDD = 5.0V, TA = +25°C
			—	6	—	mA/V	XT, VDD = 5.0V, TA = +25°C

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type, under standard operating conditions, with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "Minimum" values with an external clock applied to the OSC1 pin. When an external clock input is used, the "Maximum" cycle time limit is "DC" (no clock) for all devices.

3: Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

4: This parameter is characterized but not tested in manufacturing.

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TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
OS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
OS51	FSYS	On-Chip VCO System Frequency	120	—	340	MHz	
OS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
OS53	DCLK	CLKO Stability (Jitter)(2)	-3	0.5	3	%	

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 30-19: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)							
F20a	FRC	-1	0.5	+1	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
F20b	FRC	-2	1	+2	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V

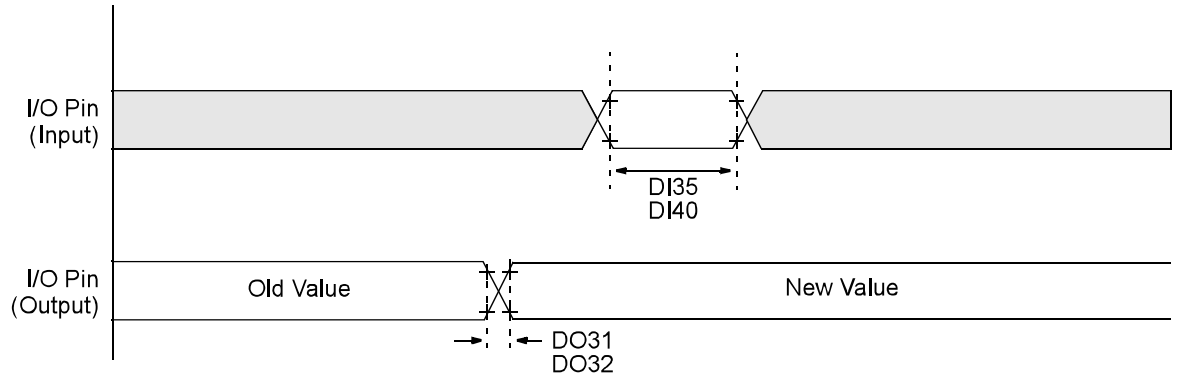
Note 1: Frequency calibrated at +25°C and 5.0V. TUN[5:0] bits can be used to compensate for temperature drift.

TABLE 30-20: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
LPRC @ 32.768 kHz(1)							
F21a	LPRC	-15	5	+15	%	-40°C ≤ TA ≤ +85°C	VDD = 4.5-5.5V
F21b	LPRC	-30	10	+30	%	-40°C ≤ TA ≤ +125°C	VDD = 4.5-5.5V

Note 1: Change of LPRC frequency as VDD changes.

FIGURE 30-3: I/O TIMING CHARACTERISTICS



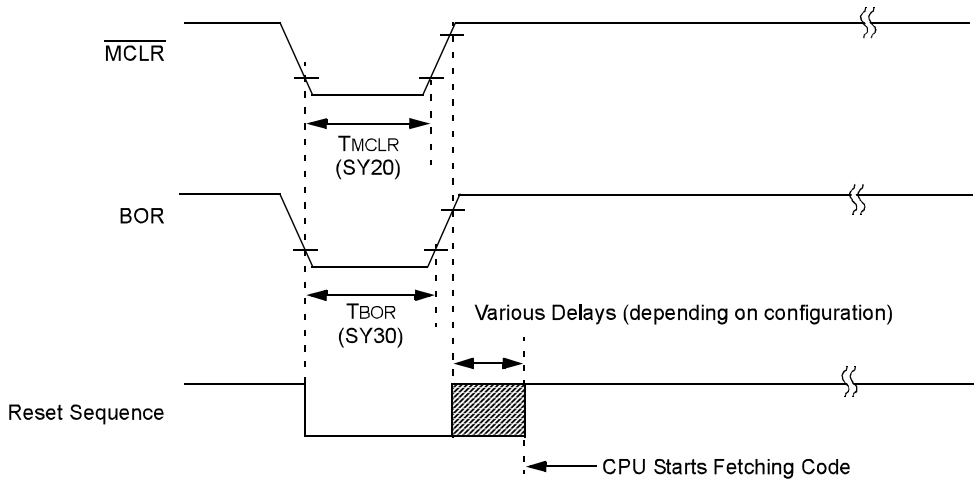
Note: Refer to Figure 30-1 for load conditions.

TABLE 30-21: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DO31	TIOR	Port Output Rise Time	—	5	10	ns	
DO32	TIOF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	TCY	

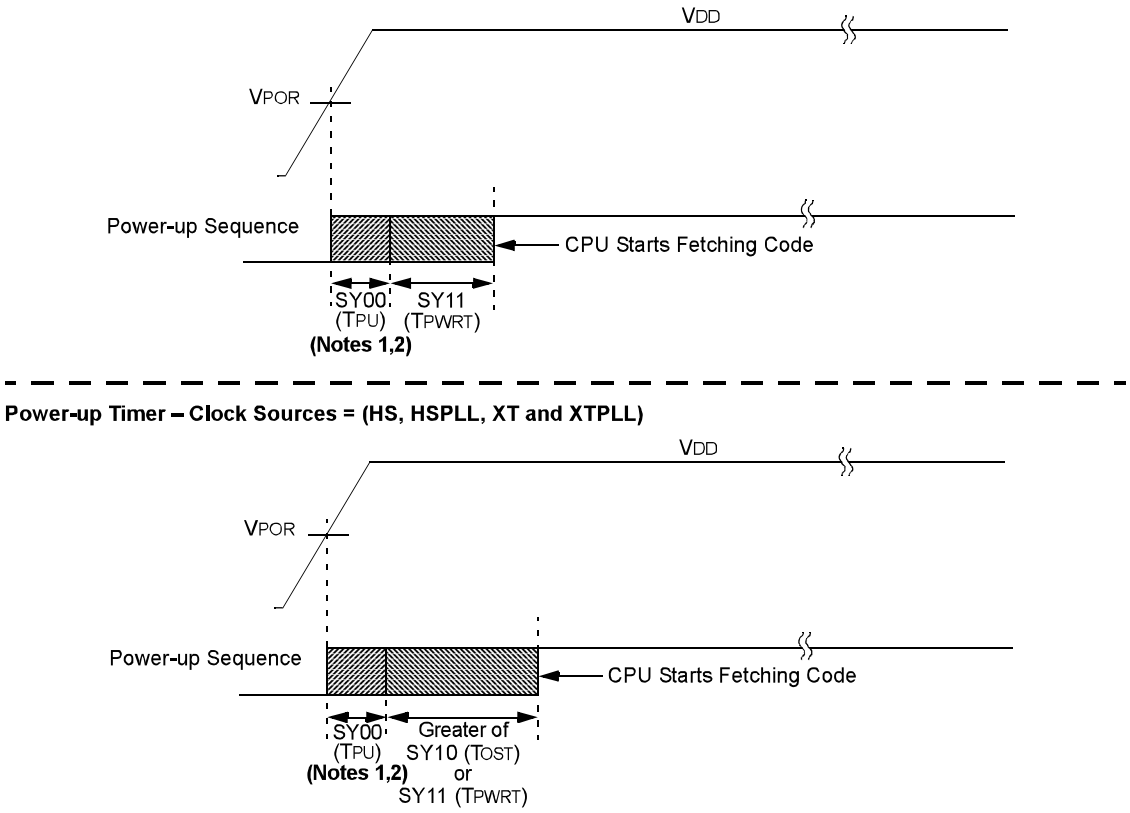
Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS



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FIGURE 30-5: POWER-ON RESET TIMING CHARACTERISTICS



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{BOR}$).

2: The power-up period includes internal voltage regulator stabilization delay.

TABLE 30-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING REQUIREMENTS

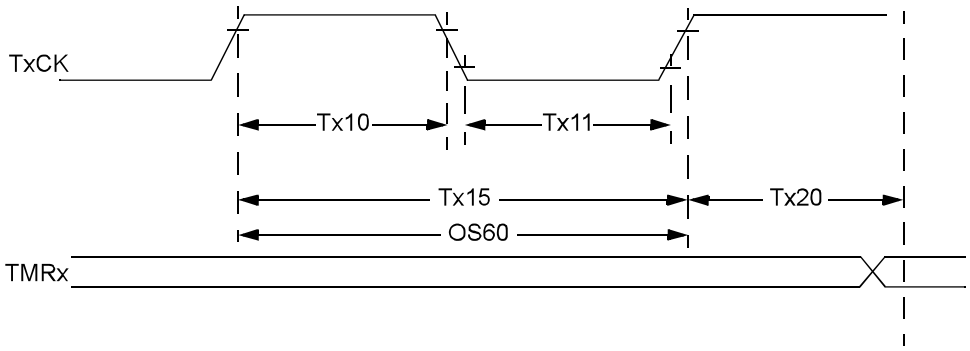
AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic(1)	Min.	Typ.(2)	Max.	Units	Conditions
SY00	TPU	Power-up Period	—	400	600	µs	
SY10	TOST	Oscillator Start-up Time	—	1024 Tosc	—	—	Tosc = OSC1 period
SY11	TPWRT	Power-up Timer Period	—	1	—	ms	Using LPRC parameters indicated in F21a/F21b (see Table 30-20)
SY12	TWDT	Watchdog Timer Time-out Period	0.8	—	1.2	ms	WDTPRE = 0, WDTPS[3:0] = 0000, using LPRC tolerances indicated in F21a/F21b (see Table 30-20) at +85°C
			3.2	—	4.8	ms	WDTPRE = 1, WDTPS[3:0] = 0000, using LPRC tolerances indicated in F21a/F21b (see Table 30-20) at +85°C
SY13	TIOZ	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	0.68	0.72	1.2	µs	
SY20	TMCLR	MCLR Pulse Width (low)	2	—	—	µs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	µs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	µs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	30	µs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	46	48	54	µs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	µs	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

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FIGURE 30-6: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(2)**		**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TA10	TTXH	T1CK High Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TA15, N = Prescaler Value (1, 8, 64, 256)
			Asynchronous mode	35	—	—	ns	
TA11	TTXL	T1CK Low Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TA15, N = Prescaler Value (1, 8, 64, 256)
			Asynchronous mode	10	—	—	ns	
TA15	TTXP	T1CK Input Period	Synchronous mode	Greater of: 40 or (2 TCY + 40)/N	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
OS60	Ft1	T1CK Oscillator Input Frequency Range (oscillator enabled by setting TCS (T1CON[1]) bit)		DC	—	50	kHz	
TA20	TCKEXTMRL	Delay from External T1CK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: Timer1 is a Type A.

2: These parameters are characterized but not tested in manufacturing.

TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic(1)		Min.	Typ.	Max.	Units	Conditions
TB10	TTXH	TxCK High Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)
TB11	TTXL	TxCK Low Time	Synchronous mode	Greater of: 20 or (TCY + 20)/N	—	—	ns	Must also meet Parameter TB15, N = Prescaler Value (1, 8, 64, 256)
TB15	TTXP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 TCY + 40)/N	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

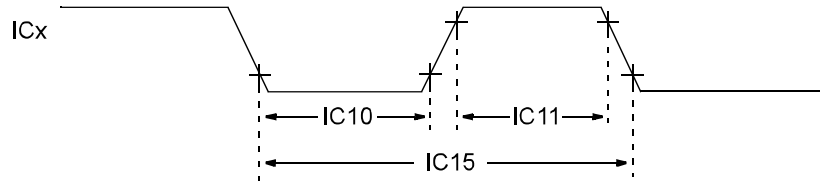
TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic(1)		Min.	Typ.	Max.	Units	Conditions
TC10	TTXH	TxCK High Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC11	TTXL	TxCK Low Time	Synchronous	TCY + 20	—	—	ns	Must also meet Parameter TC15
TC15	TTXP	TxCK Input Period	Synchronous, with Prescaler	2 TCY + 40	—	—	ns	N = Prescaler Value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 TCY + 40	—	1.75 TCY + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 30-7: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



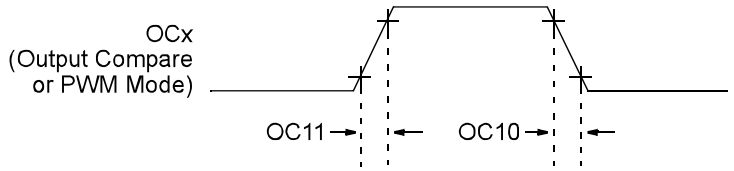
Note 1: Refer to Figure 30-1 for load conditions.

TABLE 30-26: INPUT CAPTURE x (ICx) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TccL	ICx Input Low Time	Greater of: 12.5 + 25 or (0.5 TCY/N) + 25	—	ns	Must also meet Parameter IC15	N = Prescaler Value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of: 12.5 + 25 or (0.5 TCY/N) + 25	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of: 25 + 50 or (1 TCY/N) + 50	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OUTPUT COMPARE x (OCx) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-27: OUTPUT COMPARE x (OCx) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-9: OCx/PWMx MODULE TIMING CHARACTERISTICS

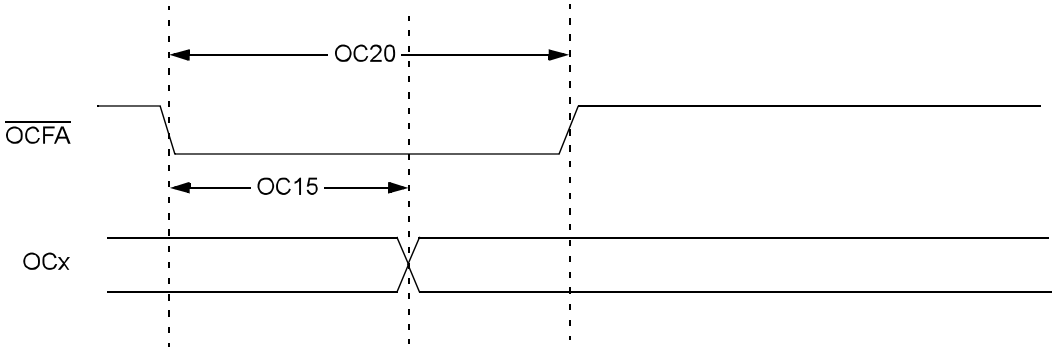


TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OC15	TFD	Fault Input to PWMx I/O Change	—	—	TCY + 20	ns	
OC20	TFLT	Fault Input Pulse Width	TCY + 20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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FIGURE 30-10: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS

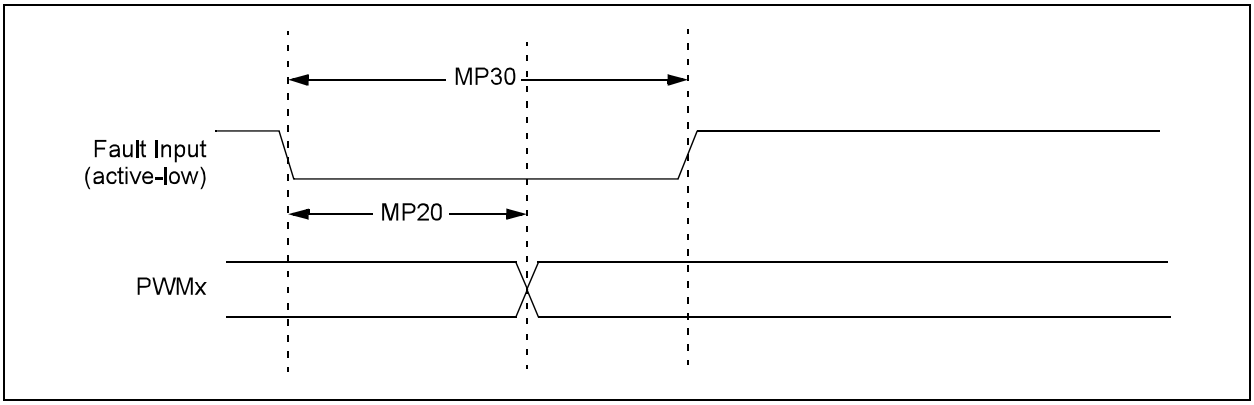
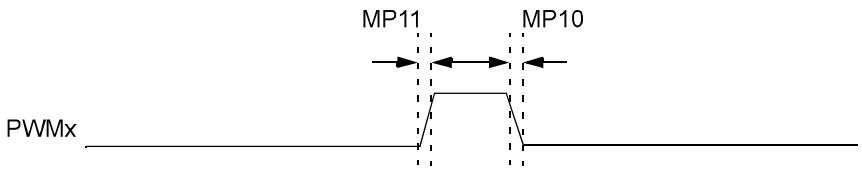


FIGURE 30-11: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS

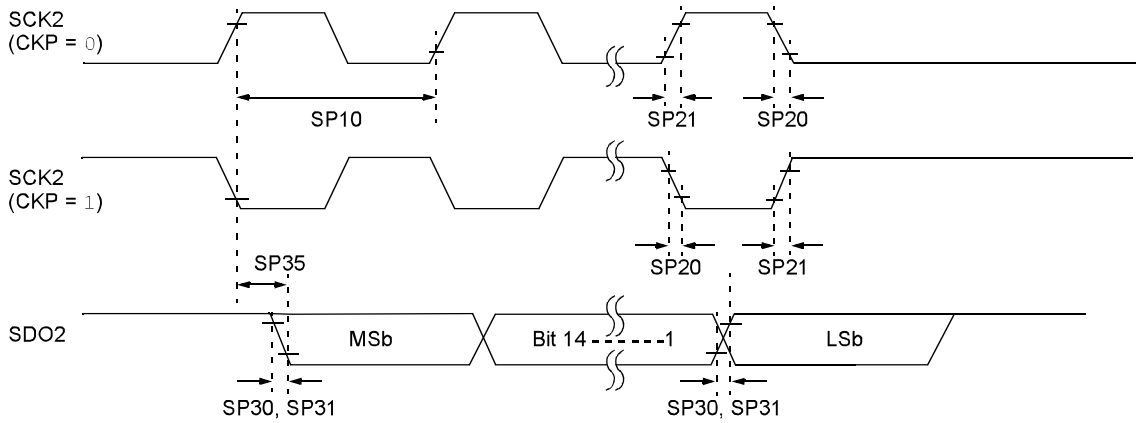
AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	TFPWM	PWMx Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWMx I/O Change	—	—	15	ns	
MP30	TFH	Fault Input Pulse Width	15	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-30: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
15 MHz	Table 30-31	—	—	0,1	0,1	0,1
9 MHz	—	Table 30-32	—	1	0,1	1
9 MHz	—	Table 30-33	—	0	0,1	1
15 MHz	—	—	Table 30-34	1	0	0
11 MHz	—	—	Table 30-35	1	1	0
15 MHz	—	—	Table 30-36	0	1	0
11 MHz	—	—	Table 30-37	0	0	0

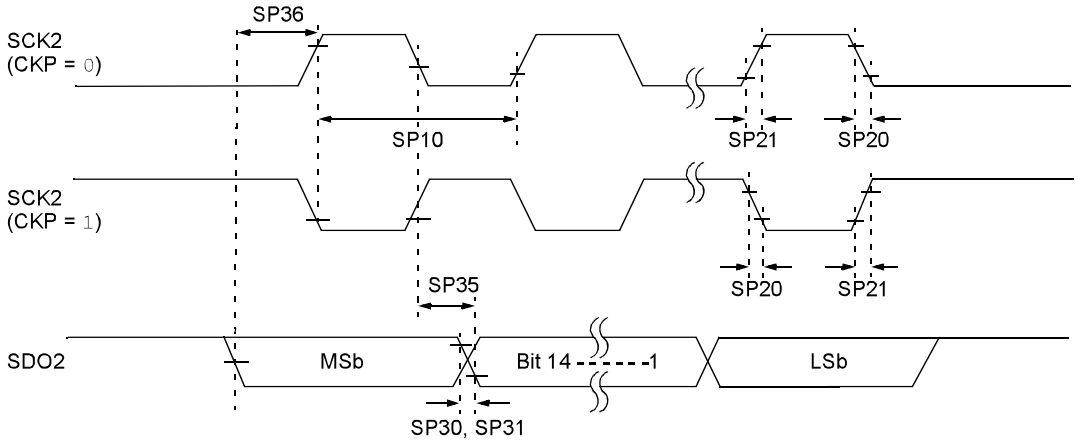
FIGURE 30-12: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

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FIGURE 30-13: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-31: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK2 Frequency	—	—	15	MHz	See **Note 3**
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	

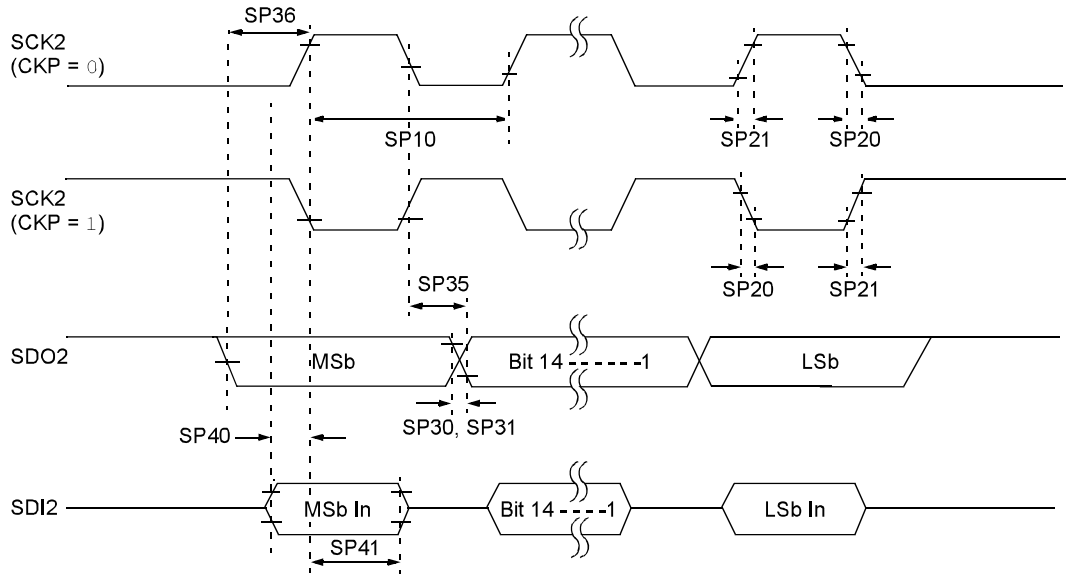
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-14: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-32: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	See **Note 3**
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

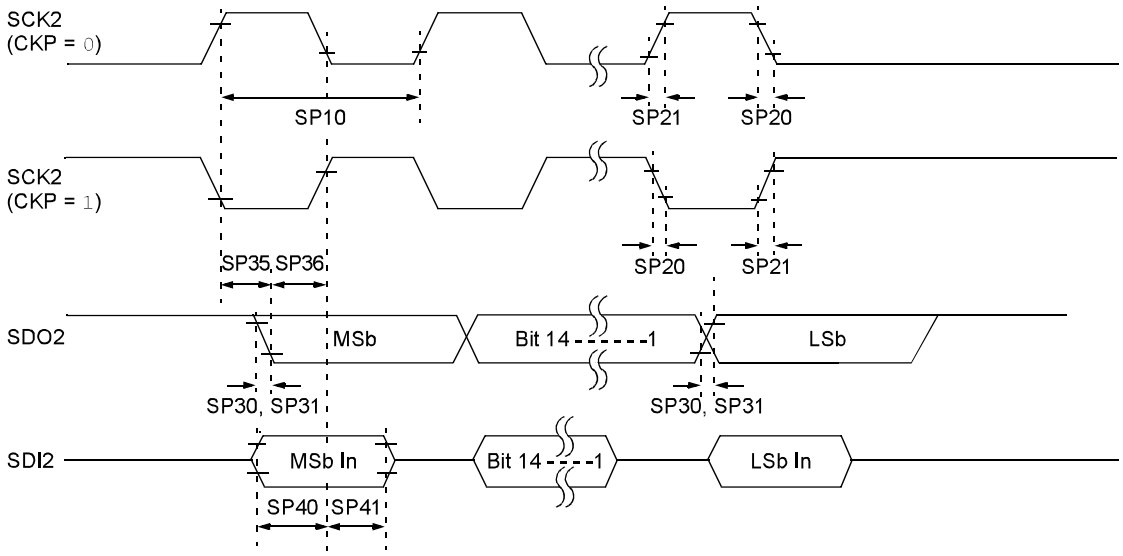
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

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FIGURE 30-15: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-33: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK2 Frequency	—	—	9	MHz	-40ºC to +125ºC and see **Note 3**
SP20	TscF	SCK2 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK2 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

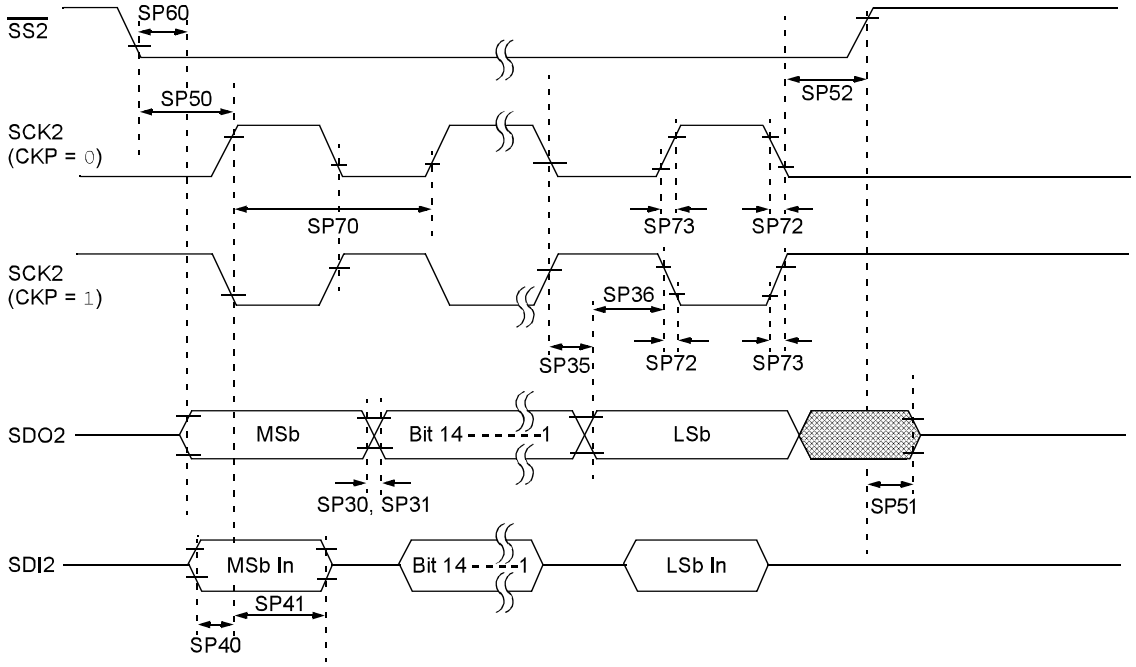
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

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FIGURE 30-16: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

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TABLE 30-34: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	SDO2 Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

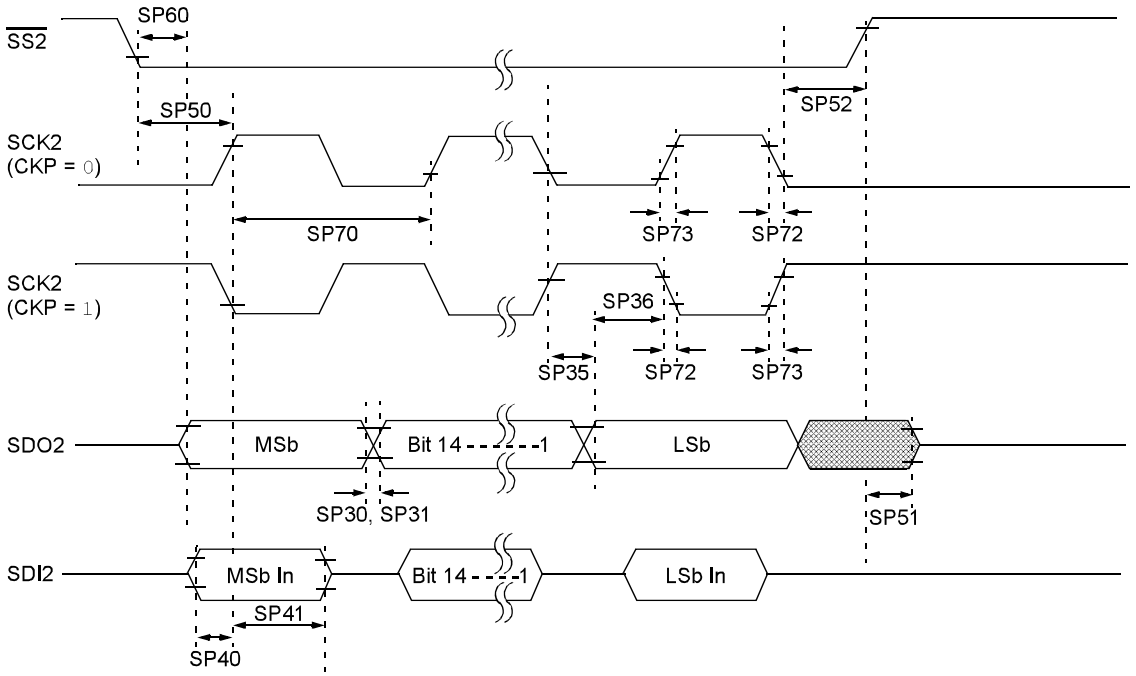
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

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FIGURE 30-17: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

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TABLE 30-35: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	SDO2 Data Output Valid after $\overline{SS2}$ Edge	—	—	50	ns	

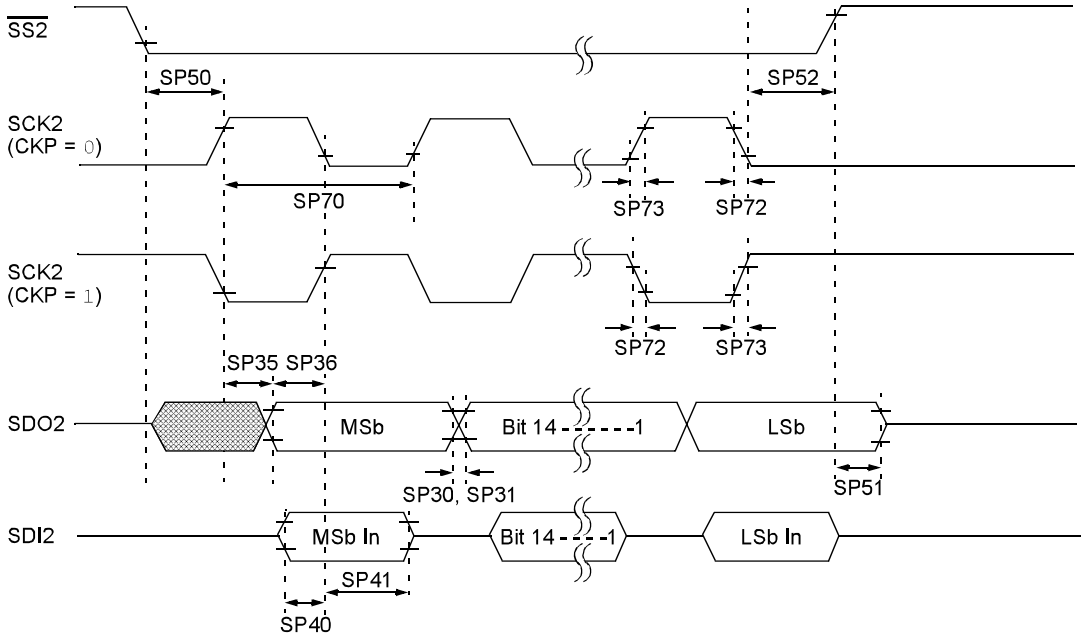
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

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TABLE 30-36: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	15	MHz	See **Note 3**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

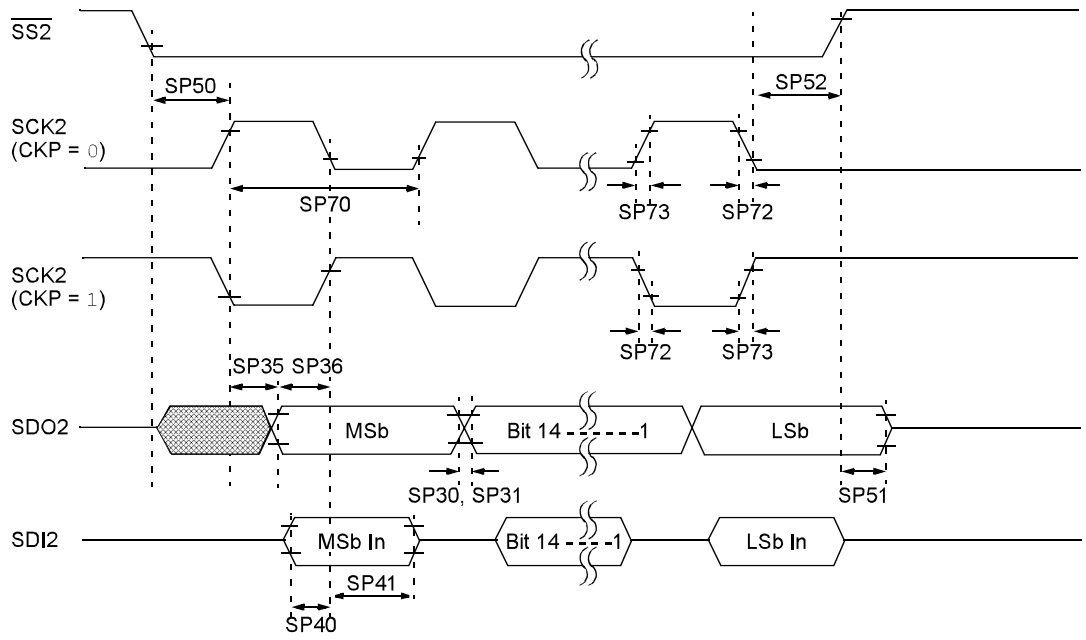
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

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TABLE 30-37: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK2 Input Frequency	—	—	11	MHz	See **Note 3**
SP72	TscF	SCK2 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK2 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO2 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO2 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO2 Data Output Valid after SCK2 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO2 Data Output Setup to First SCK2 Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI2 Data Input to SCK2 Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS2}$ ↑ to SDO2 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SS2}$ ↑ after SCK2 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

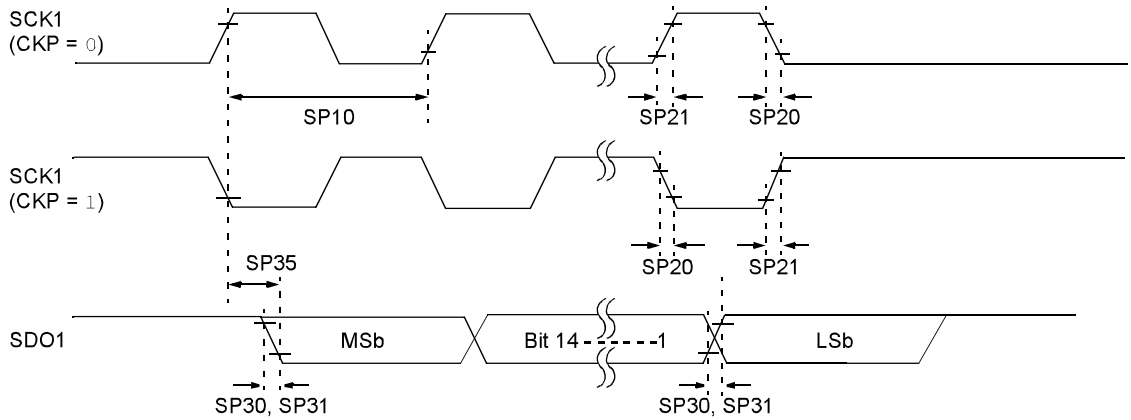
3: The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI2 pins.

TABLE 30-38: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	Master Transmit Only (Half-Duplex)	Master Transmit/Receive (Full-Duplex)	Slave Transmit/Receive (Full-Duplex)	CKE	CKP	SMP
25 MHz	Table 30-39	—	—	0,1	0,1	0,1
25 MHz	—	Table 30-40	—	1	0,1	1
25 MHz	—	Table 30-41	—	0	0,1	1
25 MHz	—	—	Table 30-42	1	0	0
25 MHz	—	—	Table 30-43	1	1	0
25 MHz	—	—	Table 30-44	0	1	0
25 MHz	—	—	Table 30-45	0	0	0

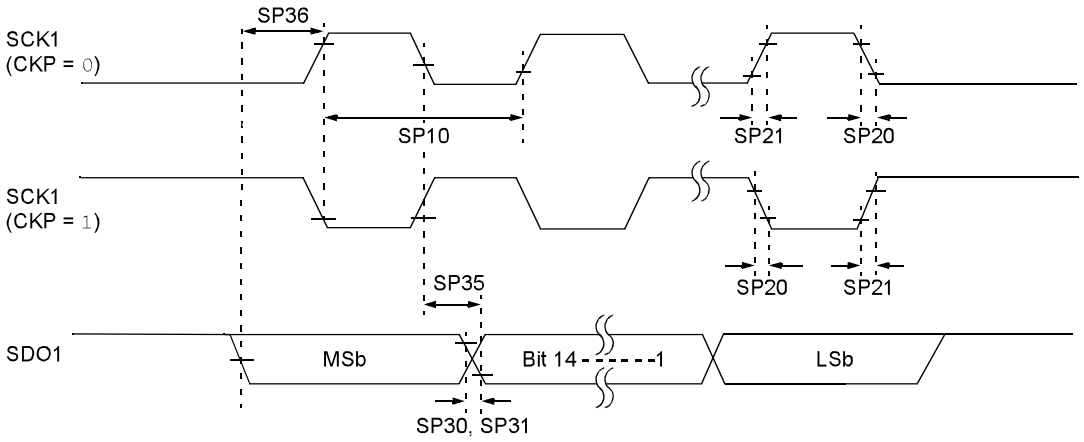
FIGURE 30-20: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

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FIGURE 30-21: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-39: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See **Note 3**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdiV2scH, TdiV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	

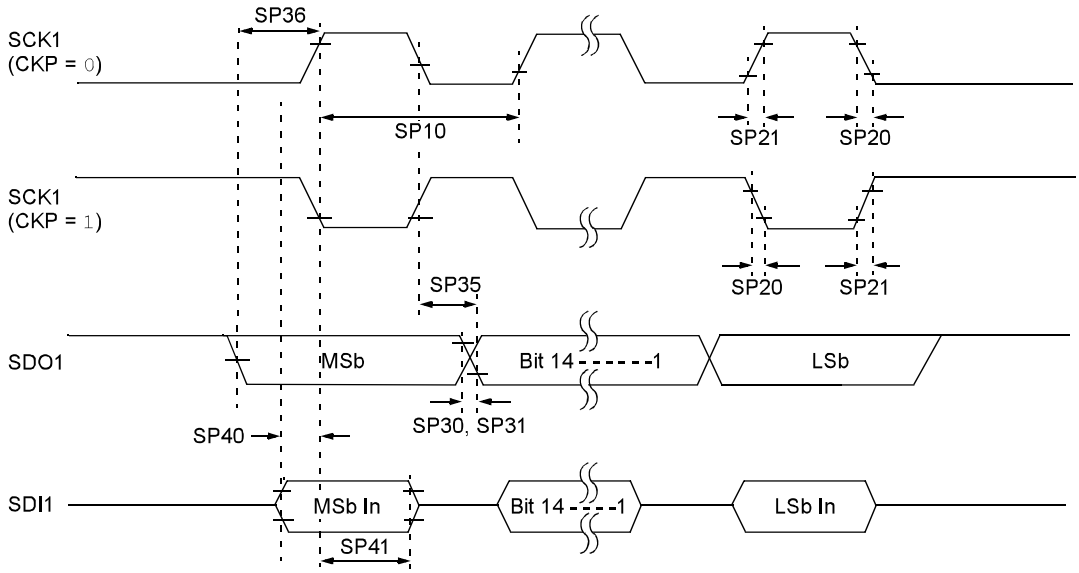
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

FIGURE 30-22: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-40: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	See **Note 3**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

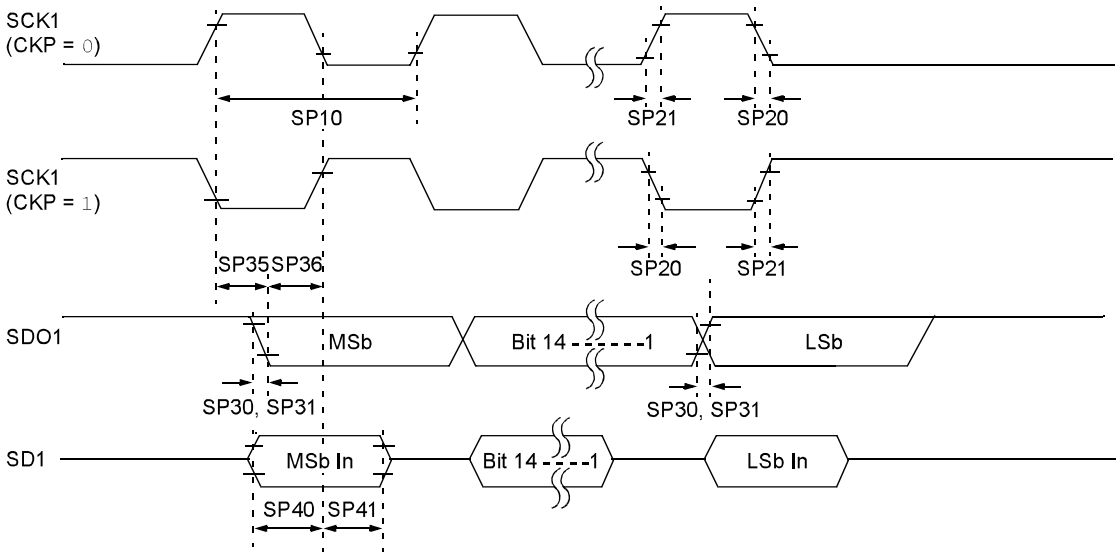
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 30-23: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-41: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP10	FscP	Maximum SCK1 Frequency	—	—	25	MHz	-40°C to +125°C and see **Note 3**
SP20	TscF	SCK1 Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP21	TscR	SCK1 Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

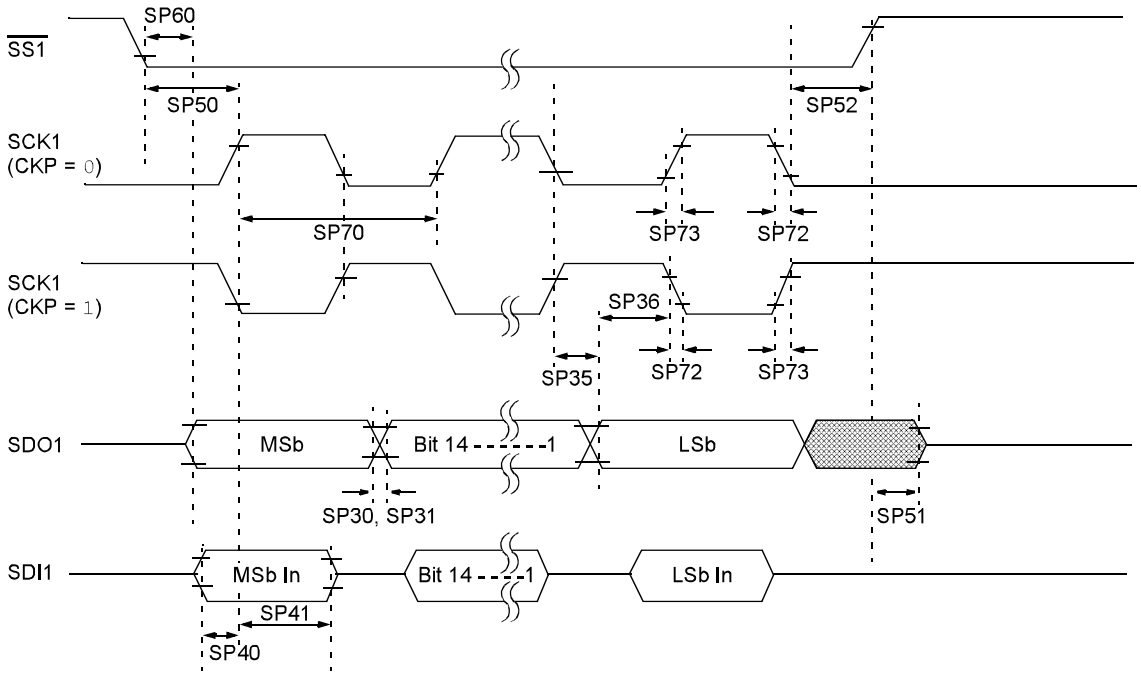
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 30-24: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-42: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

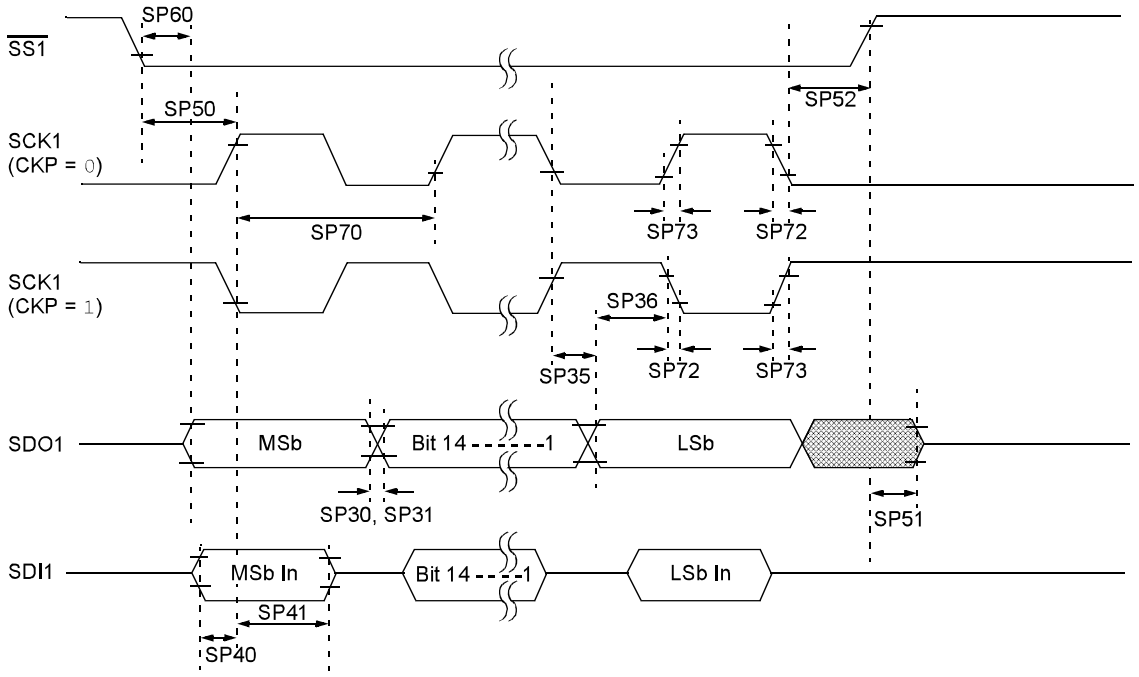
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 30-25: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-43: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

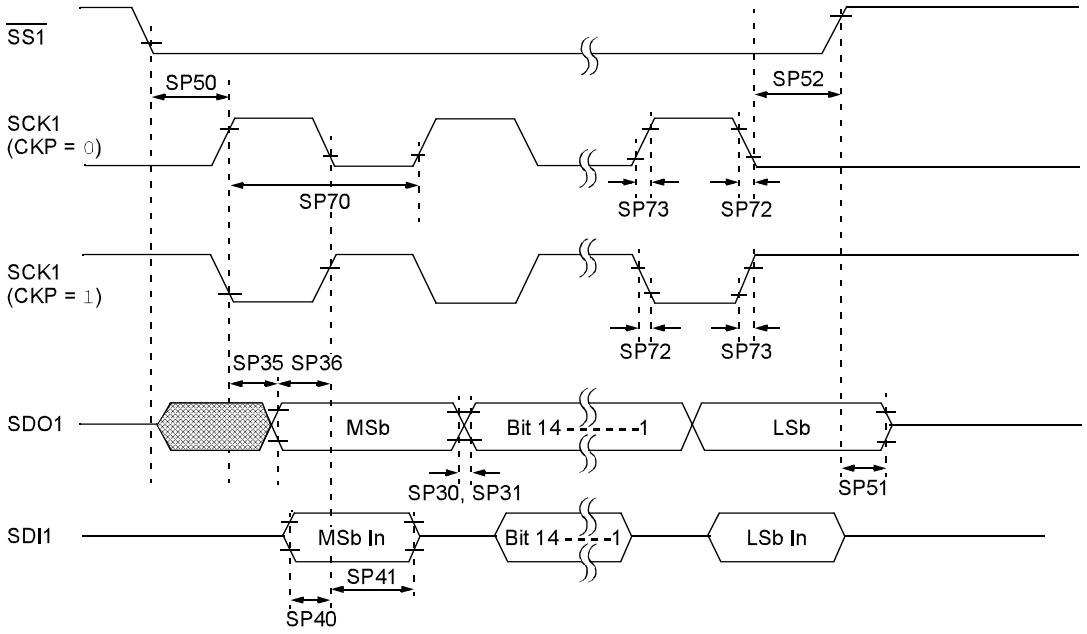
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-44: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized but not tested in manufacturing.

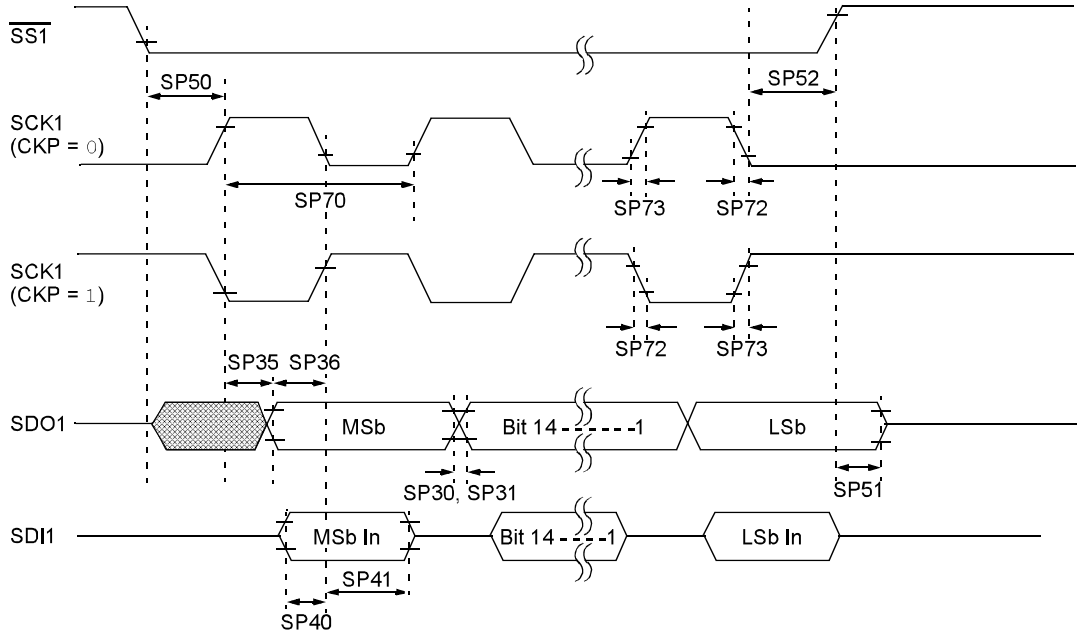
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

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FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	See **Note 3**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 and **Note 4**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 and **Note 4**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	See **Note 4**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	See **Note 4**

Note 1: These parameters are characterized but not tested in manufacturing.

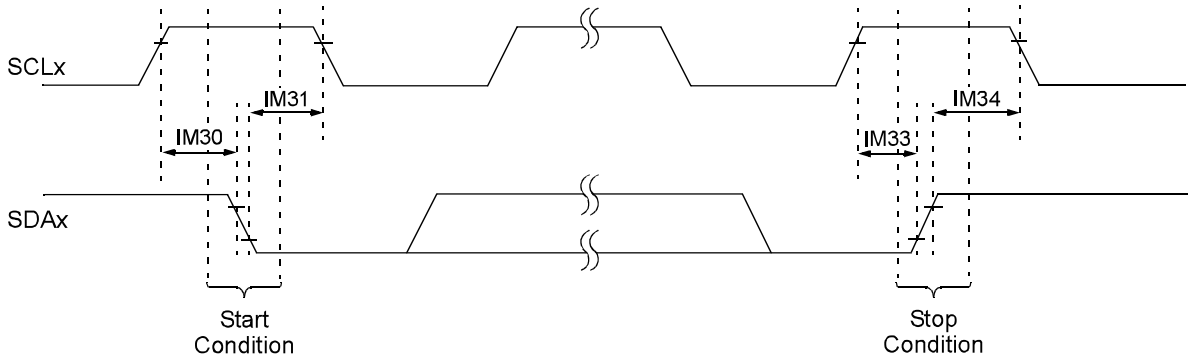
2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 40 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

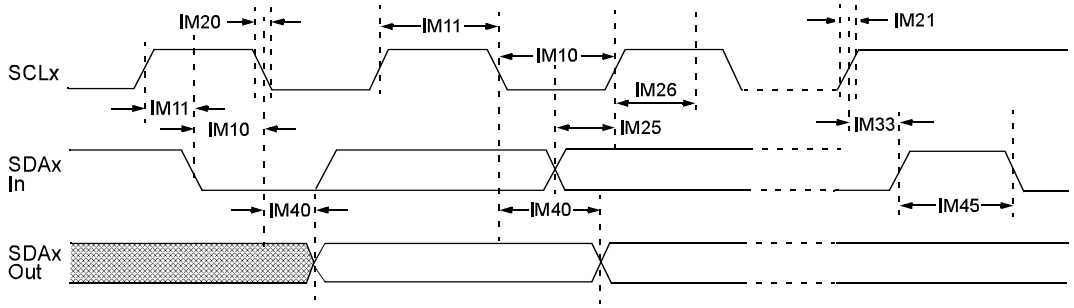
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FIGURE 30-28: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 30-1 for load conditions.

FIGURE 30-29: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-46: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic(4)		Min.(1)	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM11	THI:SCL	Clock High Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode(2)	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode(2)	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode(2)	0.2	—	µs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	TCY/2 (BRG +2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	TCY/2 (BRG + 2)	—	µs	
			400 kHz mode	TCY/2 (BRG + 2)	—	µs	
			1 MHz mode(2)	TCY/2 (BRG + 2)	—	µs	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode(2)	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode(2)	0.5	—	µs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	See **Note 3**

Note 1: BRG is the value of the I^2C Baud Rate Generator. Refer to **"Inter-Integrated Circuit (I^2C)"** (www.microchip.com/DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*. Please see the Microchip website for the latest *"dsPIC33/PIC24 Family Reference Manual"* sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized but not tested in manufacturing.

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FIGURE 30-30: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

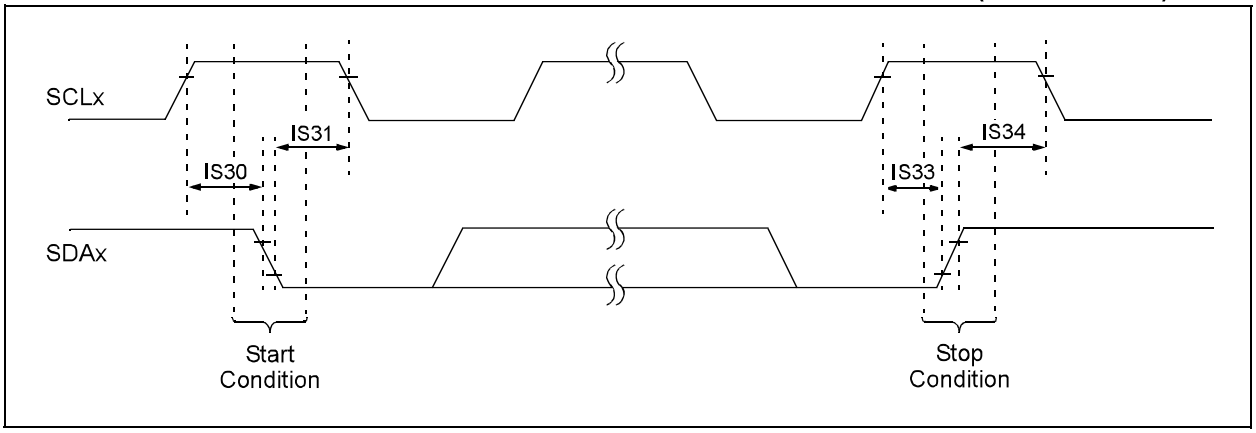


FIGURE 30-31: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)

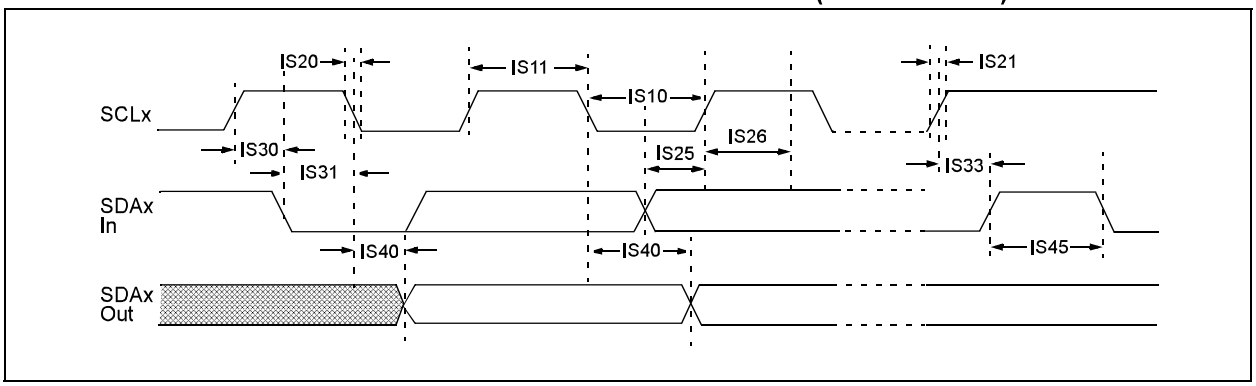


TABLE 30-47: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param. No.	Symbol	Characteristic[3]		Min.	Max.	Units	Conditions
IS10	TLO:SCL	Clock Low Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	1.3	—	µs	
			1 MHz mode[1]	0.5	—	µs	
IS11	THI:SCL	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			1 MHz mode[1]	0.5	—	µs	
IS20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode[1]	—	100	ns	
IS21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 CB	300	ns	
			1 MHz mode[1]	—	300	ns	
IS25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode[1]	100	—	ns	
IS26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	µs	
			400 kHz mode	0	0.9	µs	
			1 MHz mode[1]	0	0.3	µs	
IS30	TSU:STA	Start Condition Setup Time	100 kHz mode	4.7	—	µs	Only relevant for Repeated Start condition
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.25	—	µs	
IS31	THD:STA	Start Condition Hold Time	100 kHz mode	4.0	—	µs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.25	—	µs	
IS33	TSU:STO	Stop Condition Setup Time	100 kHz mode	4.7	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.6	—	µs	
IS34	THD:STO	Stop Condition Hold Time	100 kHz mode	4	—	µs	
			400 kHz mode	0.6	—	µs	
			1 MHz mode[1]	0.25		µs	
IS40	TAA:SCL	Output Valid From Clock	100 kHz mode	0	3500	ns	
			400 kHz mode	0	1000	ns	
			1 MHz mode[1]	0	350	ns	
IS45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
			1 MHz mode[1]	0.5	—	µs	
IS50	CB	Bus Capacitive Loading		—	400	pF	
IS51	TPGD	Pulse Gobbler Delay		65	390	ns	See Note 2

Note 1: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

2: The typical value for this parameter is 130 ns.

3: These parameters are characterized but not tested in manufacturing.

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FIGURE 30-32: CANx MODULE I/O TIMING CHARACTERISTICS

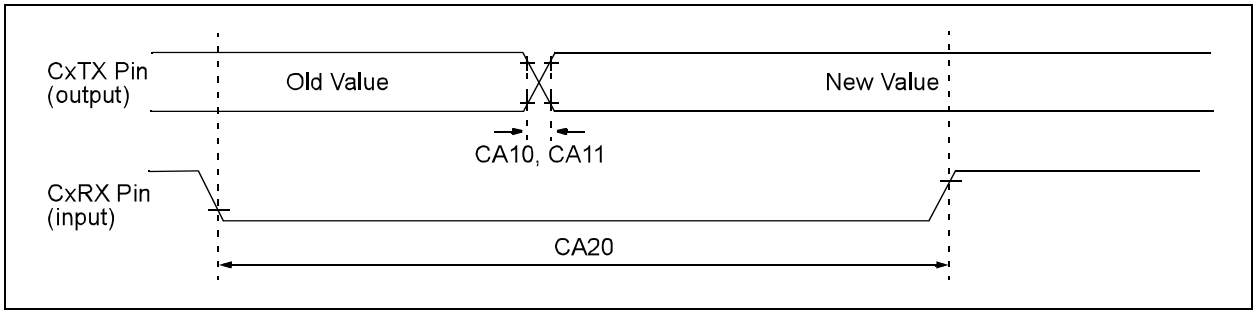


TABLE 30-48: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TIOF	Port Output Fall Time	—	—	—	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time	—	—	—	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 30-33: UARTx MODULE I/O TIMING CHARACTERISTICS

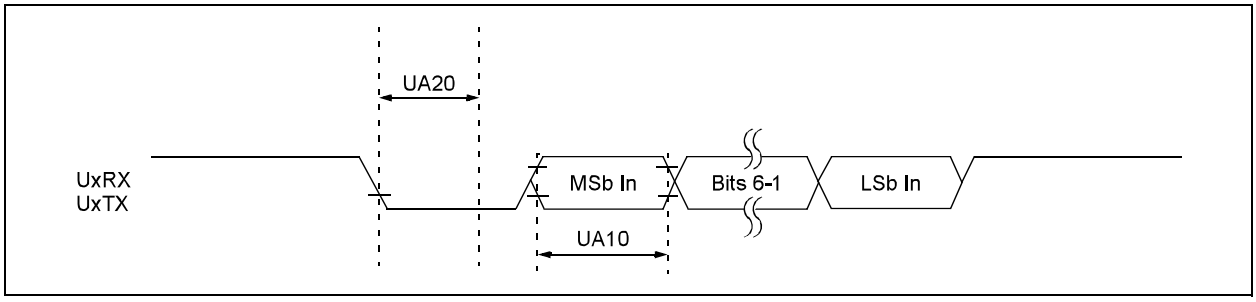


TABLE 30-49: UARTx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 30-50: OP AMP/COMPARATOR x SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Comparator AC Characteristics							
CM10	TRESP	Response Time	—	19	80	ns	V+ input step of 100 mV, V- input held at VDD/2
CM11	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	µs	
Comparator DC Characteristics							
CM30	VOFFSET	Comparator Offset Voltage	-80	±60	80	mV	
CM31	VHYST	Input Hysteresis Voltage	—	30	—	mV	
CM32	TRISE/ TFALL	Comparator Output Rise/Fall Time	—	20	—	ns	1 pF load capacitance on input
CM33	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
Op Amp AC Characteristics							
CM20	SR	Slew Rate	—	9	—	V/µs	10 pF load
CM21	PM	Phase Margin	—	35	—	°C	G = 100V/V, 10 pF load
CM22	GM	Gain Margin	—	20	—	db	G = 100V/V, 10 pF load
CM23	GBW	Gain Bandwidth	—	10	—	MHz	10 pF load
Op Amp DC Characteristics							
CM40	VCMR	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
CM41	CMRR	Common-Mode Rejection Ratio	—	45	—	db	VCM = AVDD/2
CM42	VOFFSET	Op Amp Offset Voltage	-50	±6	50	mV	
CM43	VGAIN	Open-Loop Voltage Gain	—	90	—	db	
CM44	IOS	Input Offset Current	—	—	—	—	See pad leakage currents in Table 30-10
CM45	IB	Input Bias Current	—	—	—	—	See pad leakage currents in Table 30-10
CM46	IOUT	Output Current	—	—	420	µA	With minimum value of RFEEDBACK (CM48)
CM48	RFEEDBACK	Feedback Resistance Value	8	—	—	kΩ	See **Note 2**
CM49a	VOUT	Output Voltage	AVSS + 0.075	—	AVDD – 0.075	V	IOUT = 420 µA

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

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TABLE 30-51: OP AMP/COMPARATOR x VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
VRD310	TSET	Settling Time	—	1	10	µs	See Note 1

Note 1: Settling time measured while CVRSS = 1 and the CVR[6:0] bits transition from '0000000' to '1111111'.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-52: OP AMP/COMPARATOR x VOLTAGE REFERENCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
VRD311	CVRAA	Absolute Accuracy of Internal DAC Input to Comparators	—	±25	—	mV	AVDD = CVRSRC = 5.0V
VRD312	CVRAA1	Absolute Accuracy of CVREFXO Pins	—	—	+35/-65	mV	AVDD = CVRSRC = 5.0V
VRD313	CVRSRC	Input Reference Voltage	0	—	AVDD + 0.3	V	
VRD314	CVROUT	Buffer Output Resistance	—	1.5k	—	Ω	
VRD315	CVCL	Permissible Capacitive Load (CVREFXO pins)	—	—	25	pF	
VRD316	IOCVR	Permissible Current Output (CVREFXO pins)	—	—	1	mA	
VRD317	ION	Current Consumed when Module is Enabled	—	—	500	µA	AVDD = 5.0V
VRD318	IOFF	Current Consumed when Module is Disabled	—	—	1	nA	AVDD = 5.0V

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-53: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU Current Source							
CTMUI1	IOUT1	Base Range	—	550	—	nA	CTMUICON[9:8] = 01
CTMUI2	IOUT2	10x Range	—	5.5	—	µA	CTMUICON[9:8] = 10
CTMUI3	IOUT3	100x Range	—	55	—	µA	CTMUICON[9:8] = 11
CTMUI4	IOUT4	1000x Range	—	550	—	µA	CTMUICON[9:8] = 00
CTMUFV1	VF	Temperature Diode Forward Voltage(1,2)	—	0.525	—	V	TA = +25°C, CTMUICON[9:8] = 01
			—	0.585	—	V	TA = +25°C, CTMUICON[9:8] = 10
			—	0.645	—	V	TA = +25°C, CTMUICON[9:8] = 11
CTMUFV2	VFVR	Temperature Diode Rate of Change(1,2)	—	-1.92	—	mV/°C	CTMUICON[9.8] = 01
			—	-1.74	—	mV/°C	CTMUICON[9:8] = 10
			—	-1.56	—	mV/°C	CTMUICON[9:8] = 11

Note 1: Nominal value at center point of current trim range (CTMUICON[15:10] = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements are taken with the following conditions:

- VREF = AVDD = 5.0V
- ADC configured for 10-bit mode
- ADC configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx = 0)
- CPU executing

```
while(1)
{
NOP();
}
```

- Device operating from the FRC with no PLL

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TABLE 30-54: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or VBOR	—	Lesser of: VDD + 0.3 or 5.5	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	4.5	—	5.5	V	VREFH = AVDD, VREFL = AVSS = 0
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – VBORMIN	V	See Note 1
AD06a			0	—	0	V	VREFH = AVDD, VREFL = AVSS = 0
AD07	VREF	Absolute Reference Voltage	4.5	—	5.5	V	VREF = VREFH – VREFL
AD08	IREF	Current Drain	— —	— —	10 600	µA µA	ADC off ADC on
AD09	IAD	Operating Current	—	5	—	mA	ADC operating in 10-bit mode (see Note 1)
			—	2	—	mA	ADC operating in 12-bit mode (see Note 1)
Analog Input							
AD12	VINH	Input Voltage Range VINH	VINL	—	VREFH	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range VINL	VREFL	—	AVSS + 1V	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	Impedance to achieve maximum performance of ADC

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 30-55: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (12-Bit Mode)							
AD20a	Nr	Resolution	12 data bits			bits	
AD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD22a	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD23a	GERR	Gain Error	-10	4	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD24a	EOFF	Offset Error	-10	1.75	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD25a	—	Monotonicity(2)	—	—	—	—	Guaranteed
Dynamic Performance (12-Bit Mode)							
AD30a	THD	Total Harmonic Distortion	—	—	-75	dB	
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5	—	dB	
AD32a	SFDR	Spurious Free Dynamic Range	80	—	—	dB	
AD33a	FNYQ	Input Signal Bandwidth	—	—	250	kHz	
AD34a	ENOB	Effective Number of Bits	11.09	11.3	—	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: The conversion result never decreases with an increase in the input voltage.

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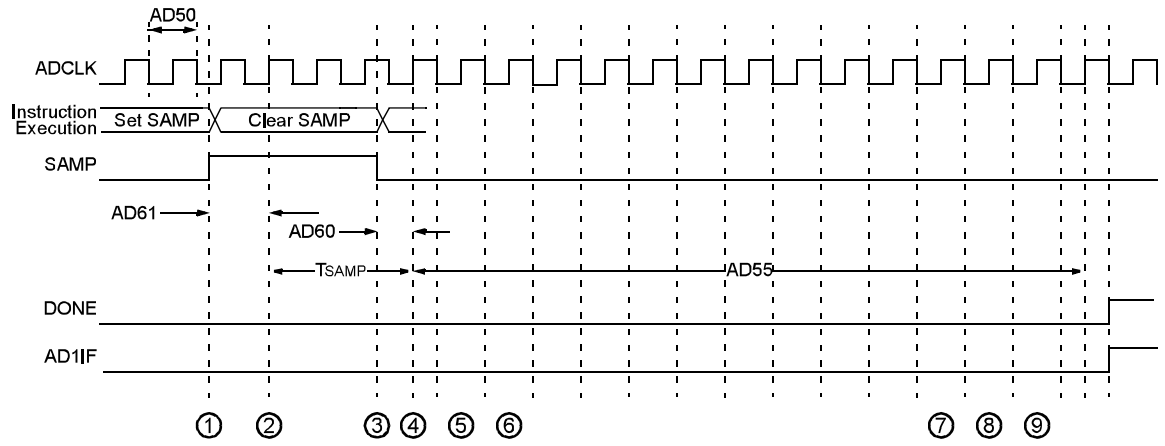
TABLE 30-56: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (10-Bit Mode)							
AD20b	Nr	Resolution	10 data bits			bits	
AD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD22b	DNL	Differential Nonlinearity	≥ 1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD23b	GERR	Gain Error	1	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD24b	EOFF	Offset Error	1	2	4	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
AD25b	—	Monotonicity(2)	—	—	—	—	Guaranteed
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion	—	—	-64	dB	
AD31b	SINAD	Signal to Noise and Distortion	57	58.5	—	dB	
AD32b	SFDR	Spurious Free Dynamic Range	72	—	—	dB	
AD33b	FNYQ	Input Signal Bandwidth	—	—	550	kHz	
AD34b	ENOB	Effective Number of Bits	9.16	9.4	—	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: The conversion result never decreases with an increase in the input voltage.

FIGURE 30-34: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC[2:0] = 000, SSRCG = 0)



1 – Software sets ADxCON1. SAMP to start sampling.

2 – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

3 – Software clears ADxCON1. SAMP to start conversion.

4 – Sampling ends, conversion sequence starts.

5 – Convert bit 11.

6 – Convert bit 10.

7 – Convert bit 1.

8 – Convert bit 0.

9 – One TAD for end of conversion.

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TABLE 30-57: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(4)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	117.6	—	—	ns	
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14	—	TAD	
AD56	FCNV	Throughput Rate	—	—	500	ksps	
AD57a	TSAMP	Sample Time when Sampling Any ANx Input	3	—	—	TAD	
AD57b	TSAMP	Sample Time when Sampling the Op Amp Outputs	3	—	—	TAD	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(1)	2	—	3	TAD	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(1)	2	—	3	TAD	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(1)	—	0.5	—	TAD	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(1)	—	—	20	µs	See Note 3

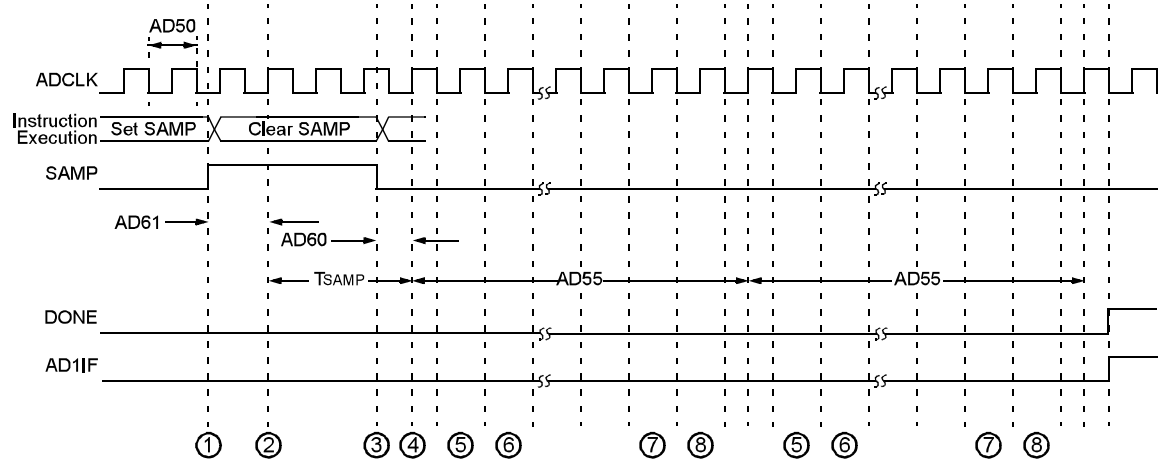
Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

3: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1[15]) = 1). During this time, the ADC result is indeterminate.

4: These parameters are characterized but not tested in manufacturing.

FIGURE 30-35: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS[1:0] = 01, SIMSAM = 0, ASAM = 0, SSRC[2:0] = 000, SSRCG = 0)



① – Software sets ADxCON1. SAMP to start sampling.

② – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

③ – Software clears ADxCON1. SAMP to start conversion.

④ – Sampling ends, conversion sequence starts.

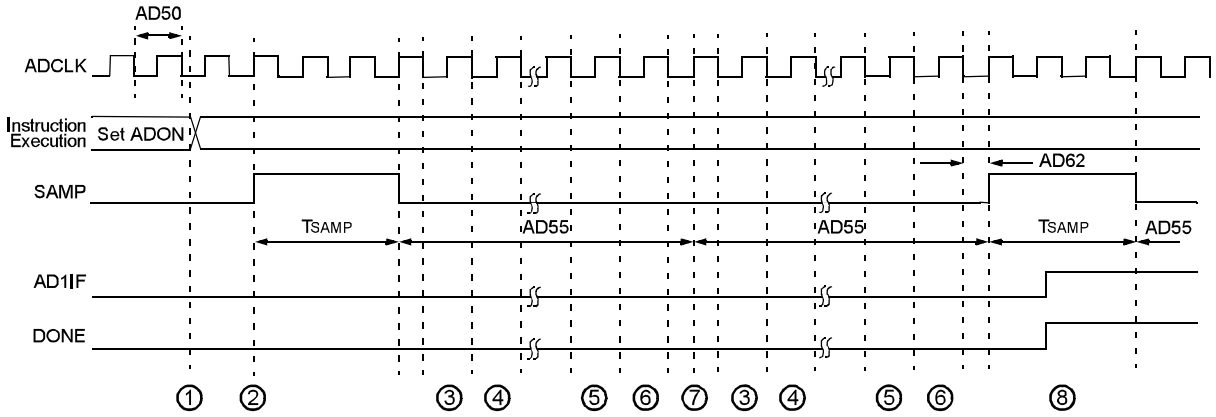
⑤ – Convert bit 9.

⑥ – Convert bit 8.

⑦ – Convert bit 0.

⑧ – One TAD for end of conversion.

FIGURE 30-36: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS[1:0] = 01, SIMSAM = 0, ASAM = 1, SSRC[2:0] = 111, SSRCG = 0, SAMC[4:0] = 00010)



① – Software sets ADxCON1. ADON to start ADC operation.

② – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

③ – Convert bit 9.

④ – Convert bit 8.

⑤ – Convert bit 0.

⑥ – One TAD for end of conversion.

⑦ – Begin conversion of next channel.

⑧ – Sample for time specified by SAMC[4:0].

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TABLE 30-58: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(4)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADC Clock Period	75	—	—	ns	
AD51	tRC	ADC Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	12	—	TAD	
AD56	FCNV	Throughput Rate	—	—	1.1	Msps	Using simultaneous sampling
AD57a	TSAMP	Sample Time When Sampling Any ANx Input	2	—	—	TAD	
AD57b	TSAMP	Sample Time When Sampling the Op Amp Outputs	4	—	—	TAD	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(2)	2	—	3	TAD	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(2)	2	—	3	TAD	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(2)	—	0.5	—	TAD	
AD63	tDPU	Time to Stabilize Analog Stage from ADC Off to ADC On(2)	—	—	20	µs	See Note 3

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

3: The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (ADxCON1[15]) = 1). During this time, the ADC result is indeterminate.

4: These parameters are characterized but not tested in manufacturing.

TABLE 30-59: DMA MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DM1	DMA Byte/Word Transfer Latency	1 TCY(2)	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

NOTES:

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31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of the dsPIC33EVXXXGM00X/10X family electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 30.0 "Electrical Characteristics"** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EVXXXGM00X/10X family high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias(2) ..... -40°C to +150°C
Storage temperature ..... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +6.0V
Maximum current out of V_{SS} pin ..... 350 mA
Maximum current into V_{DD} pin(3) ..... 350 mA
Maximum junction temperature ..... +155°C
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sunk by all ports combined ..... 200 mA
Maximum current sourced by all ports combined(3) ..... 200 mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

2: AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

3: Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

31.1 High-Temperature DC Characteristics

TABLE 31-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Max MIPS
			dsPIC33EVXXXGM00X/10X Family
HDC5	4.5V to 5.5V(1,2)	-40°C to +150°C	40

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Device functionality is tested but is not characterized. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

2: When BOR is enabled, the device will work from 4.7V to 5.5V.

TABLE 31-2: THERMAL OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
High-Temperature Devices					
Operating Junction Temperature Range	TJ	-40	—	+155	°C
Operating Ambient Temperature Range	TA	-40	—	+150	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
Operating Voltage							
HDC10	VDD	**Supply Voltage**(3)	VBOR	—	5.5	V	
HDC12	VDR	**RAM Data Retention Voltage**(2)	1.8	—	—	V	
HDC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
HDC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	1.0	—	—	V/ms	0V-5.0V in 5 ms
HDC18	VCORE	**VDD Core** Internal Regulator Voltage	1.62	1.8	1.98	V	Voltage is dependent on load, temperature and VDD

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: VDD voltage must remain at VSS for a minimum of 200 μs to ensure POR.

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TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Power-Down Current (I_{PD})						
DC60d	9.25	90	µA	-40°C	5V	Base Power-Down Current, Grade 0 Mission Profile
DC60a	15.75	100	µA	+25°C		
DC60b	67.75	465	µA	+85°C		
DC60c	270	860	µA	+125°C		
HDC60e	1300	2500	µA	+150°C		
HDC61c	10	50	µA	+150°C		Watchdog Timer Current: ΔI_{WDT}

TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
HDC40e	2.6	5.0	mA	+150°C	5V	10 MIPS
HDC42e	3.6	7.0	mA	+150°C	5V	20 MIPS

TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (I_{DD})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
HDC20e	5.9	8.0	mA	+150°C	5V	10 MIPS
HDC22e	10.3	15.0	mA	+150°C	5V	20 MIPS
HDC23e	19.0	25.0	mA	+150°C	5V	40 MIPS

TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (I_{DOZE})

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Parameter No.	**Typical**	**Max**	**Doze Ratio**	**Units**	**Conditions**		
HDC73a	18.5	22.0	1:2	mA	+150°C	5V	40 MIPS
HDC73g	8.35	12.0	1:128	mA			

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
DI10	VIL	**Input Low Voltage** Any I/O Pins	VSS	—	0.2 VDD	V	
DI20	VIH	**Input High Voltage** I/O Pins	0.75 VDD	—	5.5	V	
DI30	ICNPU	**Change Notification Pull-up Current**	200	375	600	µA	VDD = 5.0V, VPIN = VSS
DI31	ICNPD	**Change Notification Pull-Down Current(7)**	175	400	625	µA	VDD = 5.0V, VPIN = VDD
DI50	IIL	**Input Leakage Current(2,3)** I/O Pins	-200	—	200	nA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI55		$\overline{MCLR}$	-1.5	—	1.5	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	-300	—	300	nA	VSS ≤ VPIN ≤ VDD, XT and HS modes
DI60a	IICL	**Input Low Injection Current**	0	—	-5(4,6)	mA	All pins except VDD, VSS, AVDD, AVSS, $\overline{MCLR}$, VCAP and RB7
DI60b	IICH	**Input High Injection Current**	0	—	+5(5,6)	mA	All pins except VDD, VSS, AVDD, AVSS, $\overline{MCLR}$, VCAP, RB7 and all 5V tolerant pins(5)
DI60c	∑IICT	**Total Input Injection Current** (sum of all I/O and control pins)	-20(7)	—	+20(7)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL | + | IICH |) ≤ ∑IICT

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: VIL source < (VSS – 0.3). Characterized but not tested.

5: Digital 5V tolerant pins cannot tolerate any "positive" input injection current from input sources > 5.5V.

6: Non-zero injection currents can affect the ADC results by approximately four to six counts.

7: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted, provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

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TABLE 31-9: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	Symbol	Characteristic	Min.(1)	Typ.	Max.	Units	Conditions
HDO16	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	IOL = 8.8 mA, VDD = 5.0V
HDO10	VOL	**Output Low Voltage** 8x Sink Driver Pins(3)	—	—	0.4	V	IOL = 10.8 mA, VDD = 5.0V
HDO26	VOH	**Output High Voltage** 4x Sink Driver Pins(2)	VDD – 0.6	—	—	V	IOH = -8.3 mA, VDD = 5.0V
HDO20	VOH	**Output High Voltage** 8x Sink Driver Pins	VDD – 0.6	—	—	V	IOH = -12.3 mA, VDD = 5.0V

Note 1: Parameters are characterized but not tested.

2: Includes all I/O pins that are not 8x sink driver pins (see below).

3: Includes pins, such as RA3, RA4 and RB[15:10] for 28-pin and 36-pin devices, RA3, RA4, RA9 and RB[15:10] for 44-pin and 48-pin devices, RA4, RA7, RA9, RB[15:10] and RC15 for 64-pin devices.

TABLE 31-10: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	Symbol	Characteristic	Min.(1)	Typ.	Max.	Units	Conditions
HBO10	VBOR	BOR Event on VDD Transition High-to-Low	4.15	4.285	4.4	V	VDD (see **Note 2**, **Note 3** and **Note 4**)

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The VBOR specification is relative to the VDD.

3: The device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but is not characterized.

4: **The start-up VDD must rise above 4.6V.**

TABLE 31-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature				
Param No.	Symbol	Characteristic(1)	Min.	Typ.	Max.	Units	Conditions
		Program Flash Memory					
HD130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C(2)
HD134	TRETD	Characteristic Retention	20	—	—	Year	1000 E/W cycles or less and no other specifications are violated

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to +150°C.

31.2 AC Characteristics and Timing Parameters

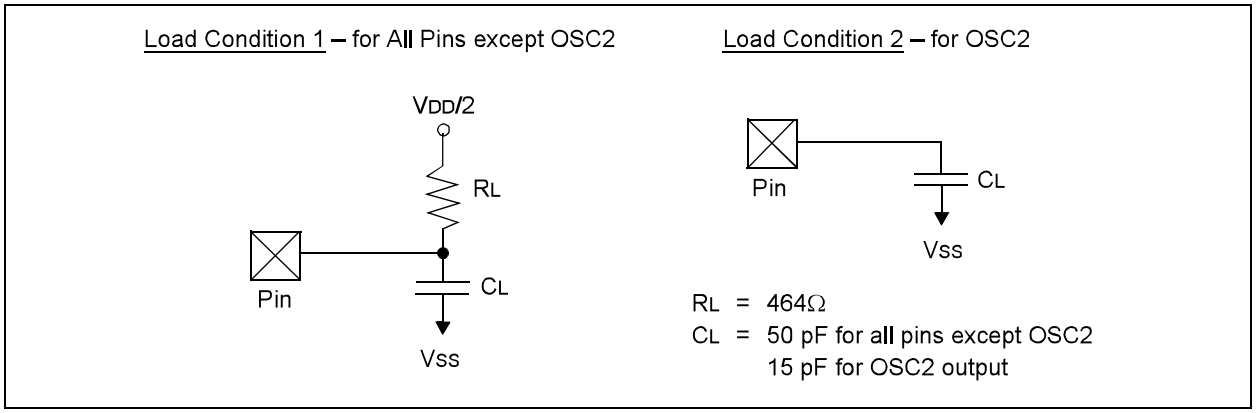
The information contained in this section defines the dsPIC33EVXXXGM00X/10X family AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 "AC Characteristics and Timing Parameters"** is the Industrial and Extended temperature equivalent of HOS53.

TABLE 31-12: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	**Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +150°C Operating voltage VDD range as described in Table 31-1.

FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



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TABLE 31-13: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
HOS50	FPLLI	PLL Voltage Controlled Oscillator (VCO) Input Frequency Range	0.8	—	8.0	MHz	ECPLL, XTPLL modes
HOS51	FSYS	On-Chip VCO System Frequency	120	—	340	MHz	
HOS52	TLOCK	PLL Start-up Time (Lock Time)	0.9	1.5	3.1	ms	
HOS53	DCLK	CLKO Stability (Jitter)(2)	-3	0.5	3	%	

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

TABLE 31-14: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz							
HF20C	FRC	-3	1	+3	%	-40°C ≤ TA ≤ +150°C	VDD = 4.5V to 5.5V

TABLE 31-15: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
LPRC @ 32.768 kHz(1,2)							
HF21C	LPRC	-30	10	+30	%	-40°C ≤ TA ≤ +150°C	VDD = 4.5V to 5.5V

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 27.5 "Watchdog Timer (WDT)"** for more information.

TABLE 31-16: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU Current Source							
HCTMUI1	IOUT1	Base Range	—	550	—	nA	CTMUICON[9.8] = 01
HCTMUI2	IOUT2	10x Range	—	5.5	—	µA	CTMUICON[9.8] = 10
HCTMUI3	IOUT3	100x Range	—	55	—	µA	CTMUICON[9.8] = 11
HCTMUI0	IOUT4	1000x Range	—	550	—	µA	CTMUICON[9.8] = 00
HCTMUFV1	VF	Temperature Diode Forward Voltage(2)	—	0.525	—	V	TA = +25°C, CTMUICON[9.8] = 01
			—	0.585	—	V	TA = +25°C, CTMUICON[9.8] = 10
			—	0.645	—	V	TA = +25°C, CTMUICON[9.8] = 11

Note 1: Normal value at center point of current trim range (CTMUICON[15:10] = 000000).

2: Parameters are characterized but not tested in manufacturing. Measurements are taken with the following conditions:

- VREF = AVDD = 5.0V
- ADC module configured for 10-bit mode
- ADC module configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx = 0)
- CPU executing

```
while(1)
{
NOP();
}
```

- Device operating from the FRC with no PLL

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TABLE 31-17: OP AMP/COMPARATOR x SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min.	Typ.(1)	Max.	Units	Conditions
Comparator DC Characteristics							
HCM30	VOFFSET	Comparator Offset Voltage	-80	±60	80	mV	
HCM31	VHYST	Input Hysteresis Voltage	—	30	—	mV	
HCM34	VICM	Input Common-Mode Voltage	AVSS	—	AVDD	V	
Op Amp DC Characteristics(2)							
HCM40	VCMR	Common-Mode Input Voltage Range	AVSS	—	AVDD	V	
HCM42	VOFFSET	Op Amp Offset Voltage	-50	±6	50	mV	

Note 1: Data in "Typ." column are at 5.0V, +25°C unless otherwise stated.

2: Resistances can vary by ±10% between op amps.

3: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter HBO10 in Table 31-10 for the minimum and maximum BOR values.

TABLE 31-18: ADC MODULE SPECIFICATIONS (12-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (12-Bit Mode)							
HAD20a	Nr	Resolution	12 data bits			bits	
HAD21a	INL	Integral Nonlinearity	-2	—	+2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
HAD22a	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
HAD23a	GERR	Gain Error	-10	4	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
HAD24a	EOFF	Offset Error	-10	1.75	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 30-12 for the minimum and maximum BOR values.

TABLE 31-19: ADC MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 4.5V to 5.5V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (10-Bit Mode)							
HAD20b	Nr	Resolution	10 data bits			bits	
HAD21b	INL	Integral Nonlinearity	-1.5	—	+1.5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
HAD22b	DNL	Differential Nonlinearity	≥ 1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
HAD23b	GERR	Gain Error	1	3	6	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V
HAD24b	EOFF	Offset Error	1	2	4	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 5.5V

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but is not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter HBO10 in Table 31-10 for the minimum and maximum BOR values.

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32.0 CHARACTERISTICS FOR INDUSTRIAL/EXTENDED TEMPERATURE DEVICES (-40°C TO +125°C)

32.1 IDD

FIGURE 32-1: TYPICAL/MAXIMUM IDD vs. FOSC (EC MODE, 10 MHz TO 70 MHz, 5.5V MAX)

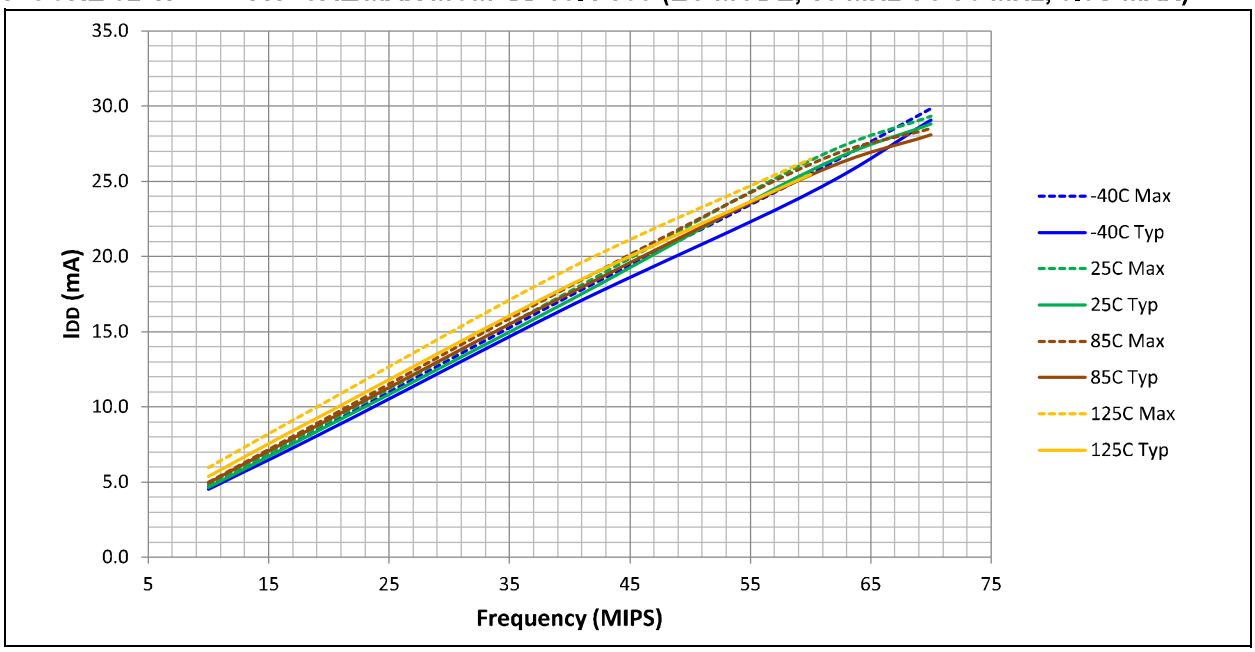


FIGURE 32-2: TYPICAL IDD vs. VDD (EC MODE, 10 MIPS)

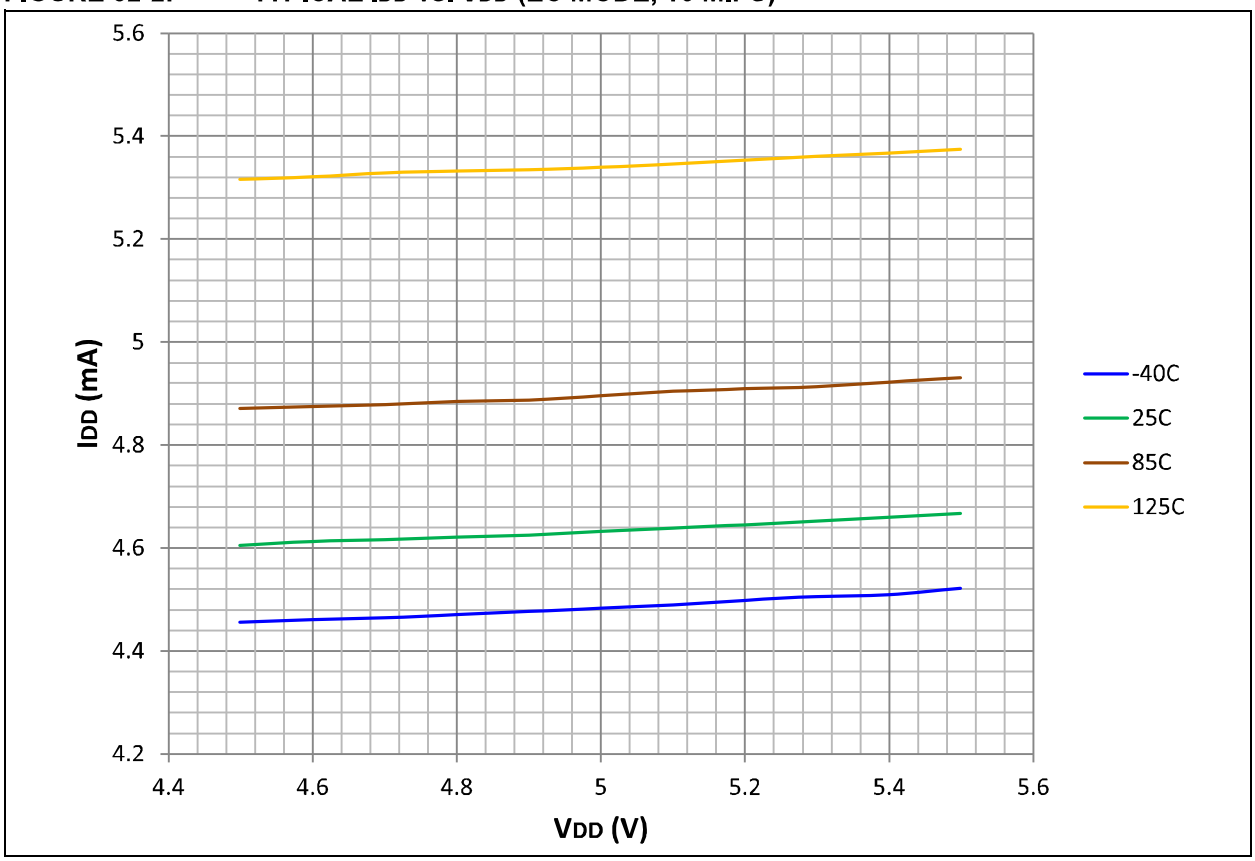


FIGURE 32-3: TYPICAL IDD vs. VDD (EC MODE, 20 MIPS)

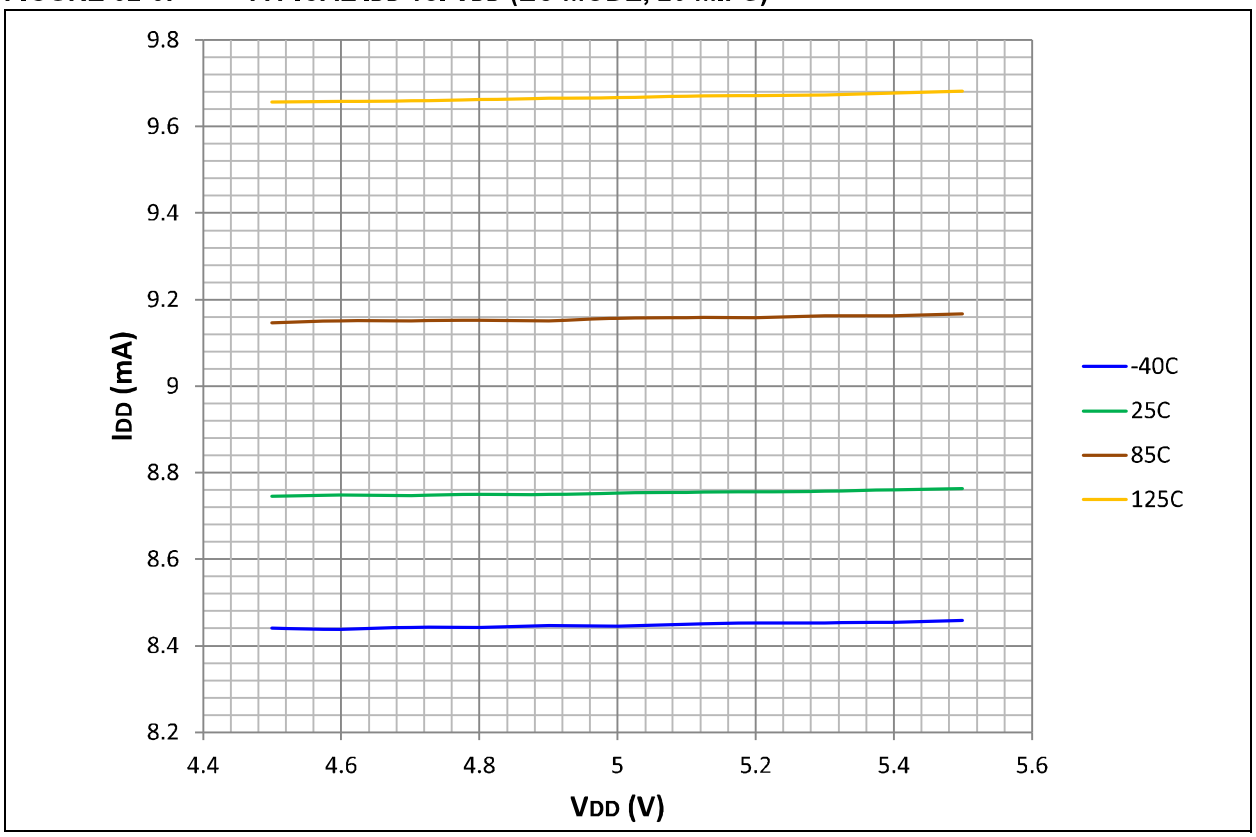
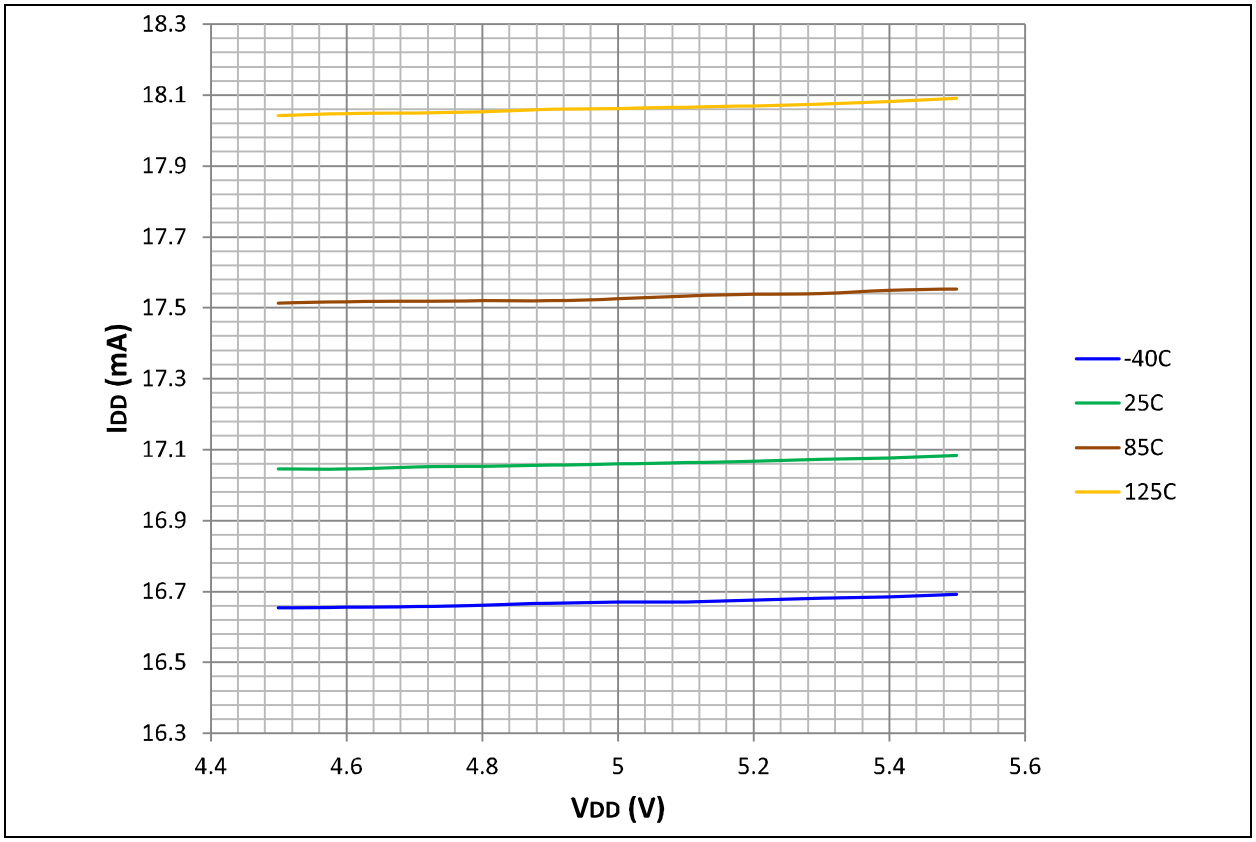


FIGURE 32-4: TYPICAL IDD vs. VDD (EC MODE, 40 MIPS)



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FIGURE 32-5: TYPICAL IDD vs. VDD (EC MODE, 60 MIPS)

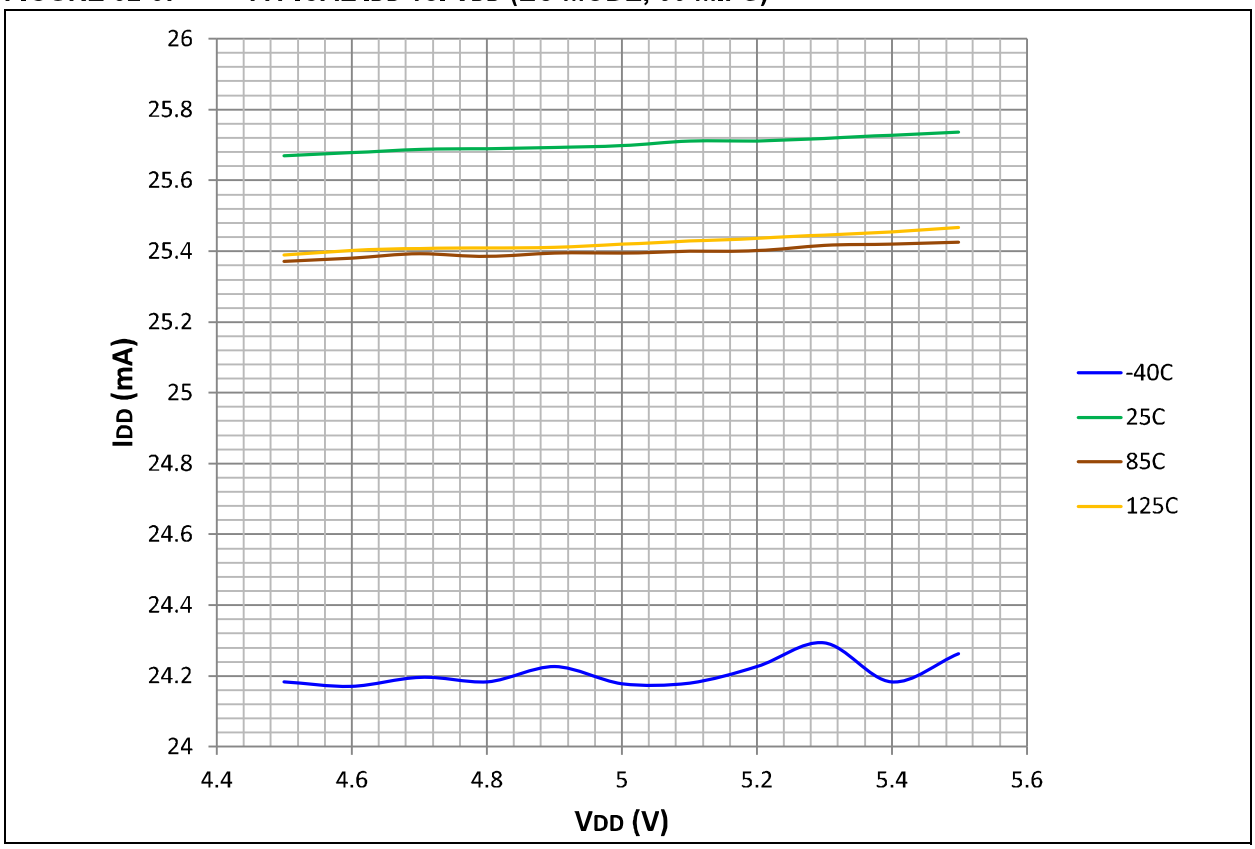
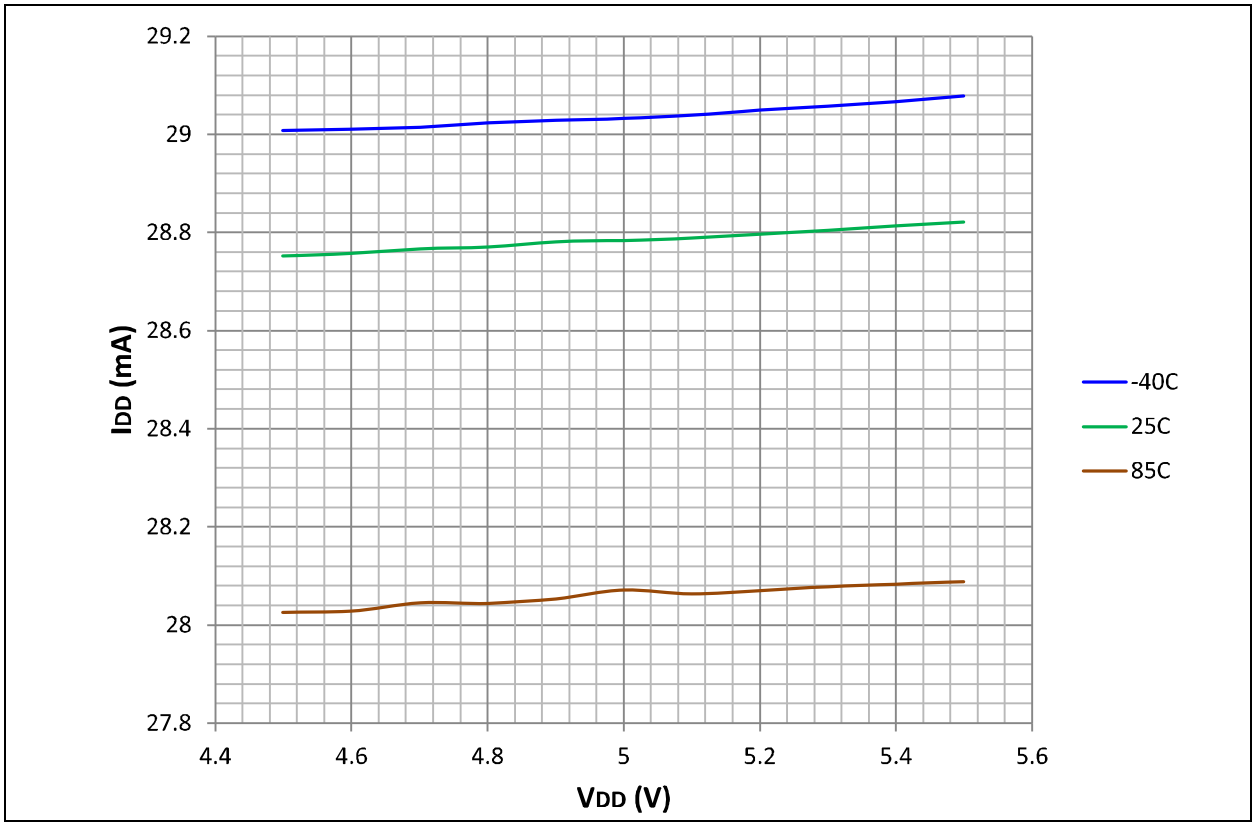


FIGURE 32-6: TYPICAL IDD vs. VDD (EC MODE, 70 MIPS)



32.2 IIDLE

FIGURE 32-7: TYPICAL/MAXIMUM IIDLE vs. FOSC (EC MODE 10 MHz TO 70 MHz, 5.5V MAX)

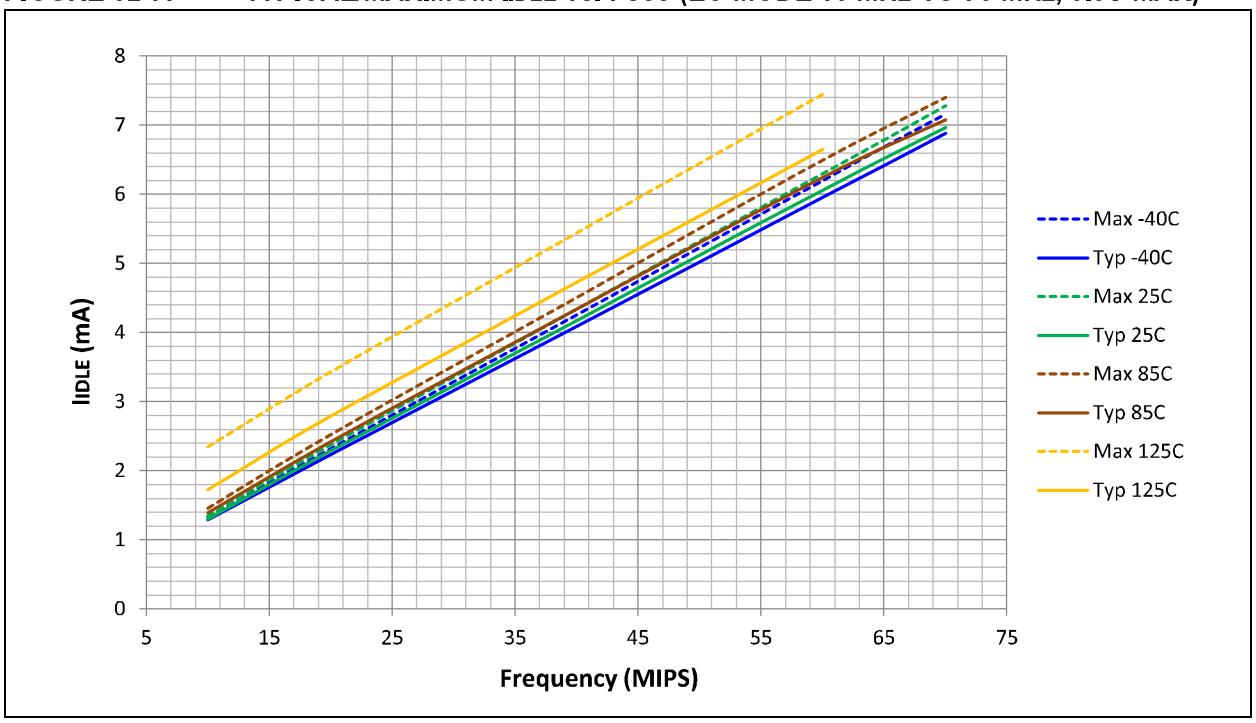
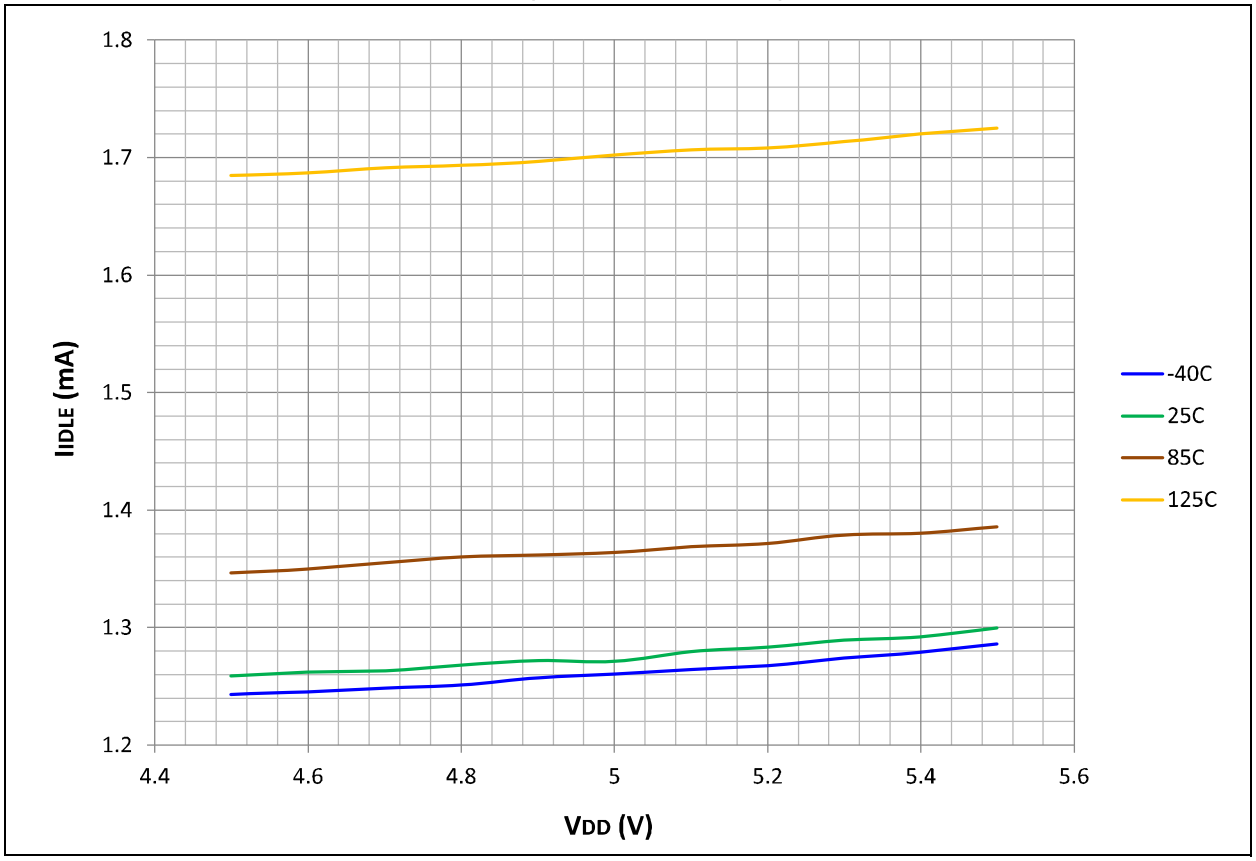


FIGURE 32-8: TYPICAL IIDLE vs. VDD (EC MODE, 10 MIPS)



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FIGURE 32-9: TYPICAL IIDLE vs. VDD (EC MODE, 20 MIPS)

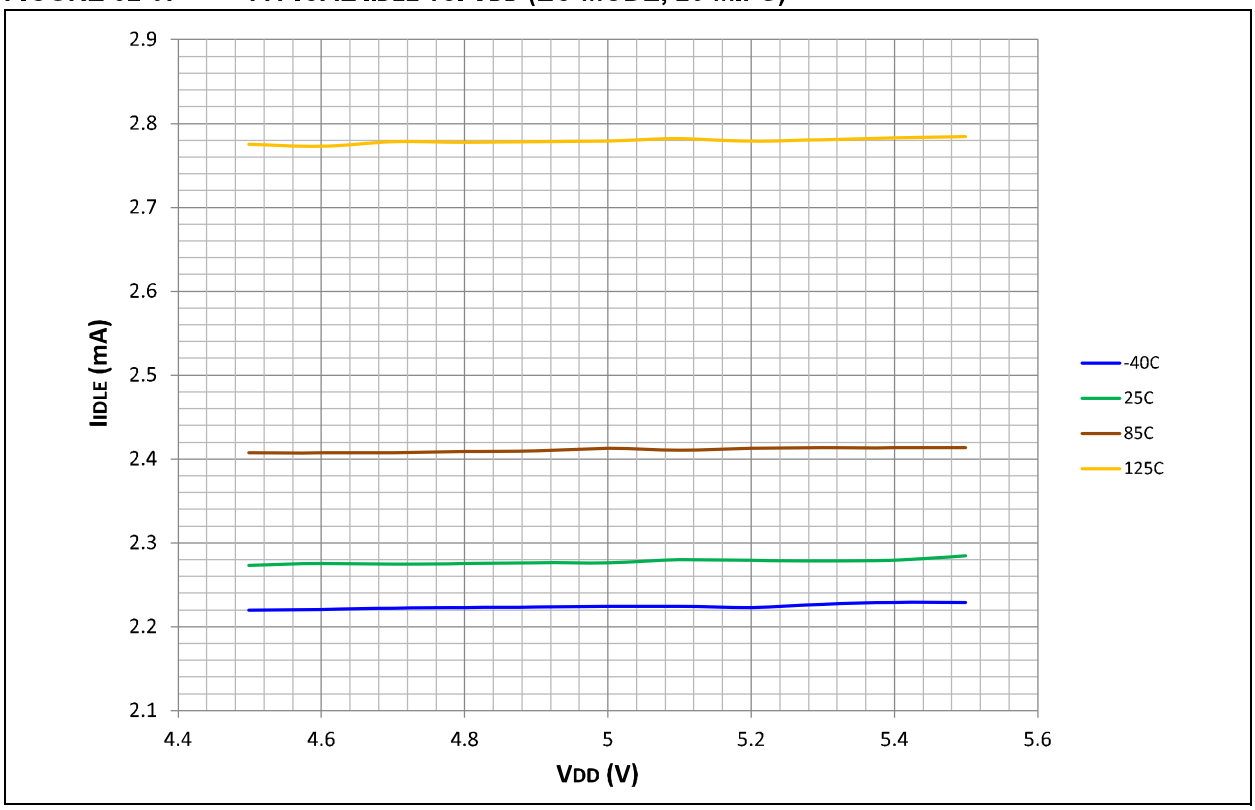


FIGURE 32-10: TYPICAL IIDLE vs. VDD (EC MODE, 40 MIPS)

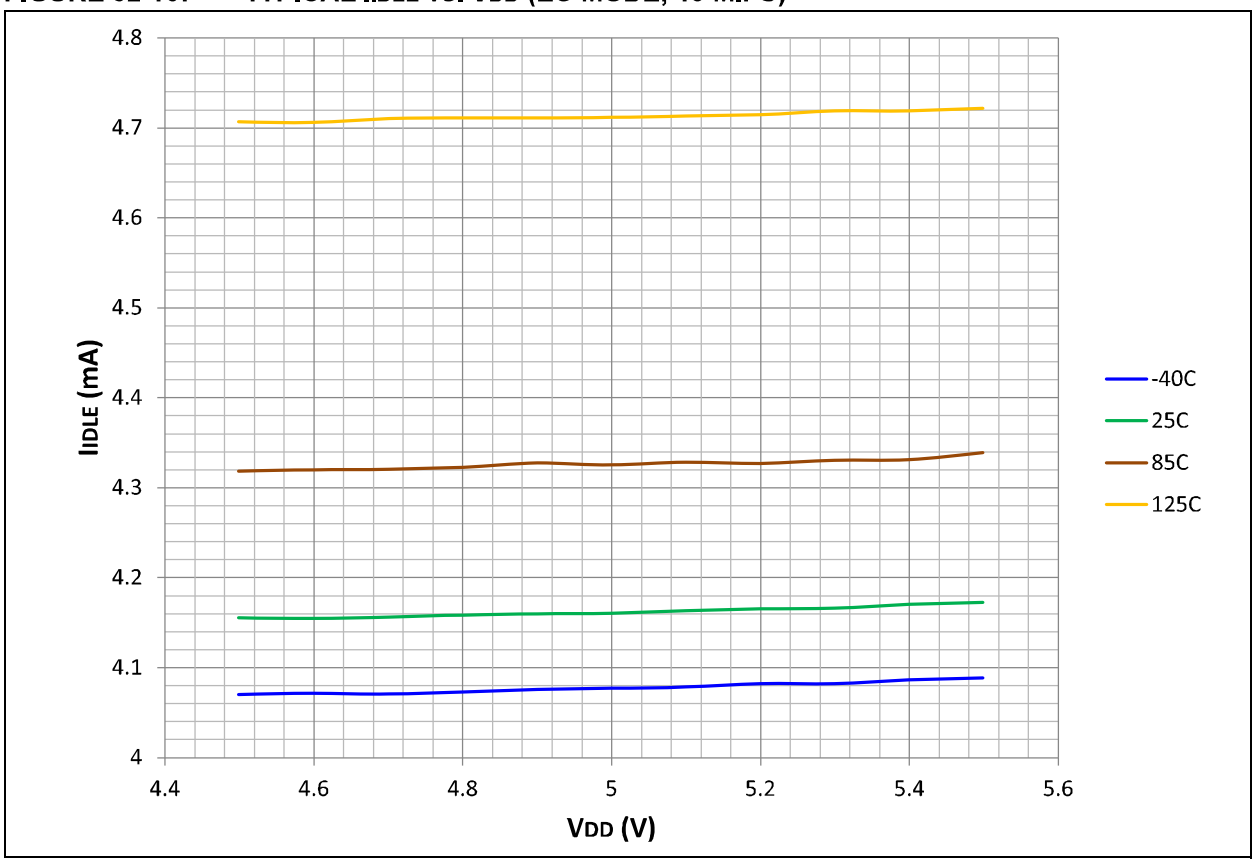


FIGURE 32-11: TYPICAL IIDLE vs. VDD (EC MODE, 60 MIPS)

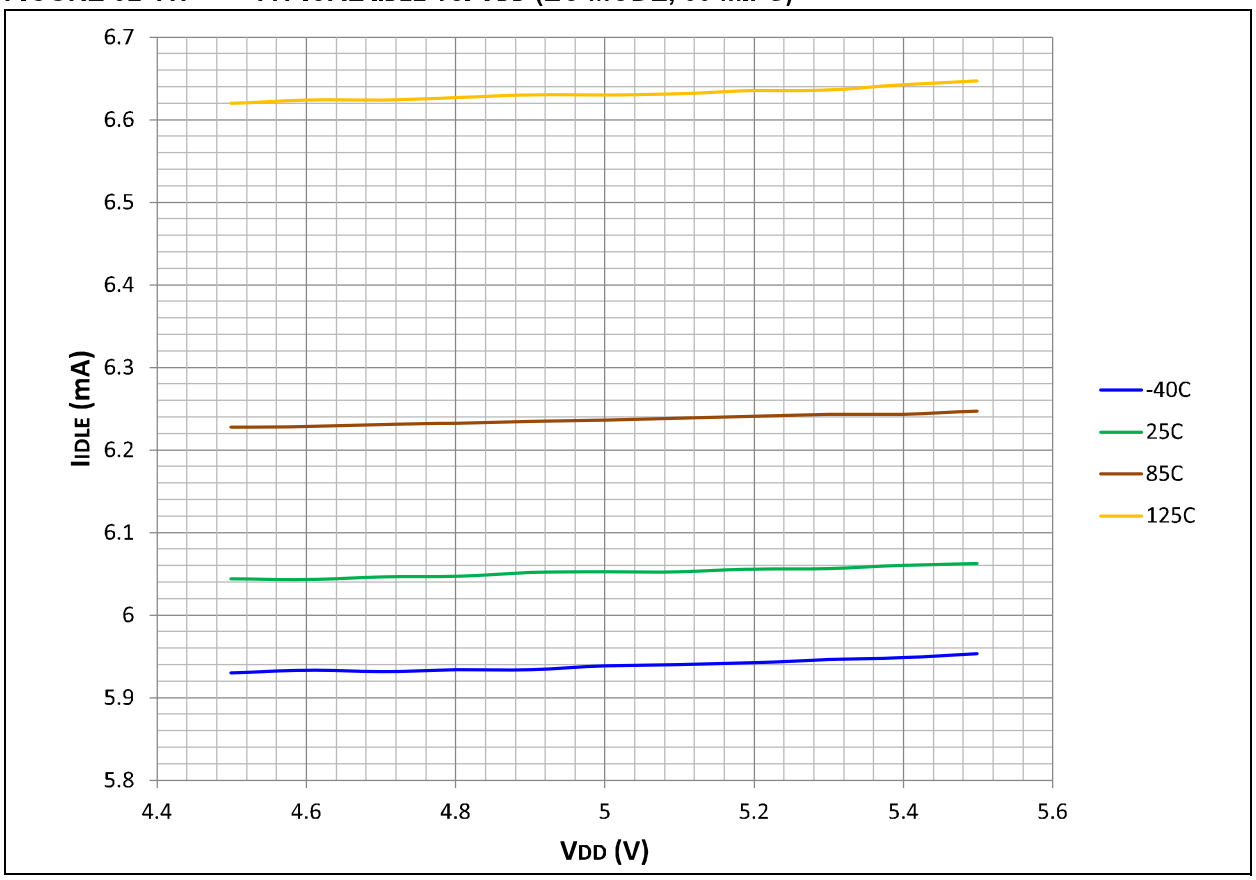
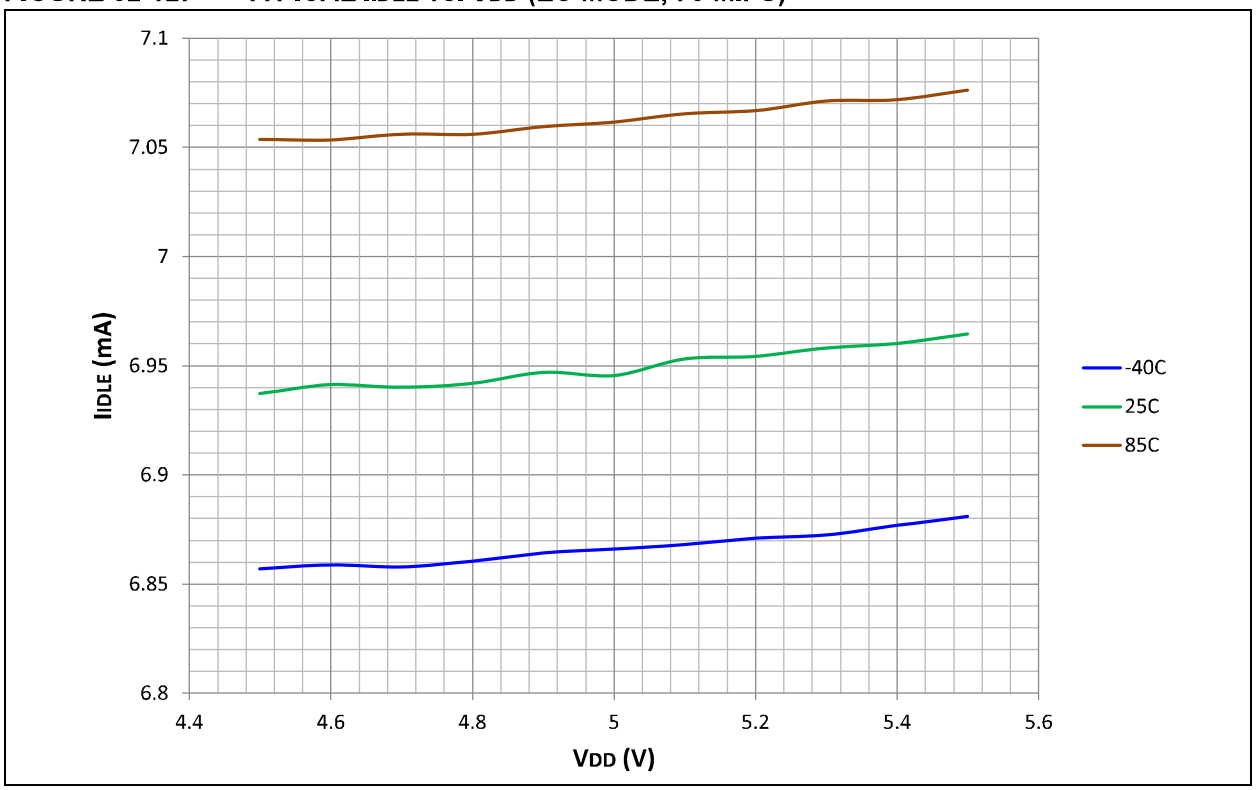


FIGURE 32-12: TYPICAL IIDLE vs. VDD (EC MODE, 70 MIPS)



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32.3 IDOZE

FIGURE 32-13: TYPICAL IDOZE vs. VDD (DOZE 1:2, 70 MIPS)

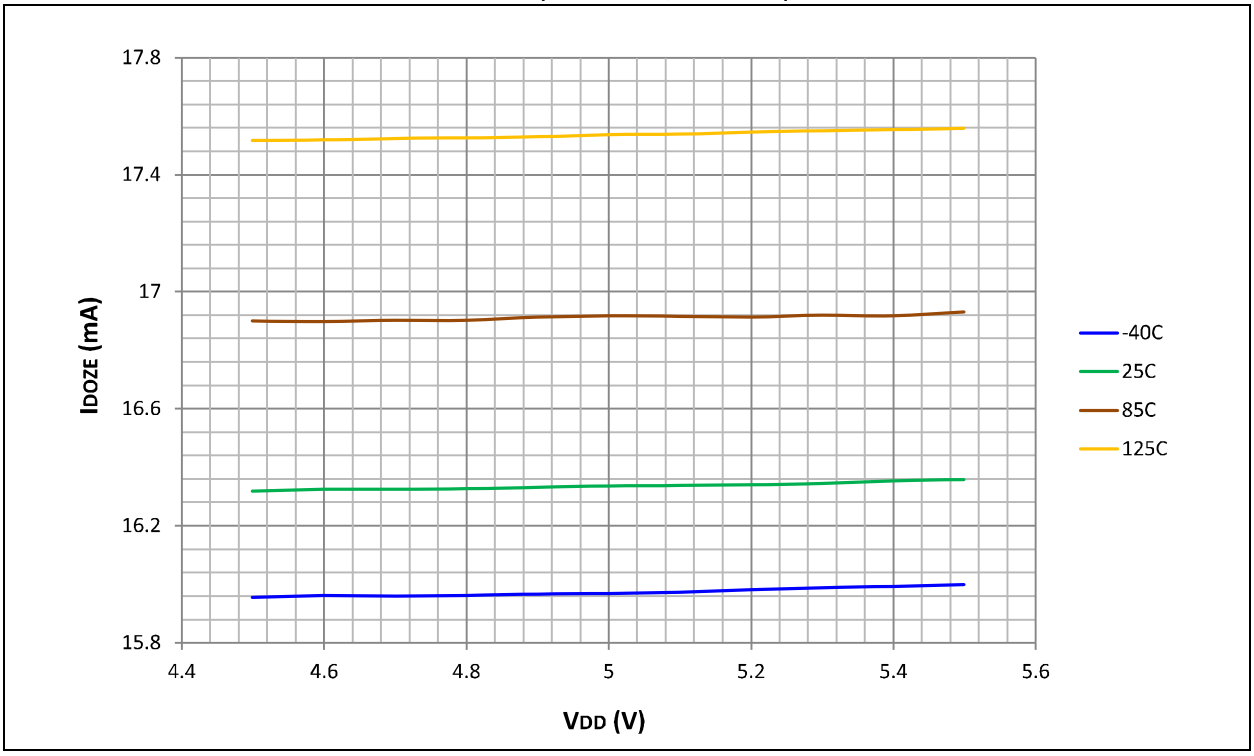


FIGURE 32-14: TYPICAL/MAXIMUM IDOZE vs. TEMPERATURE (DOZE 1:2, 70 MIPS)

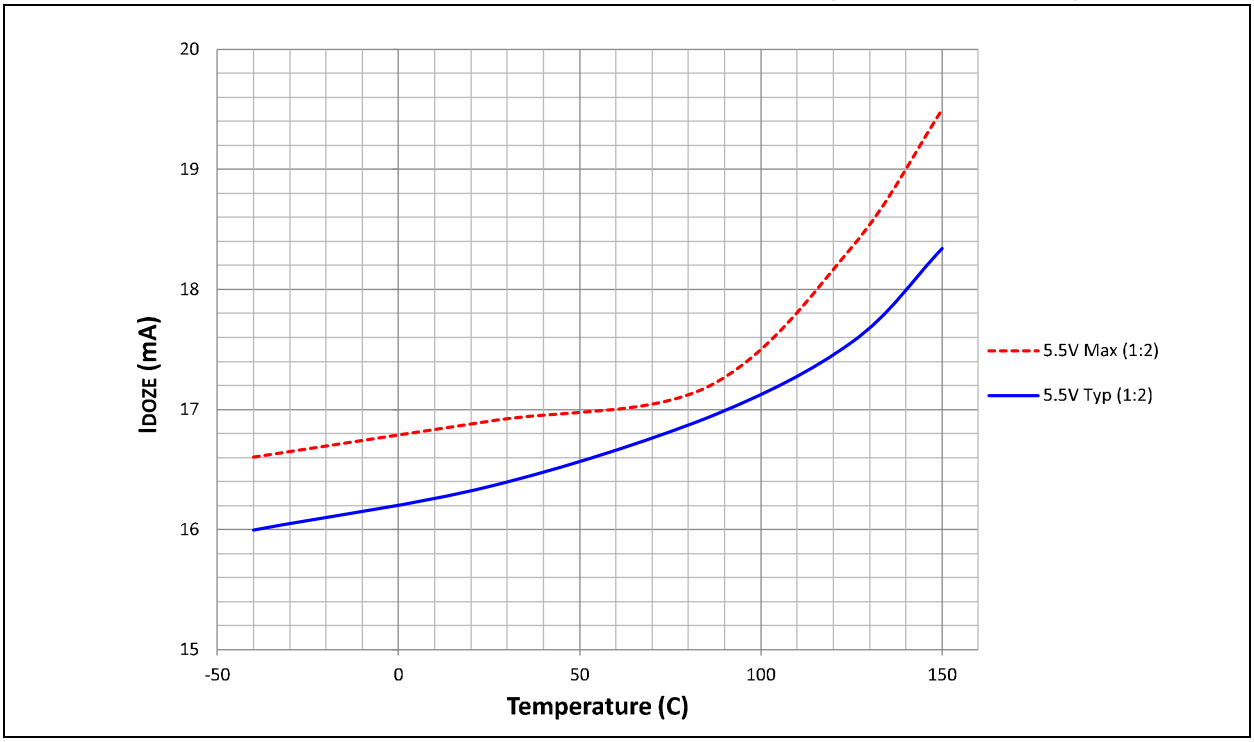


FIGURE 32-15: TYPICAL IDOZE vs. VDD (DOZE 1:128, 70 MIPS)

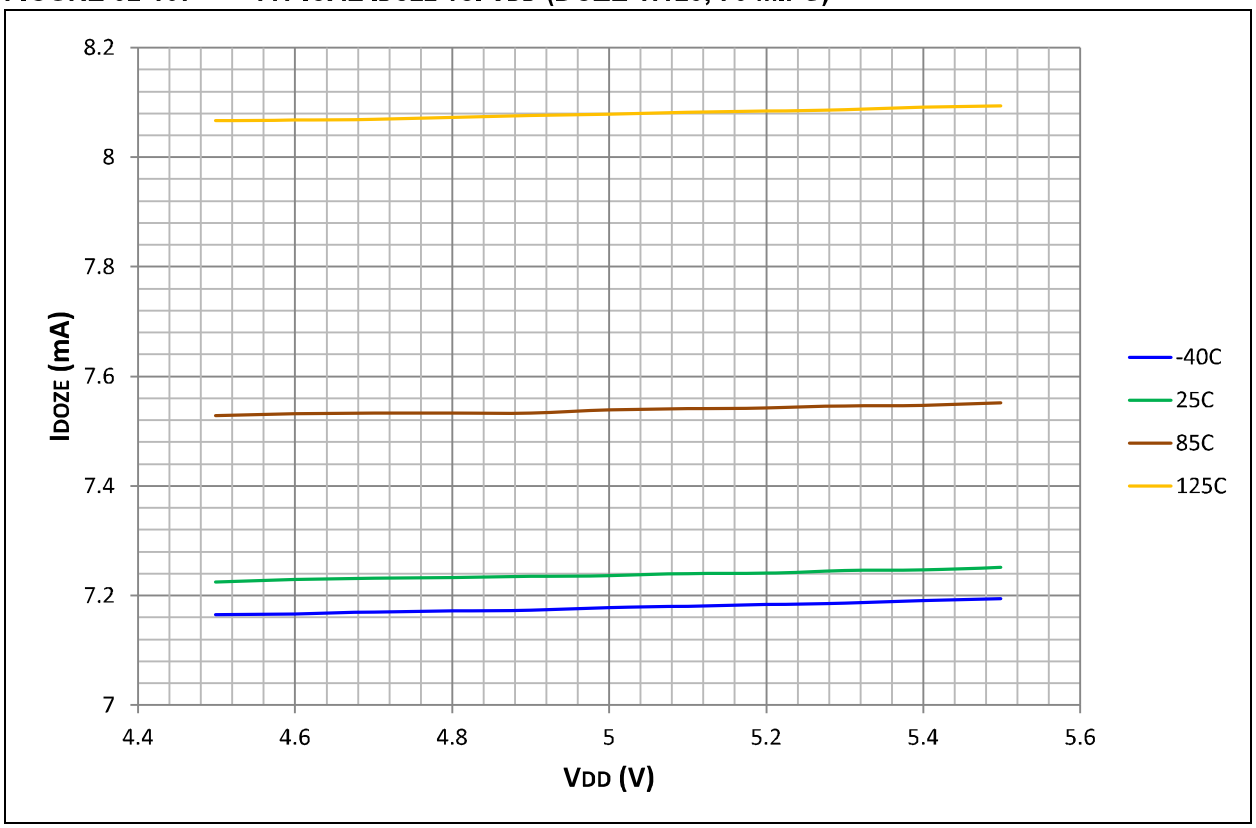
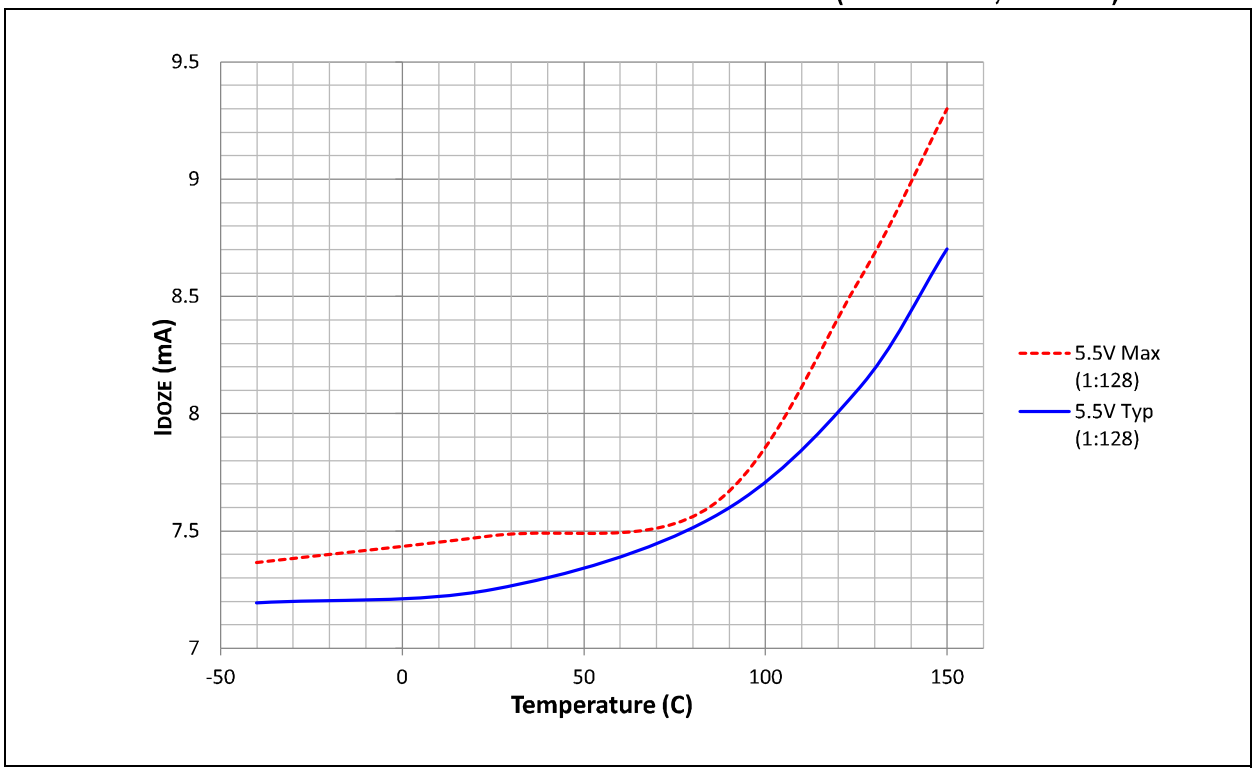


FIGURE 32-16: TYPICAL/MAXIMUM IDOZE vs. TEMPERATURE (DOZE 1:128, 70 MIPS)



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32.4 IPD

FIGURE 32-17: TYPICAL IPD vs. VDD

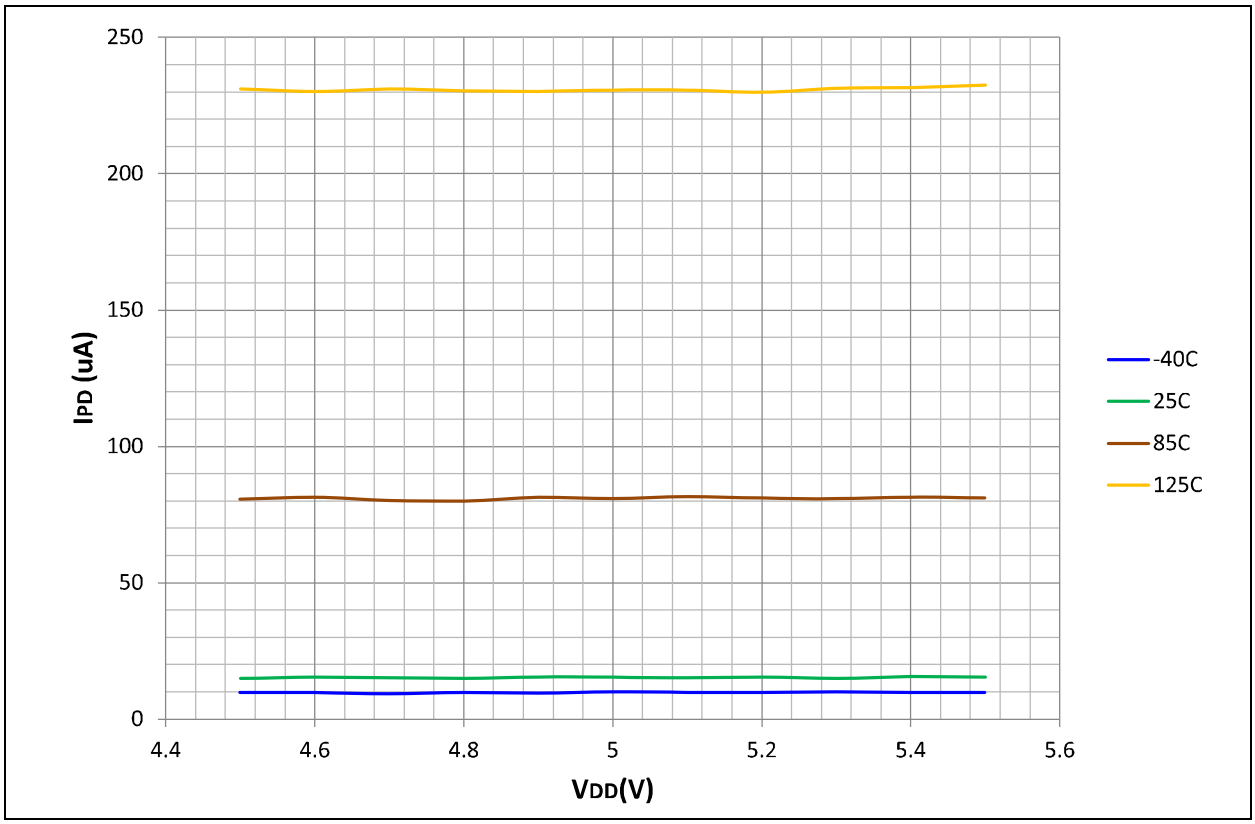


FIGURE 32-18: TYPICAL/MAXIMUM IPD vs. TEMPERATURE

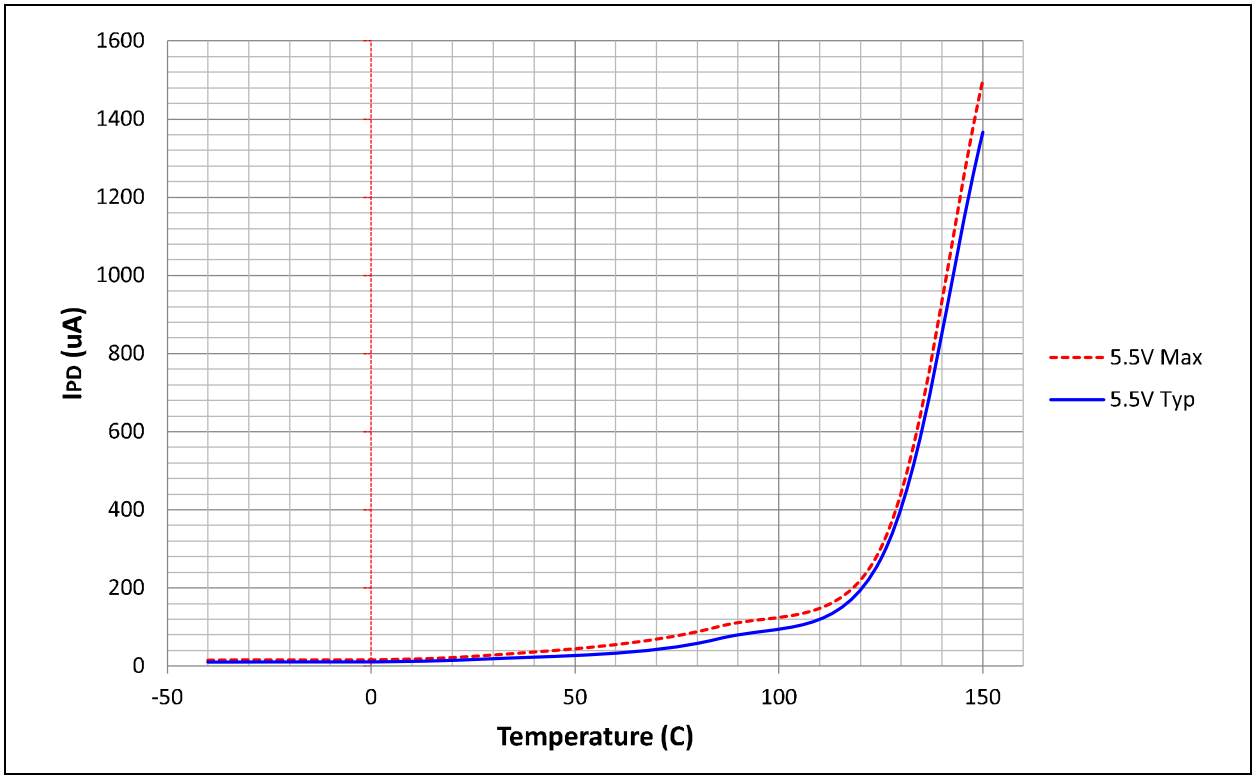
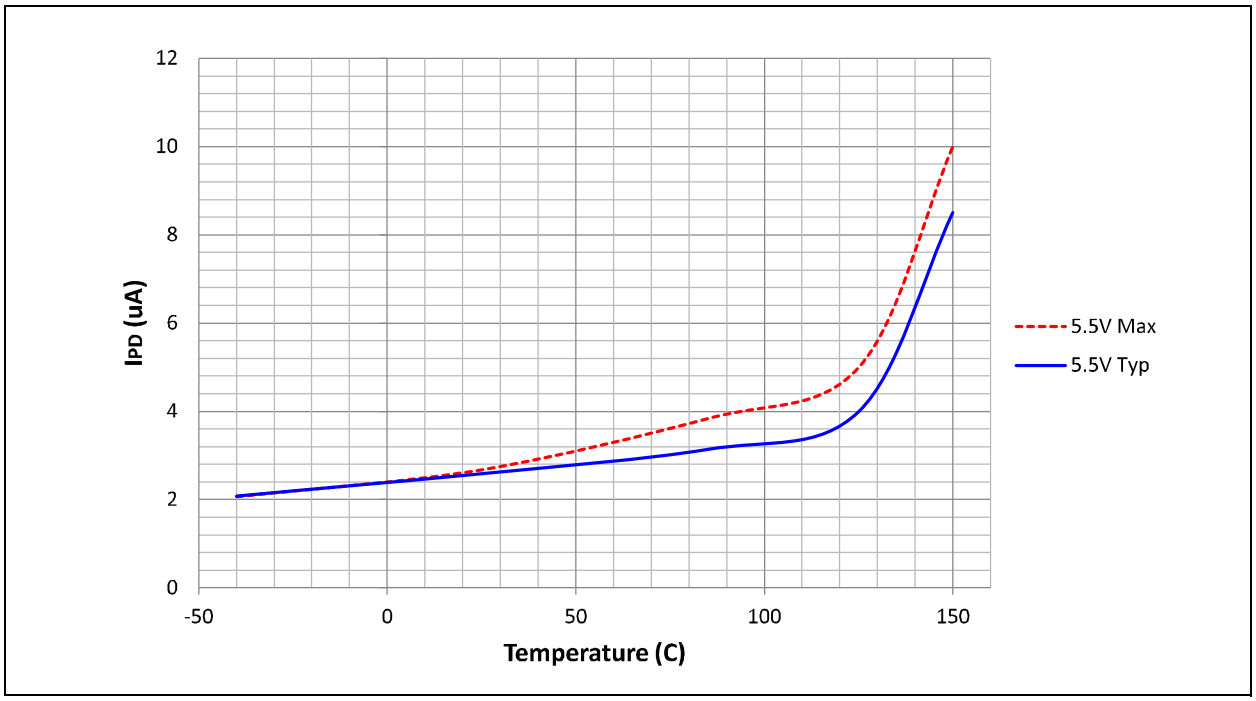
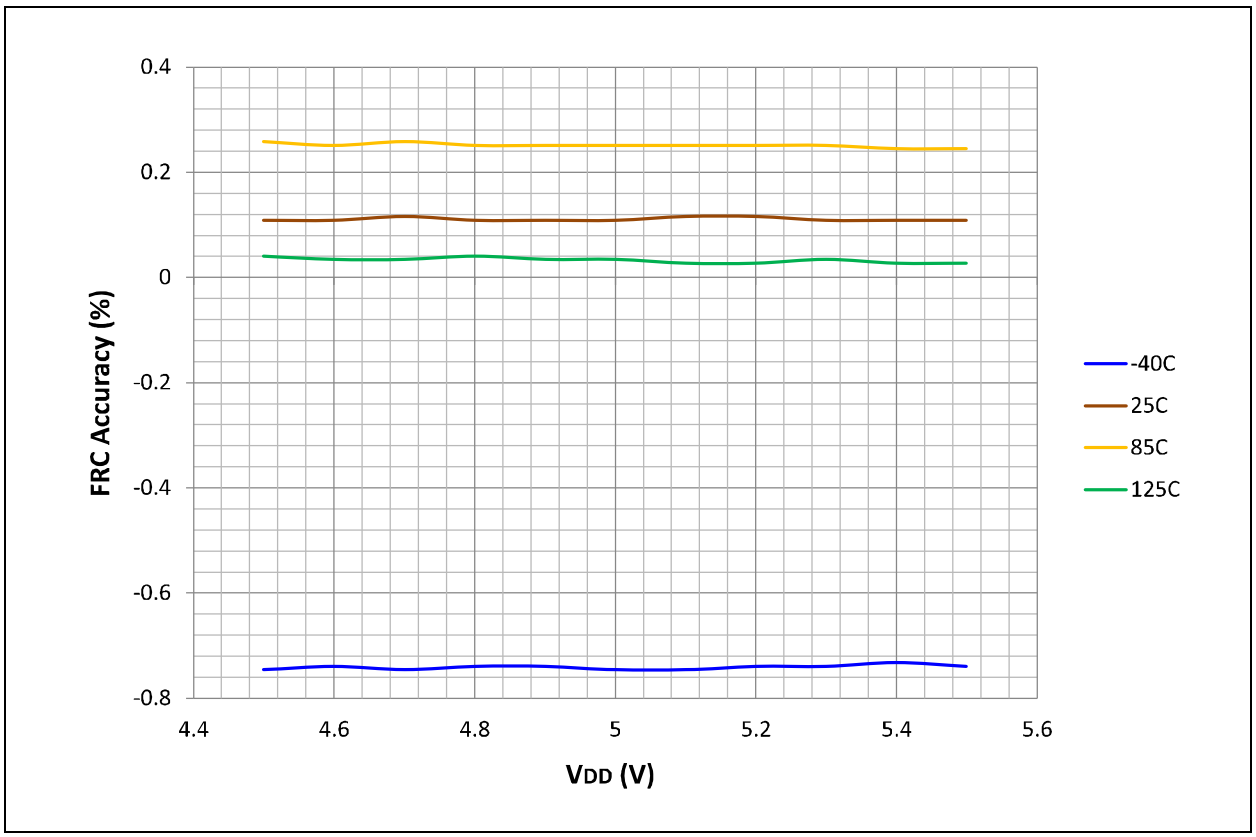


FIGURE 32-19: TYPICAL/MAXIMUM ΔIWDT vs. TEMPERATURE



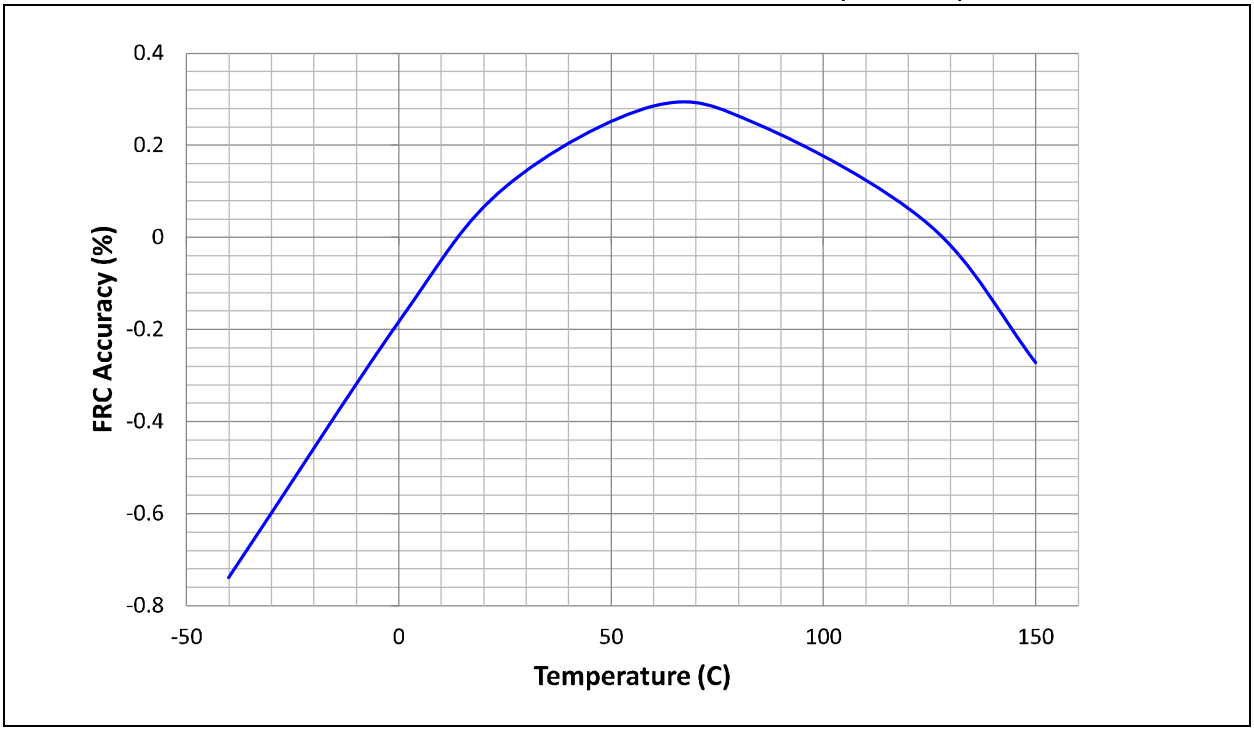
32.5 FRC

FIGURE 32-20: TYPICAL FRC ACCURACY vs. VDD



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FIGURE 32-21: TYPICAL FRC ACCURACY vs. TEMPERATURE (5.5V VDD)



32.6 LPRC

FIGURE 32-22: TYPICAL LPRC ACCURACY vs. VDD

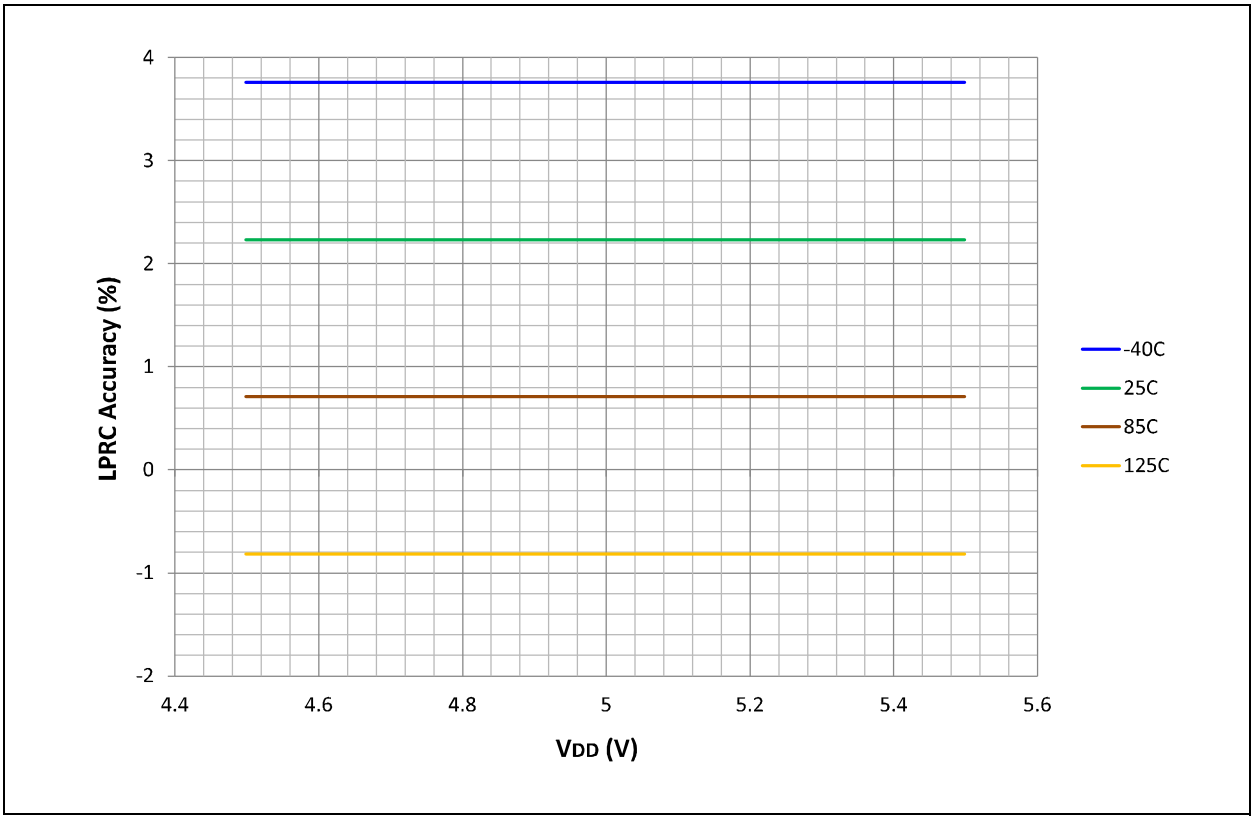
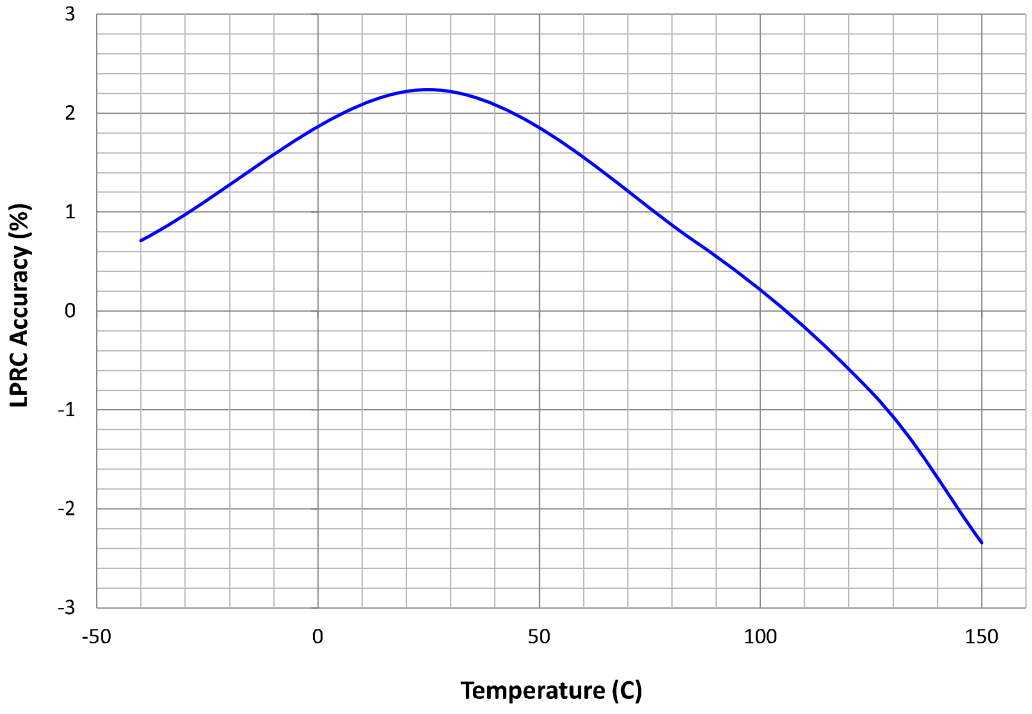
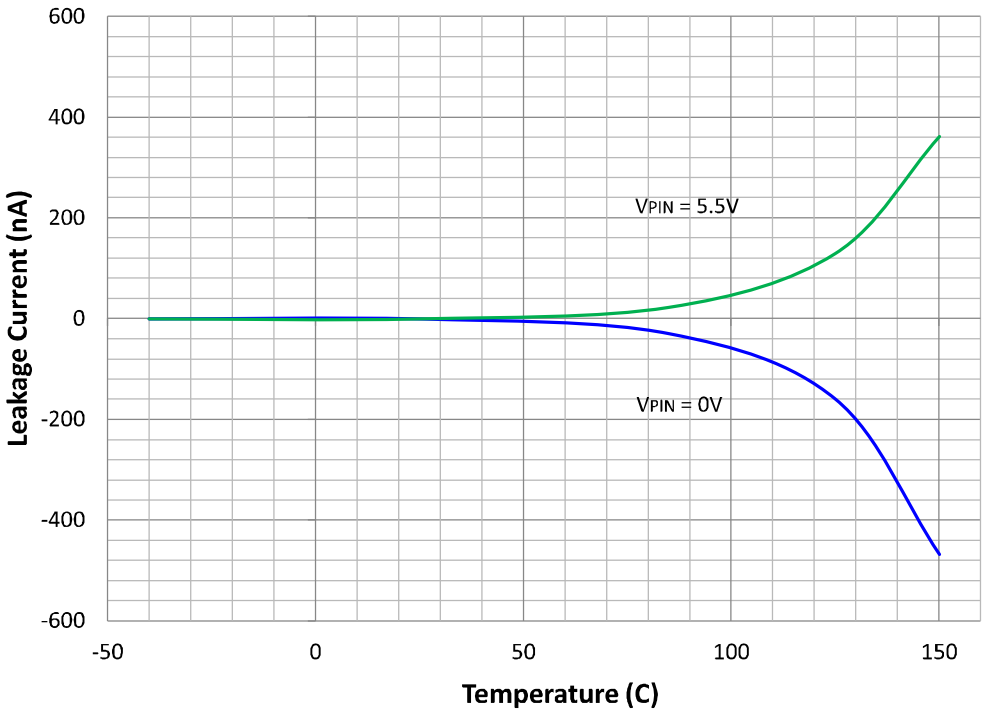


FIGURE 32-23: TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V VDD)



32.7 Leakage Current

FIGURE 32-24: TYPICAL IIL vs. TEMPERATURE ($\overline{MCLR}$)



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FIGURE 32-25: TYPICAL I_{IL} vs. TEMPERATURE (OSC1)

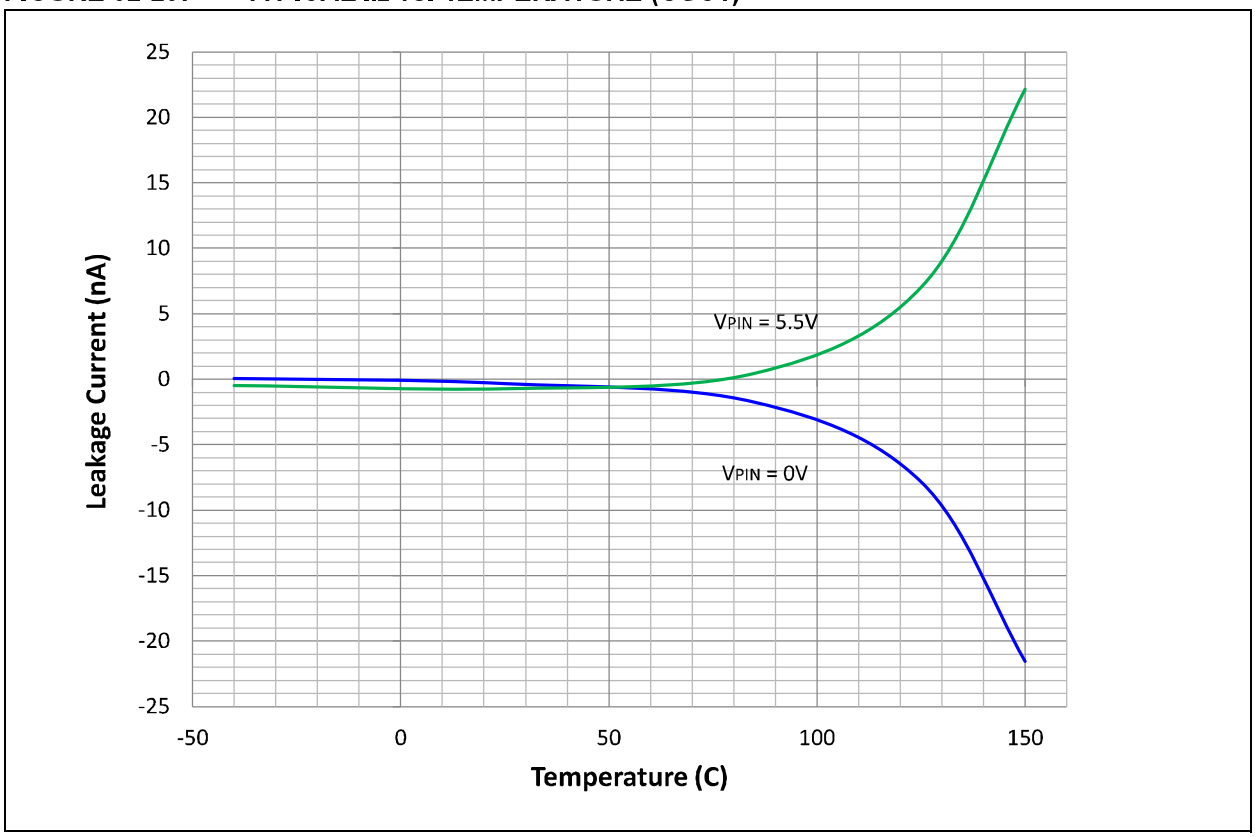
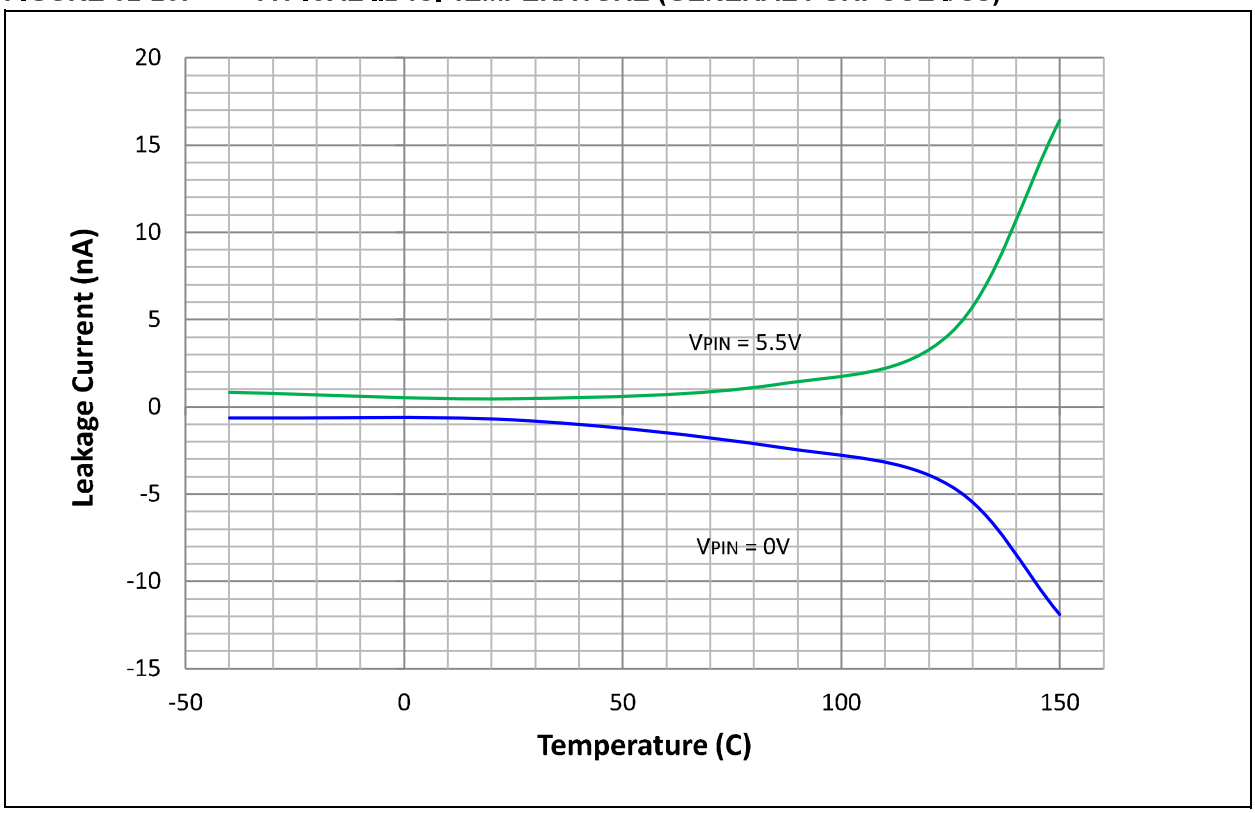


FIGURE 32-26: TYPICAL I_{IL} vs. TEMPERATURE (GENERAL PURPOSE I/Os)



32.8 Pull-up and Pull-Down Current

FIGURE 32-27: TYPICAL PULL-UP CURRENT (V_{PIN} = V_{SS}) vs. TEMPERATURE

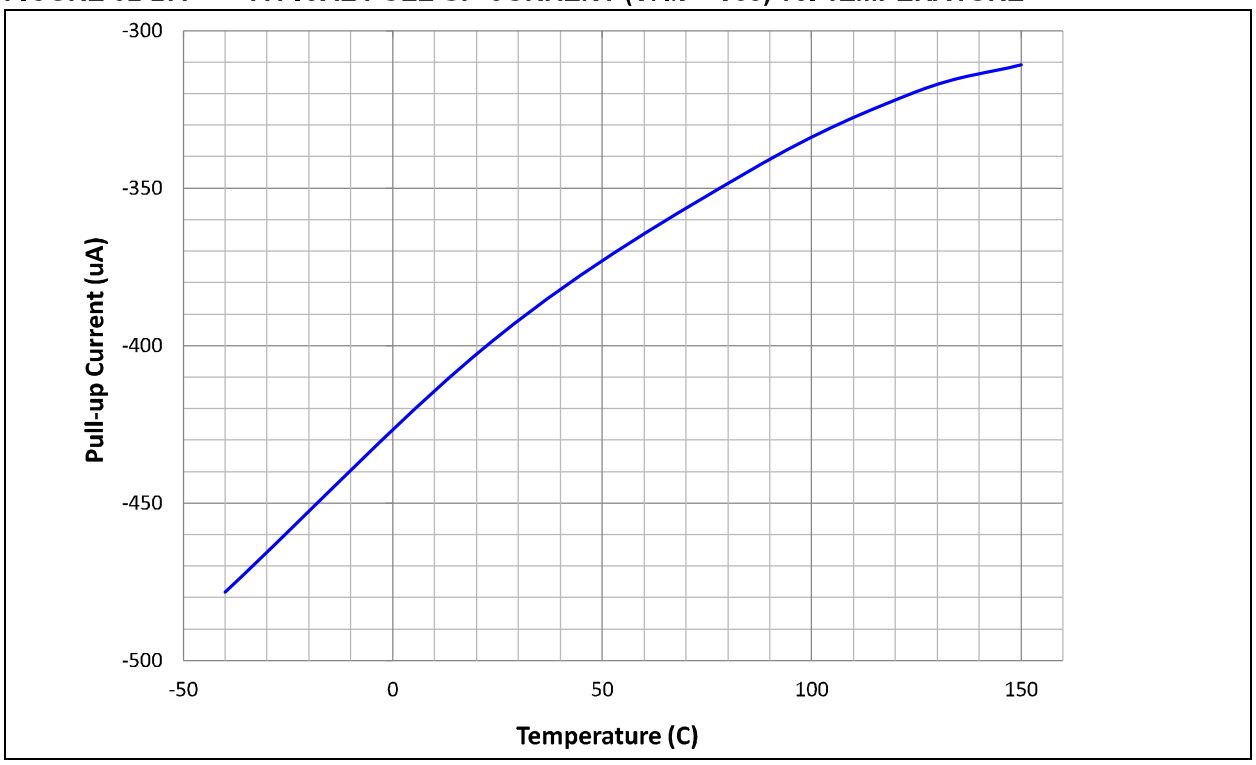
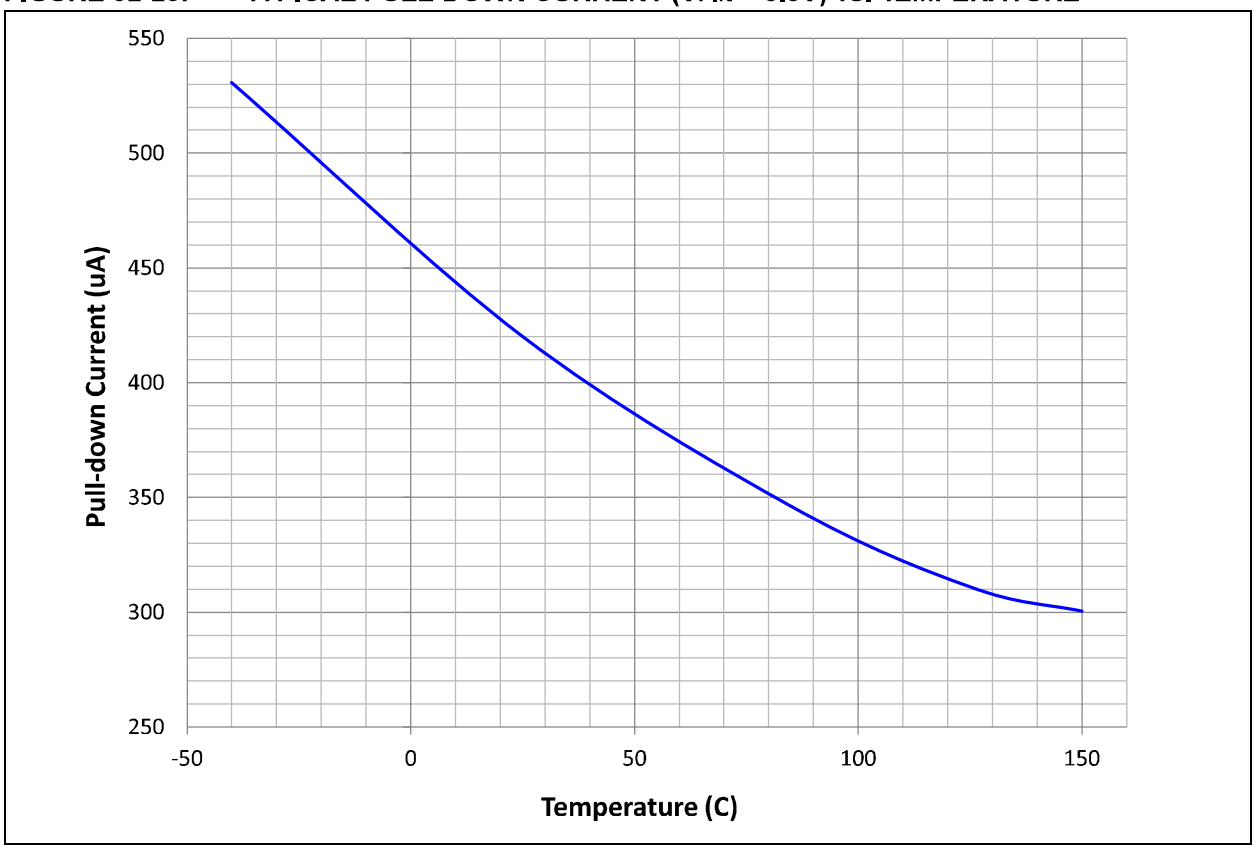


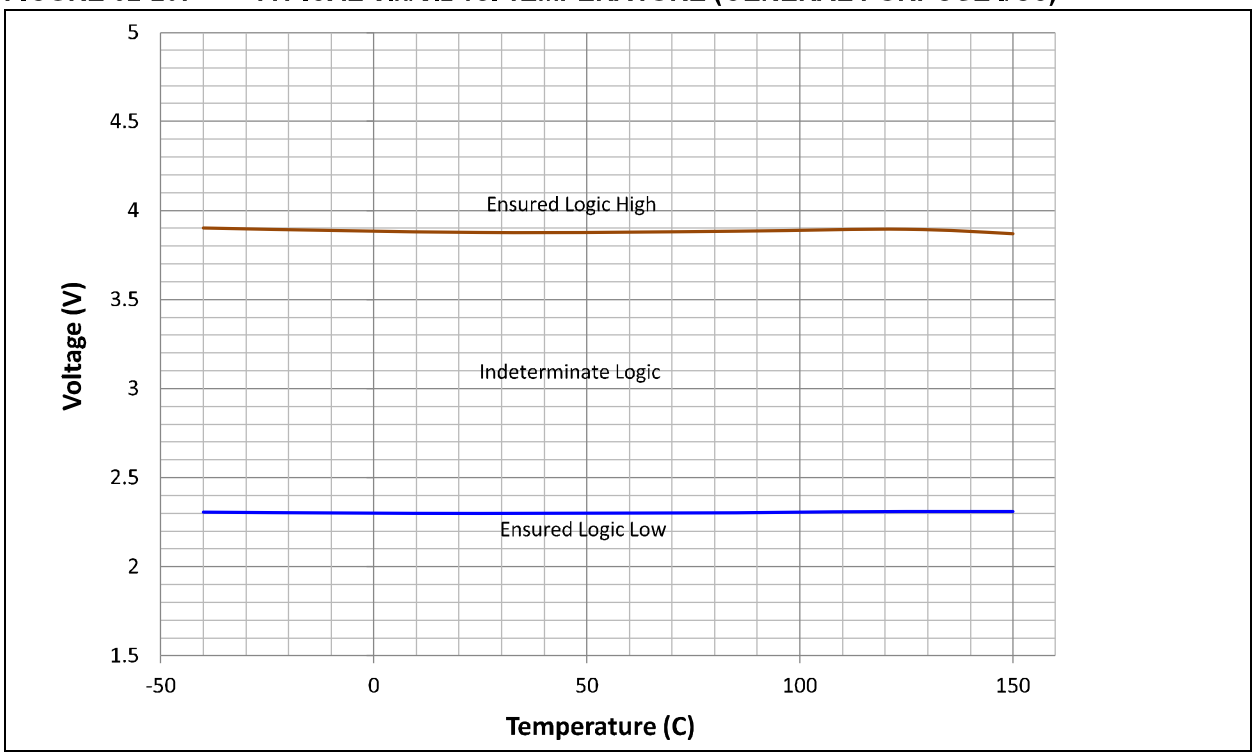
FIGURE 32-28: TYPICAL PULL-DOWN CURRENT (V_{PIN} = 5.5V) vs. TEMPERATURE



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32.9 Voltage Input Low (VIL) – Voltage Input High (VIH)

FIGURE 32-29: TYPICAL VIH/VIL vs. TEMPERATURE (GENERAL PURPOSE I/Os)



32.10 Voltage Output Low (VOL) – Voltage Output High (VOH)

FIGURE 32-30: TYPICAL VOH 8x DRIVER PINS vs. IOH (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

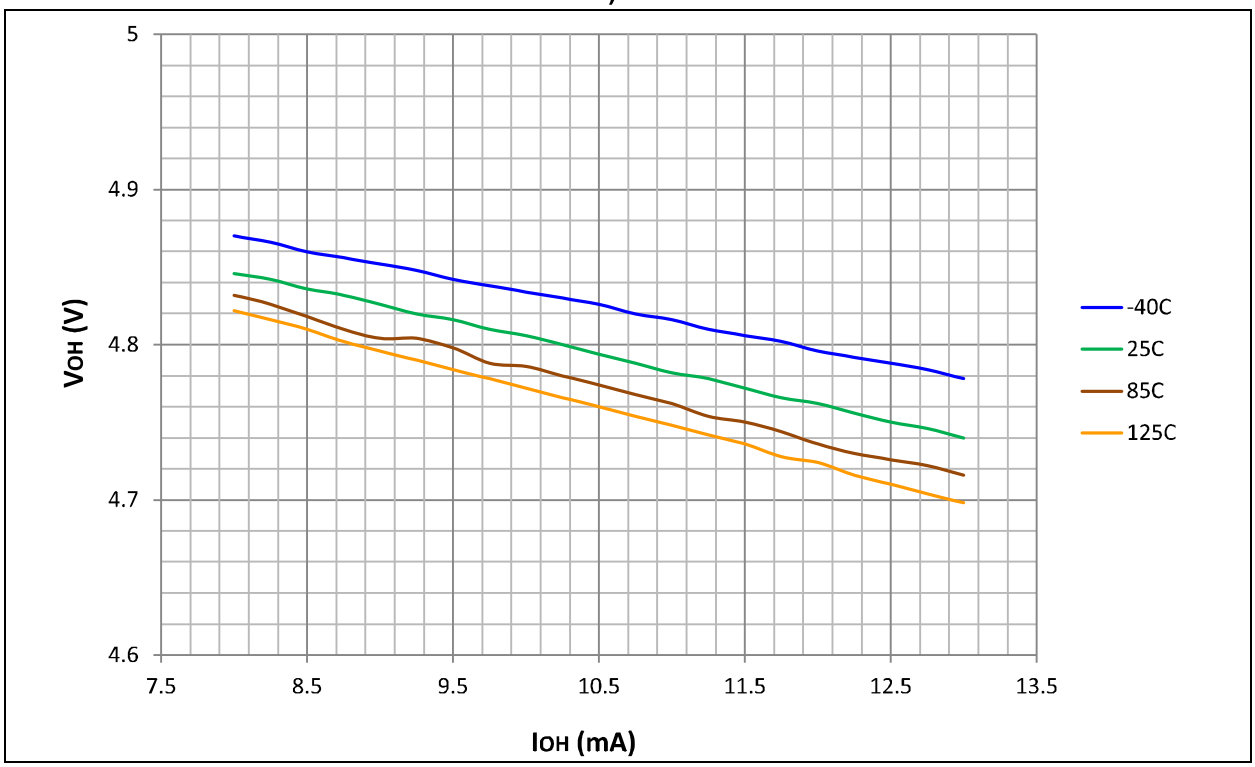


FIGURE 32-31: TYPICAL VOH 4x DRIVER PINS vs. IOH (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

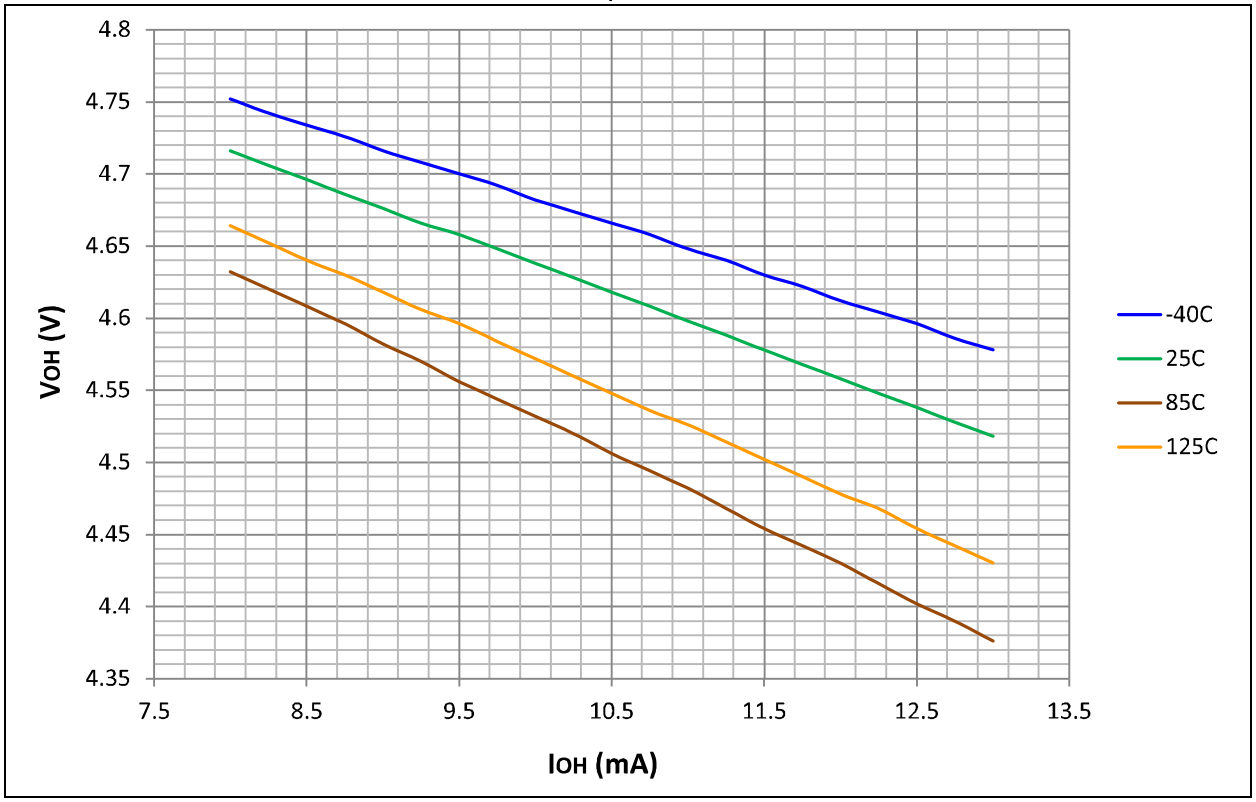
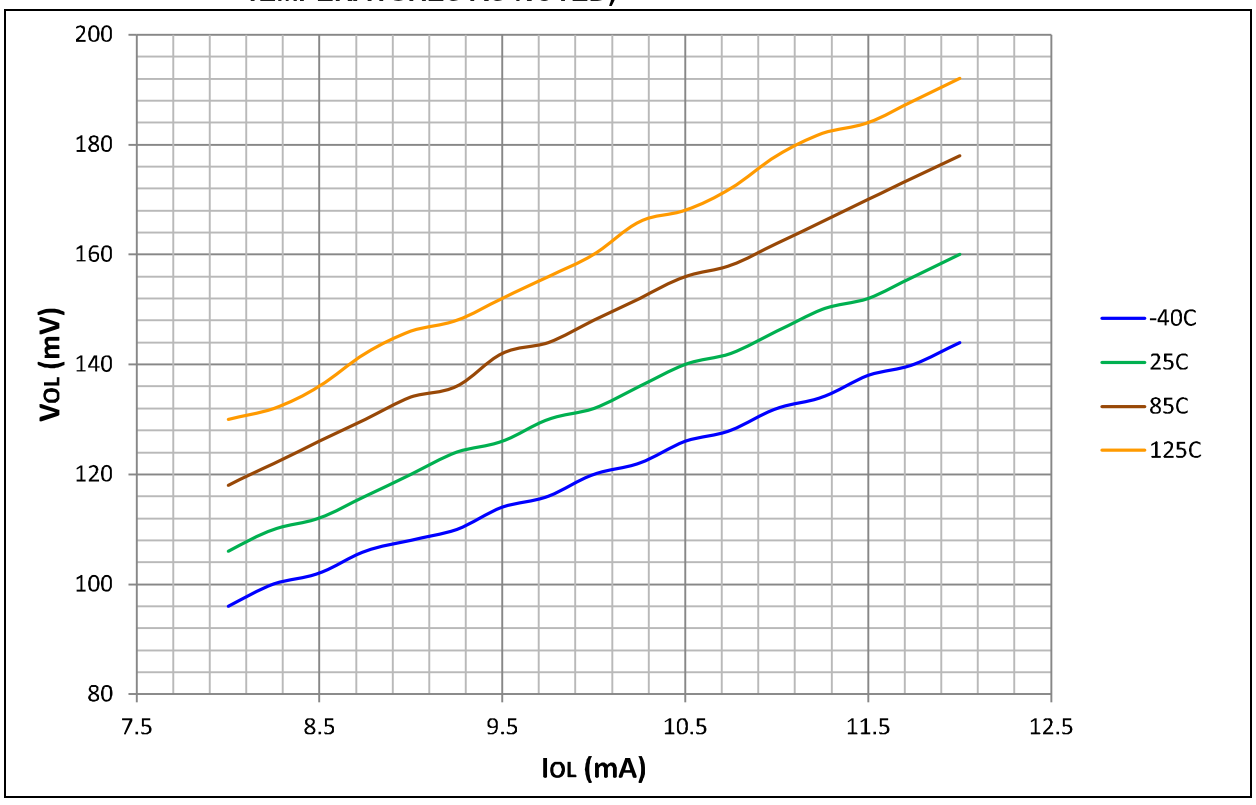
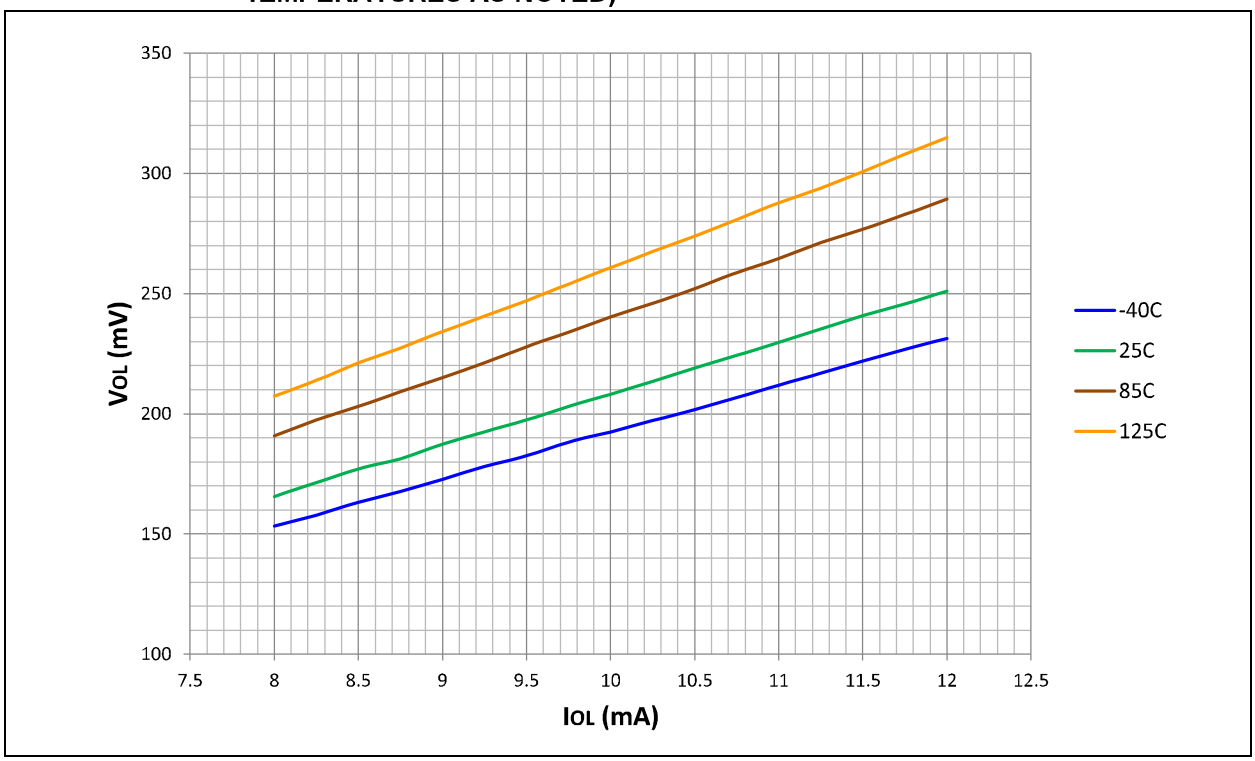


FIGURE 32-32: TYPICAL VOL 8x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



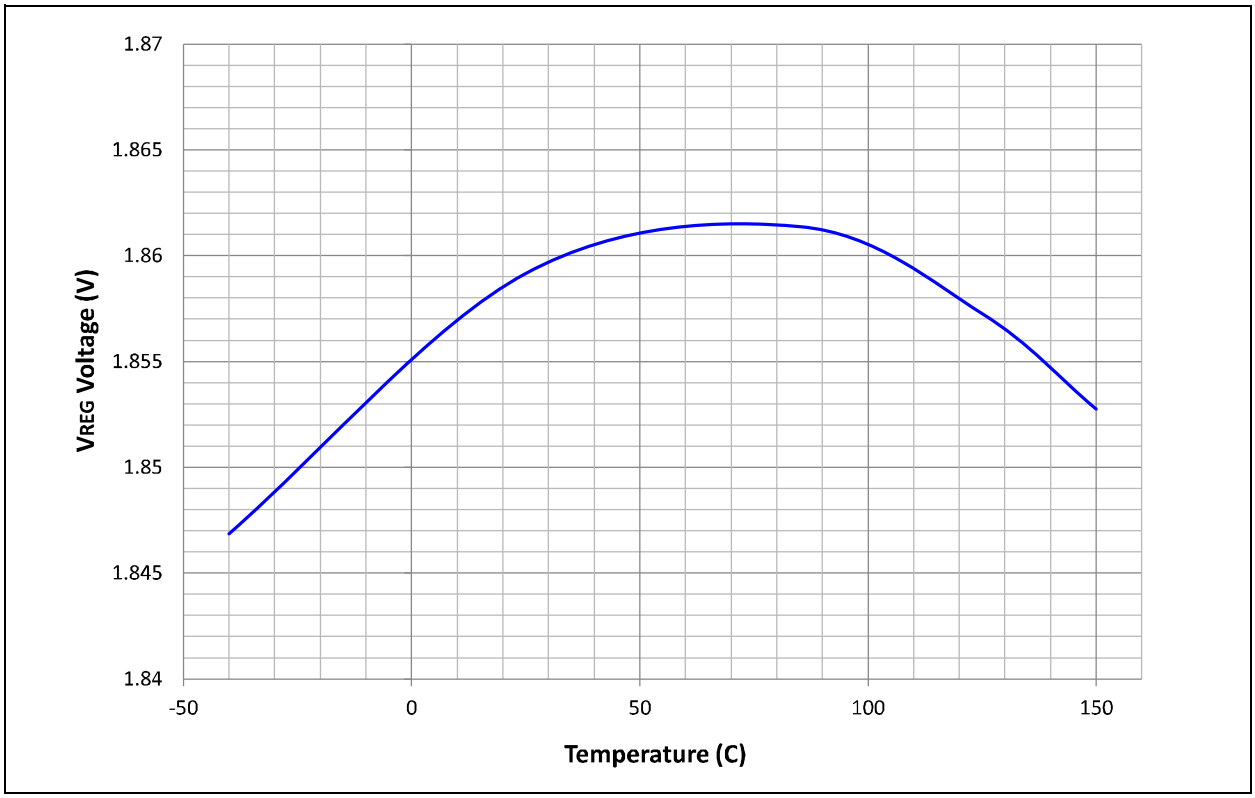
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FIGURE 32-33: TYPICAL VOL 4x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



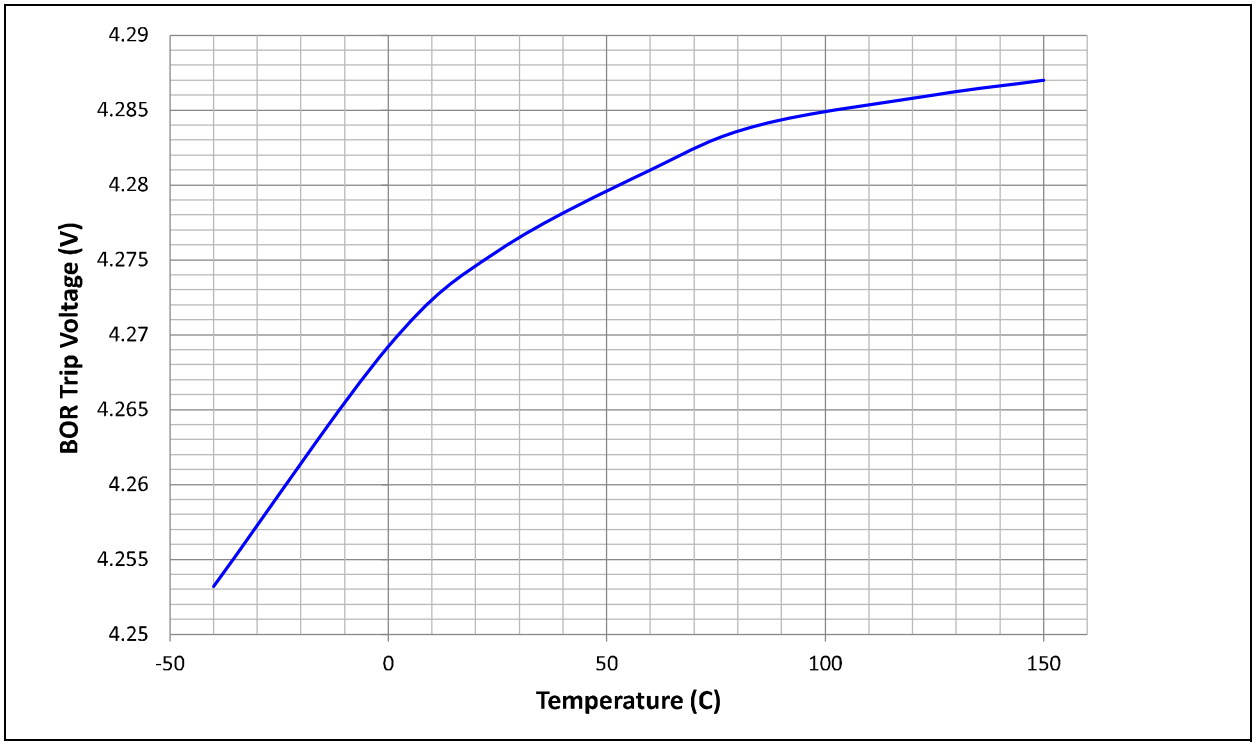
32.11 VREG

FIGURE 32-34: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE



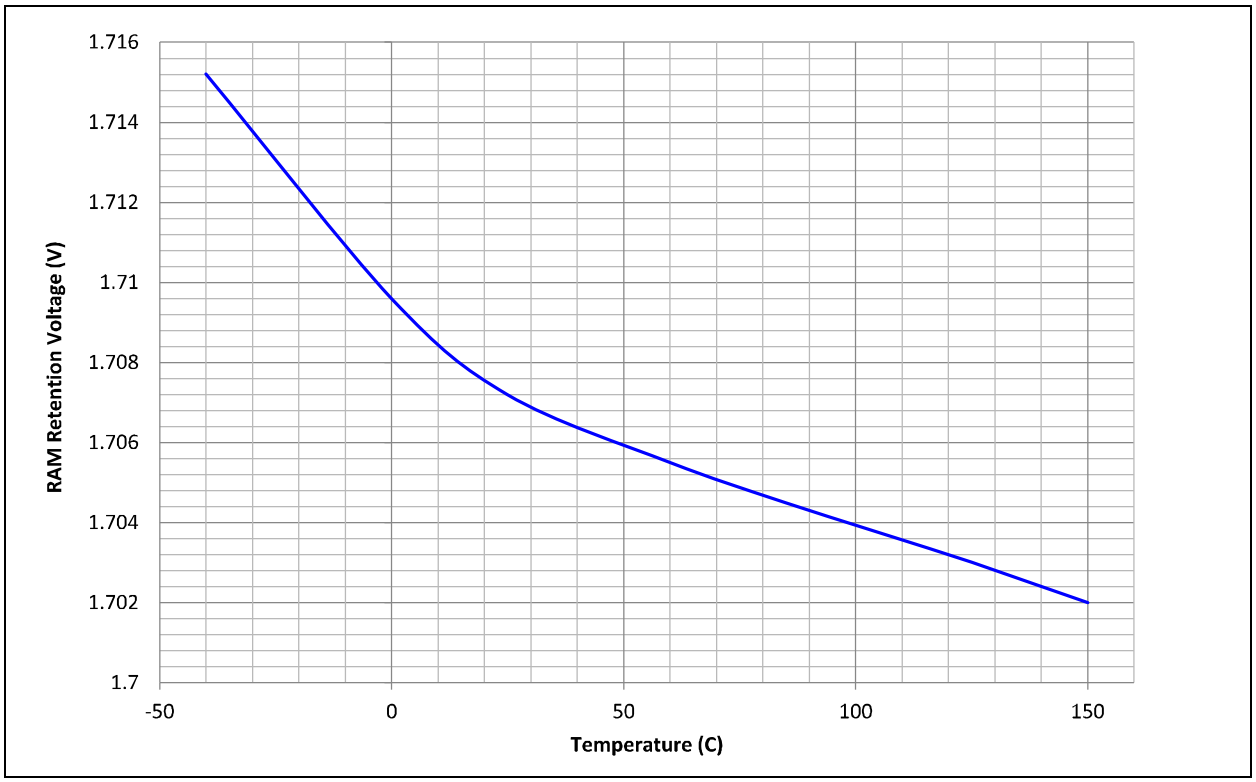
32.12 VBOR

FIGURE 32-35: TYPICAL BOR TRIP RANGE vs. TEMPERATURE



32.13 RAM Retention

FIGURE 32-36: TYPICAL RAM RETENTION VOLTAGE vs. TEMPERATURE



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32.14 Comparator Op Amp Offset

FIGURE 32-37: TYPICAL COMPARATOR OFFSET vs. VCM

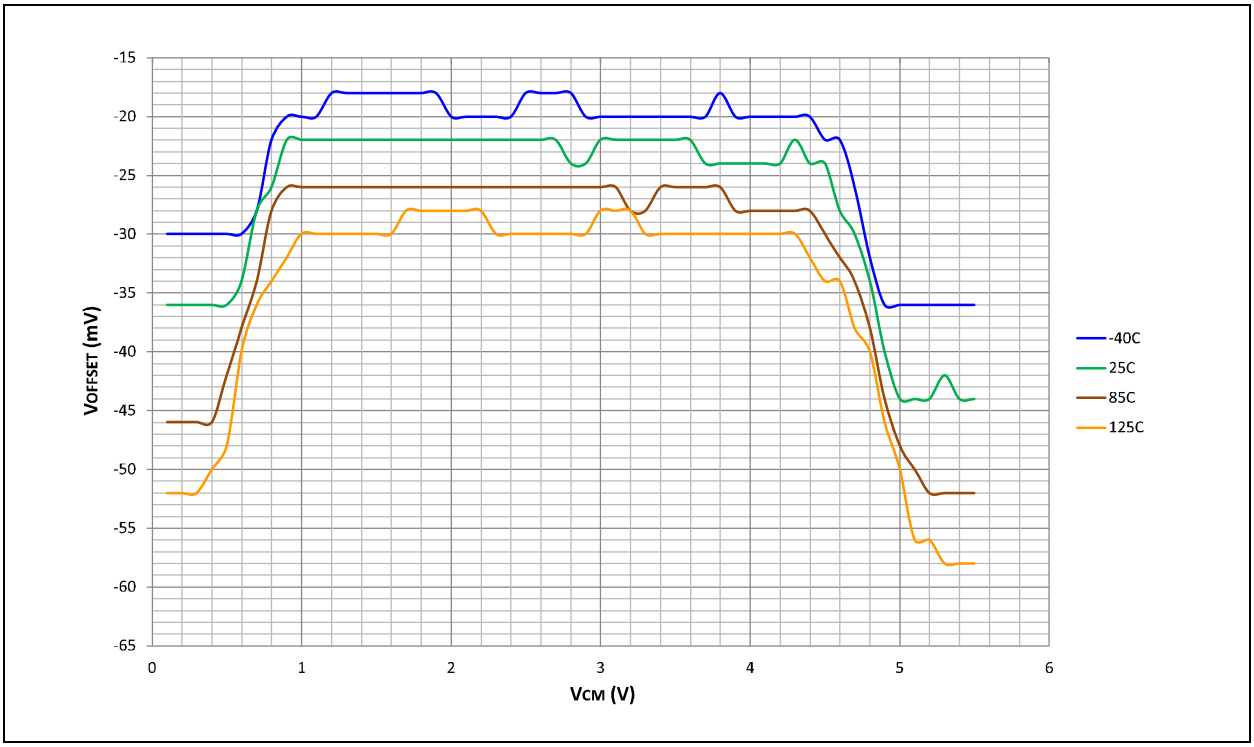
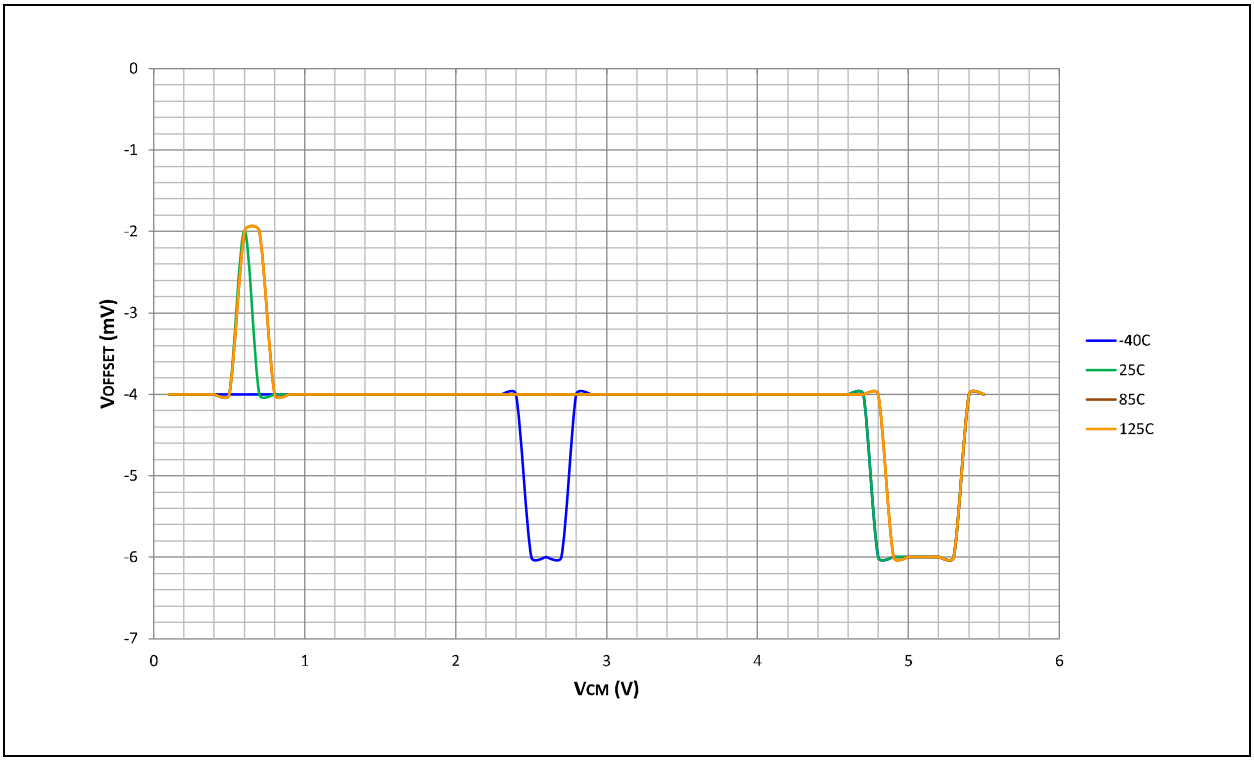
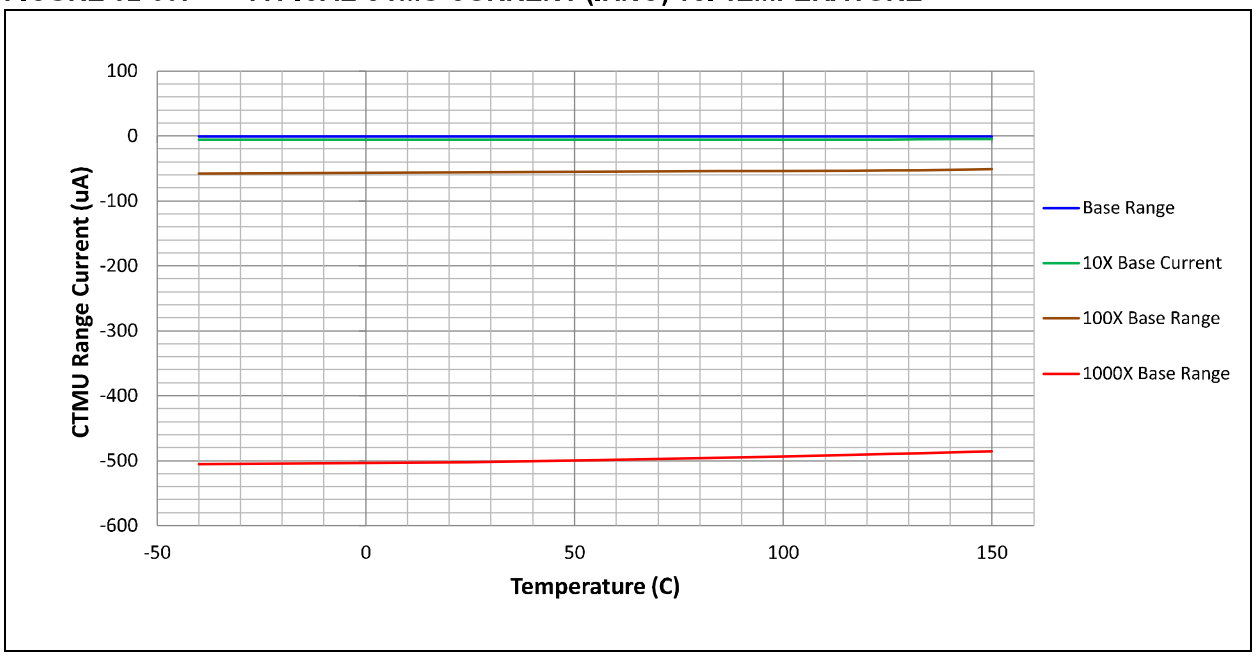


FIGURE 32-38: TYPICAL OP AMP OFFSET vs. VCM OP AMP OFFSET



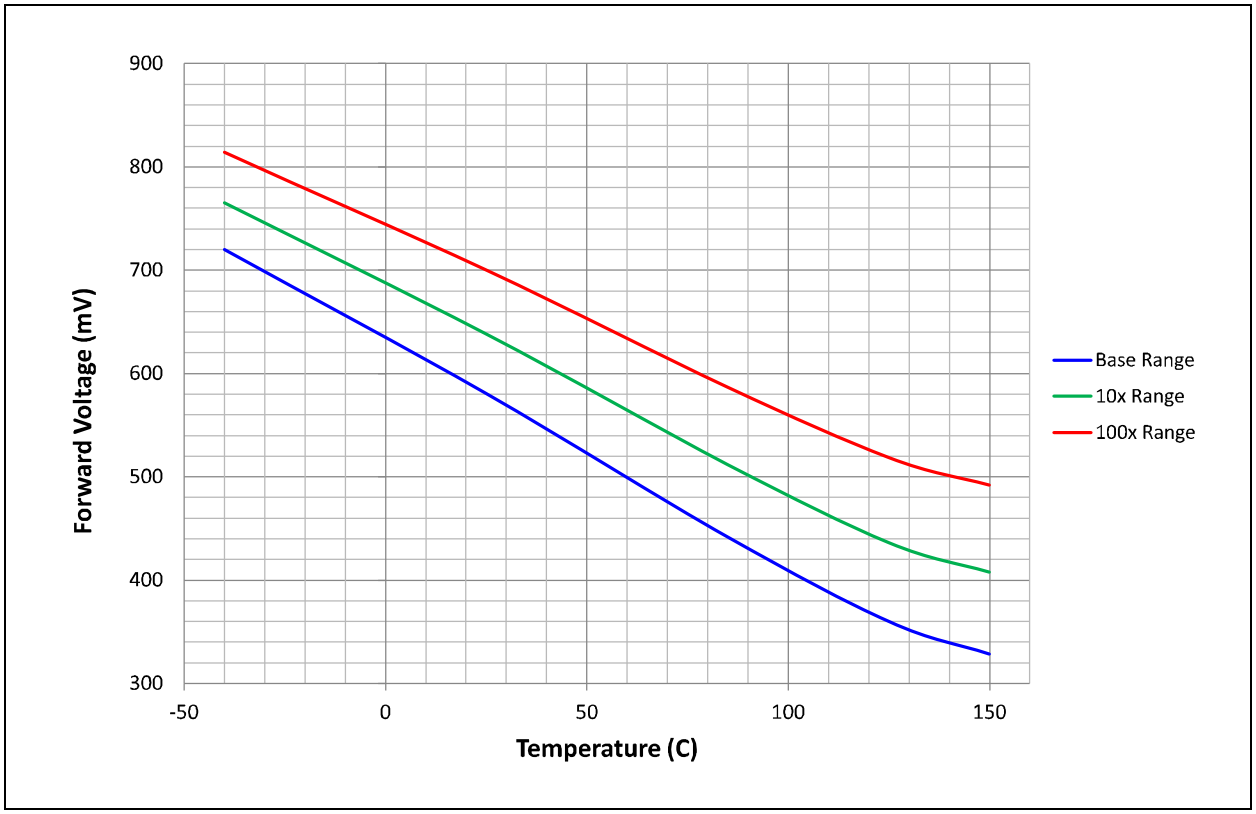
32.15 CTMU Current vs. Temperature

FIGURE 32-39: TYPICAL CTMU CURRENT (IRNG) vs. TEMPERATURE



32.16 CTMU Temperature Forward Diode

FIGURE 32-40: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE vs. TEMPERATURE



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32.17 ADC DNL

FIGURE 32-41: TYPICAL DNL (V_{DD} = 5.5V, -40°C)

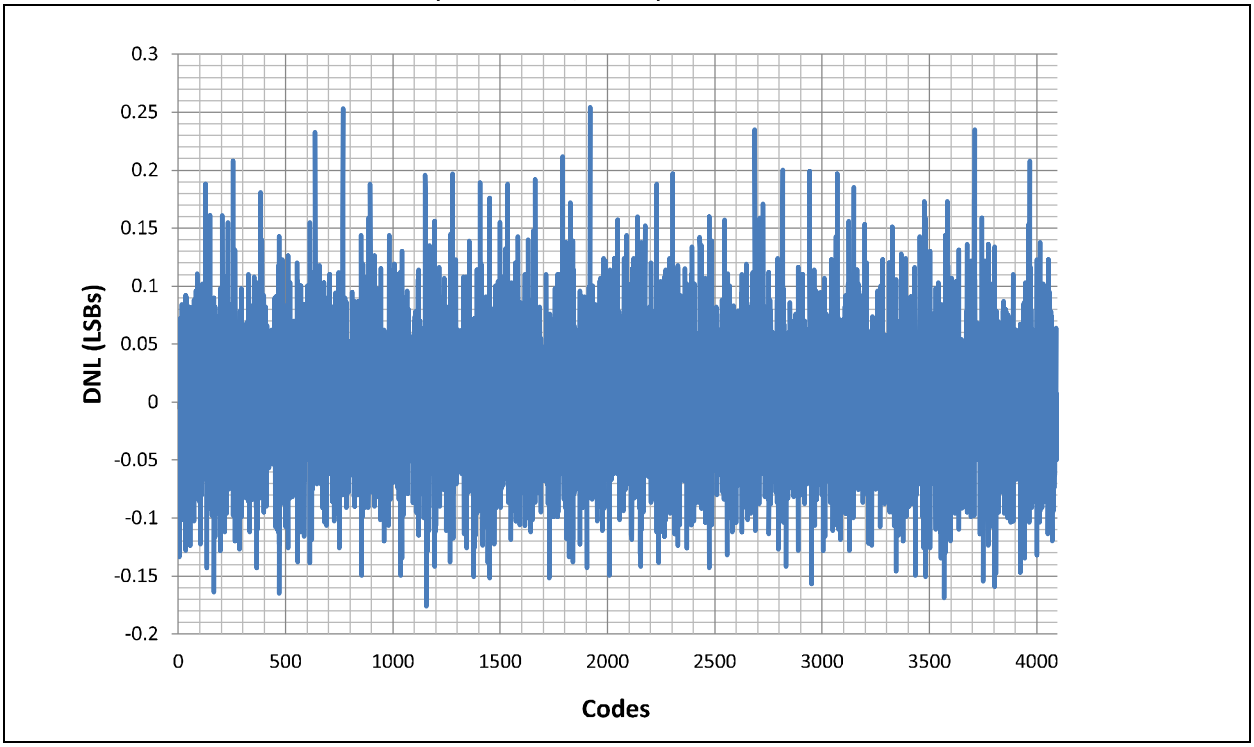


FIGURE 32-42: TYPICAL DNL (V_{DD} = 5.5V, +25°C)

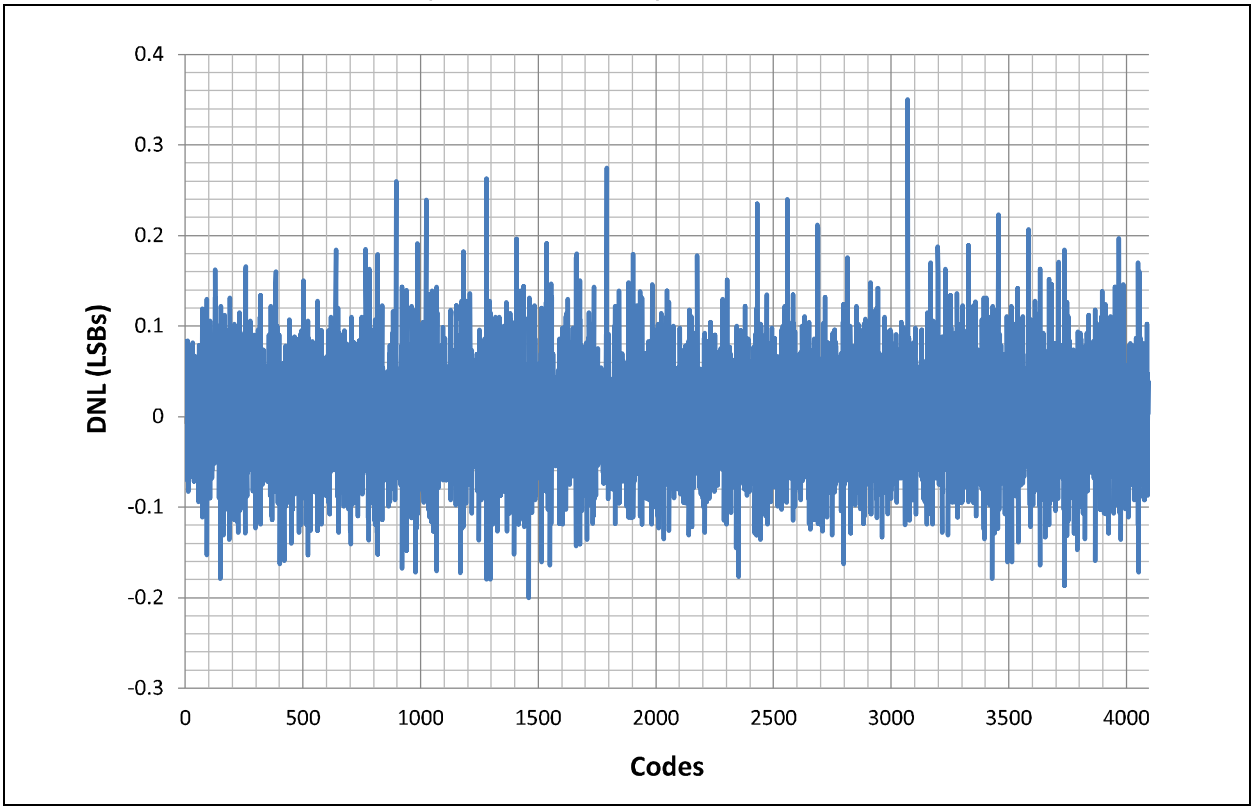


FIGURE 32-43: TYPICAL DNL (V_{DD} = 5.5V, +85°C)

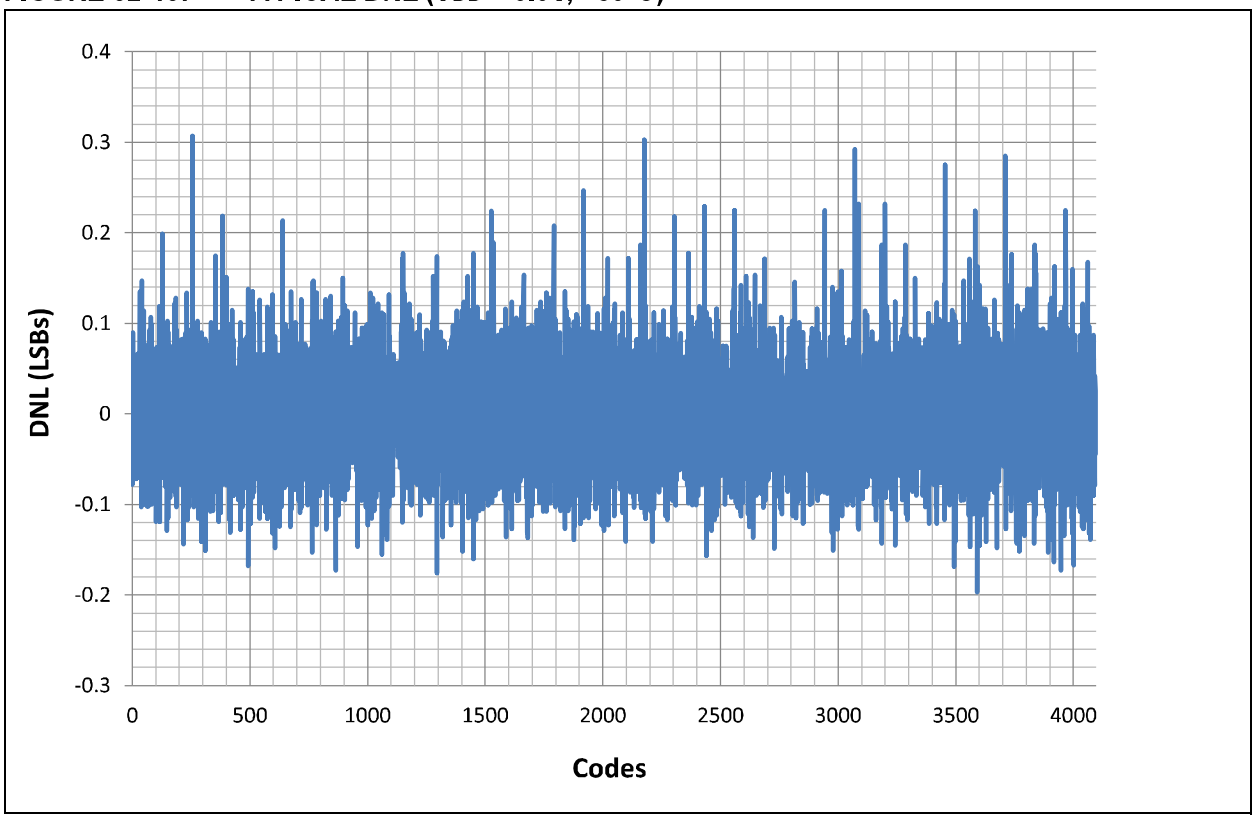
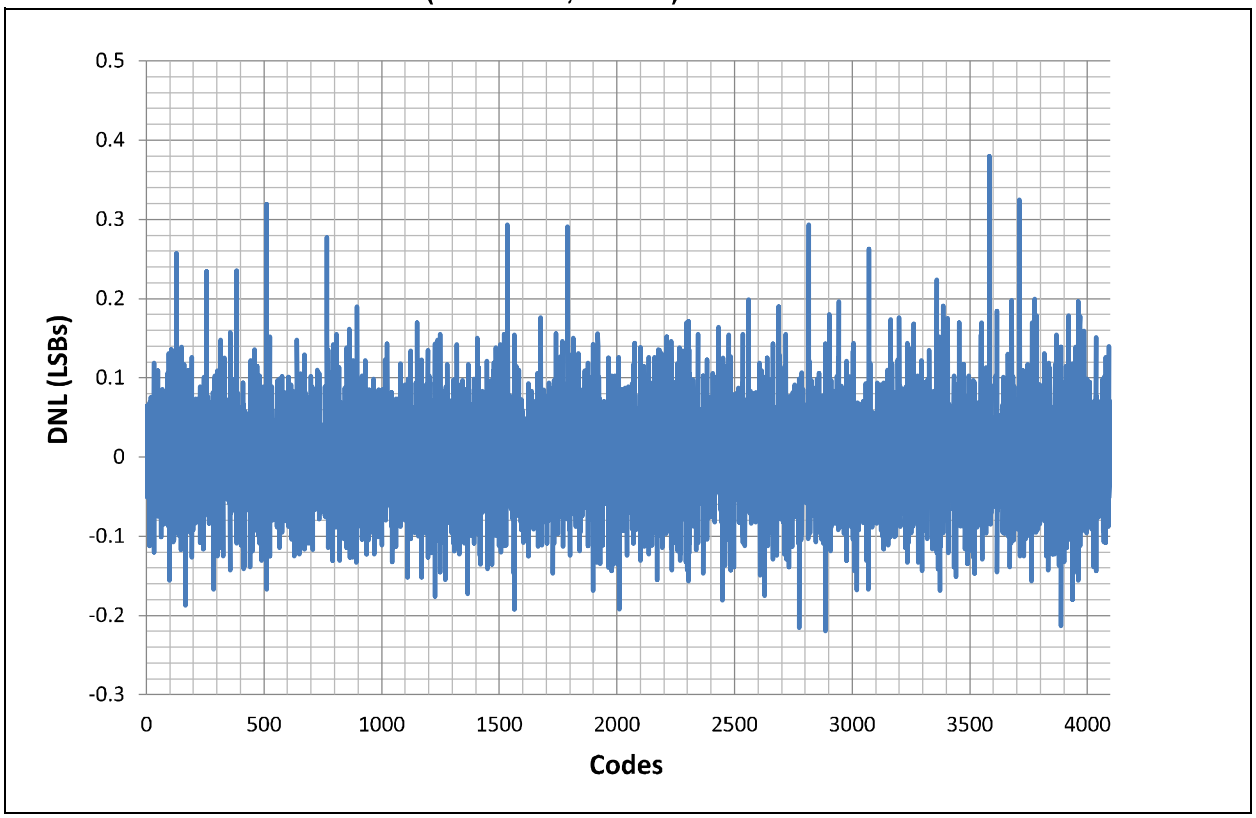


FIGURE 32-44: TYPICAL DNL (V_{DD} = 5.5V, +125°C)



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32.18 ADC INL

FIGURE 32-45: TYPICAL INL (V_{DD} = 5.5V, -40°C)

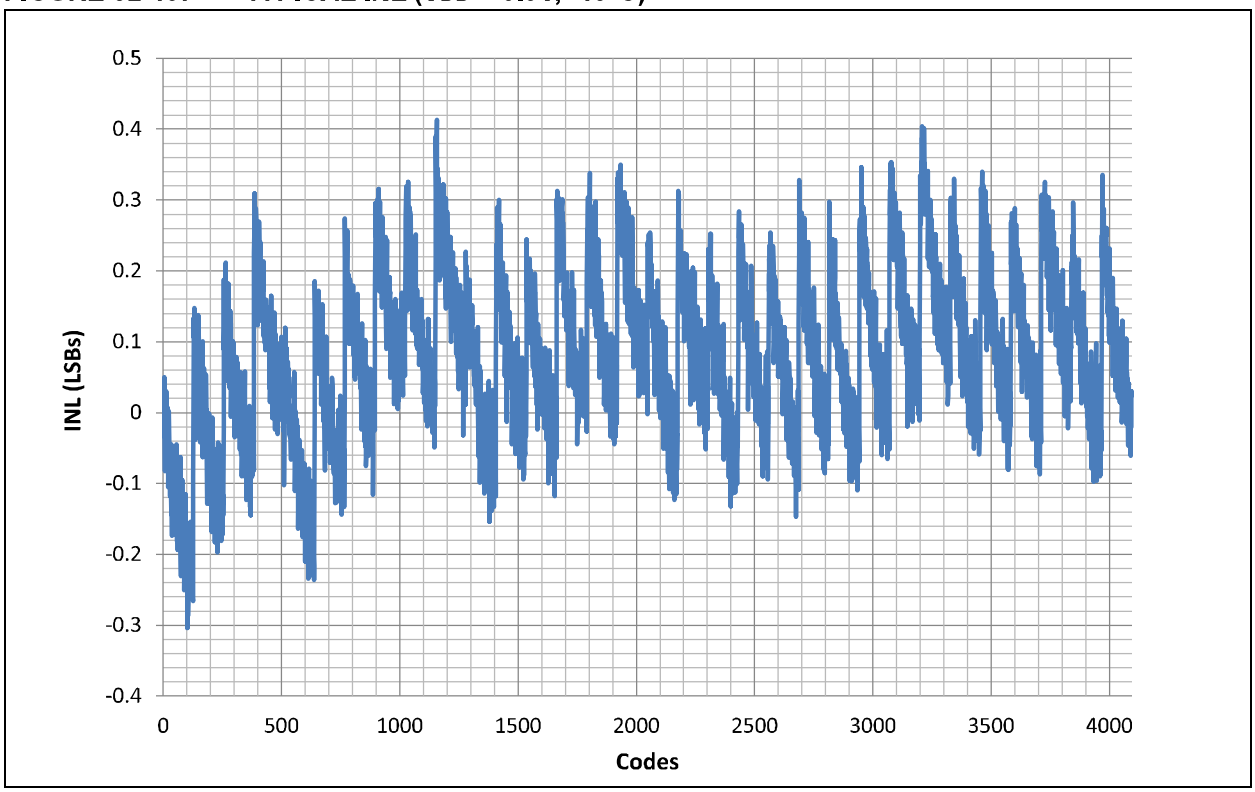


FIGURE 32-46: TYPICAL INL (V_{DD} = 5.5V, +25°C)

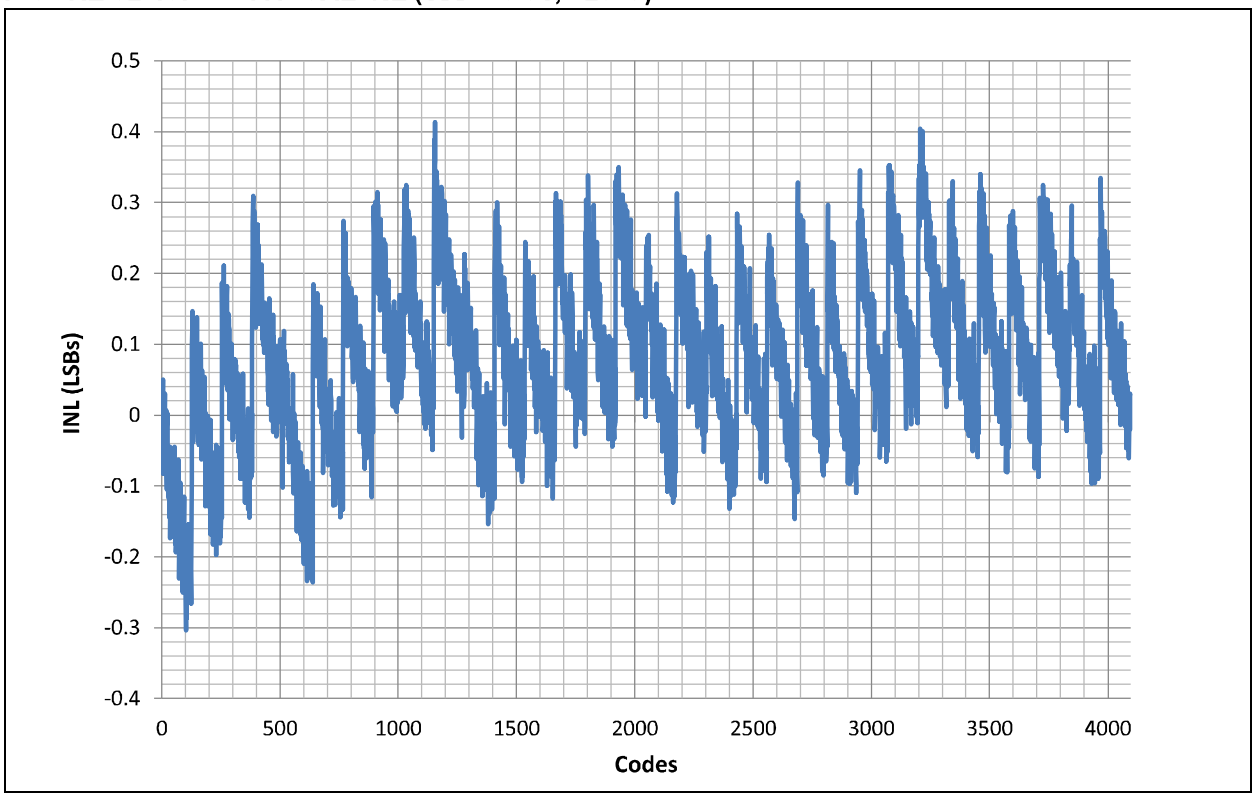


FIGURE 32-47: TYPICAL INL (VDD = 5.5V, +85°C)

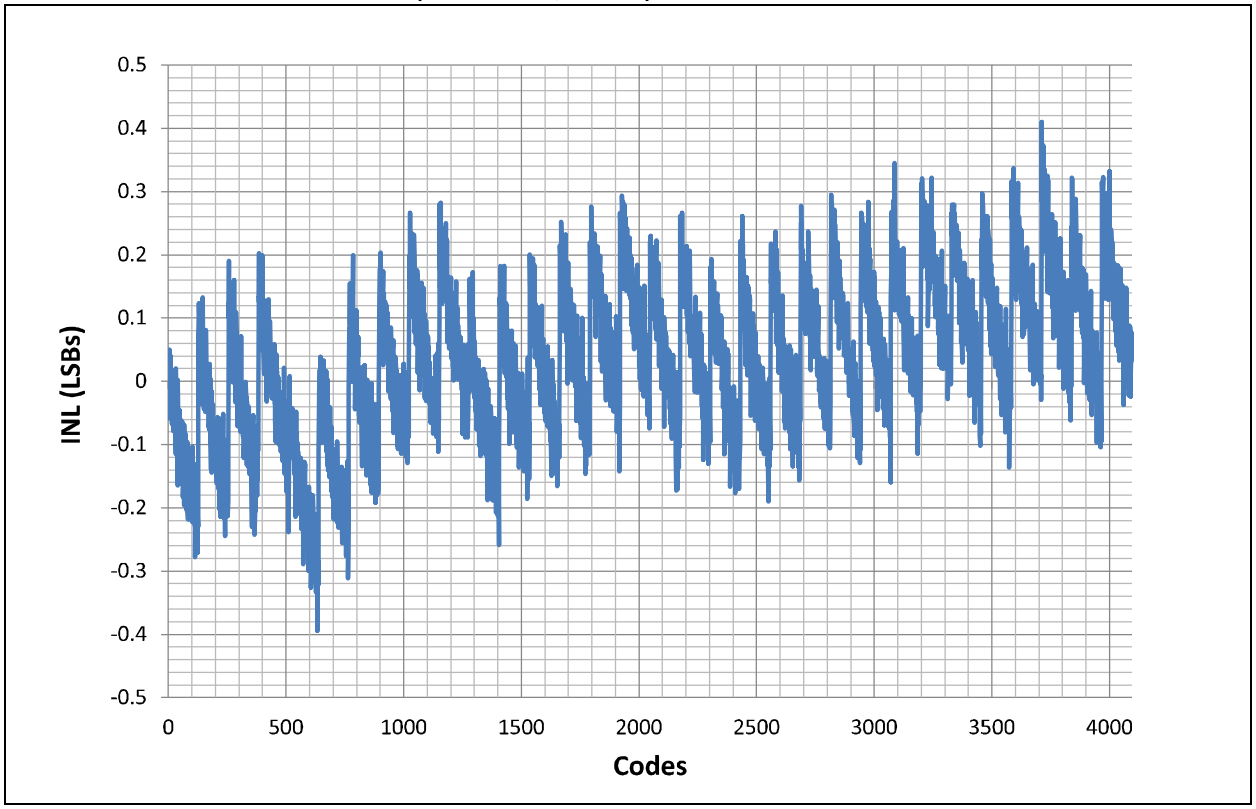
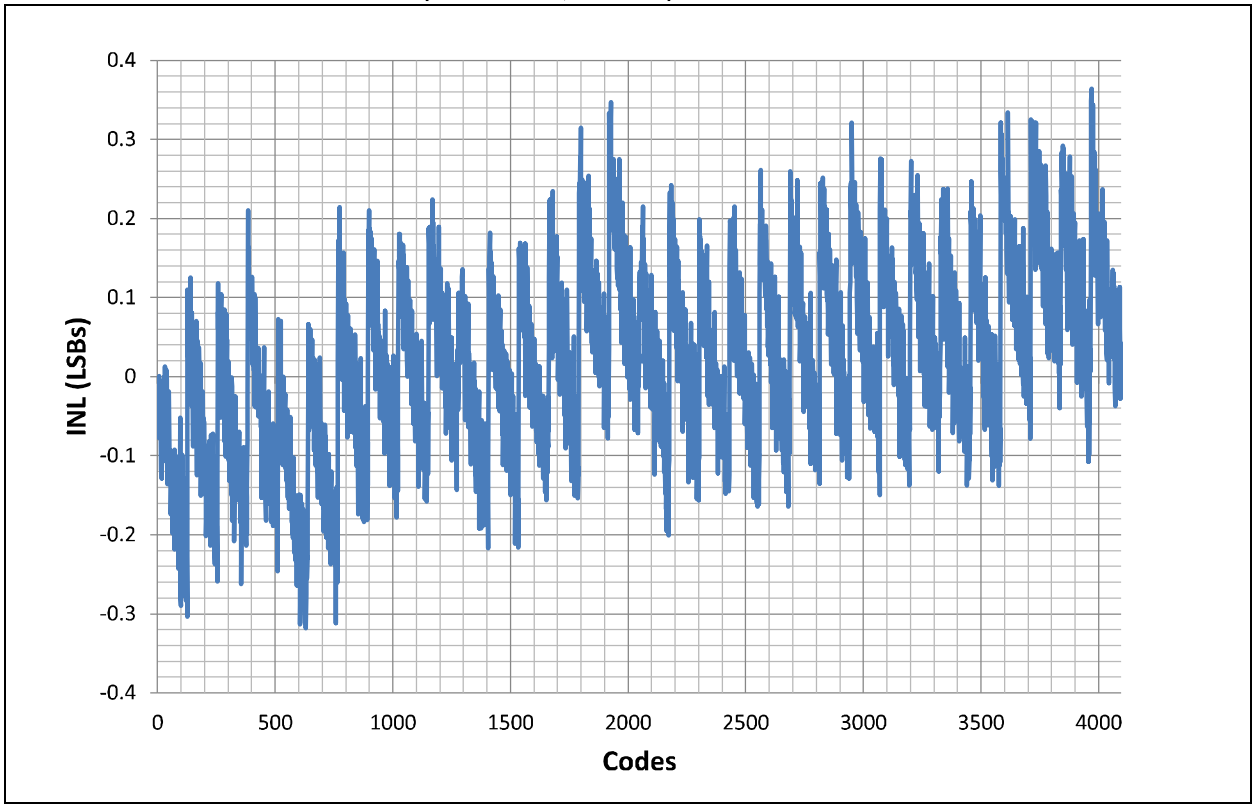


FIGURE 32-48: TYPICAL INL (VDD = 5.5V, +125°C)



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32.19 ADC Gain Offset Error

FIGURE 32-49: TYPICAL ADC GAIN ERROR vs. TEMPERATURE

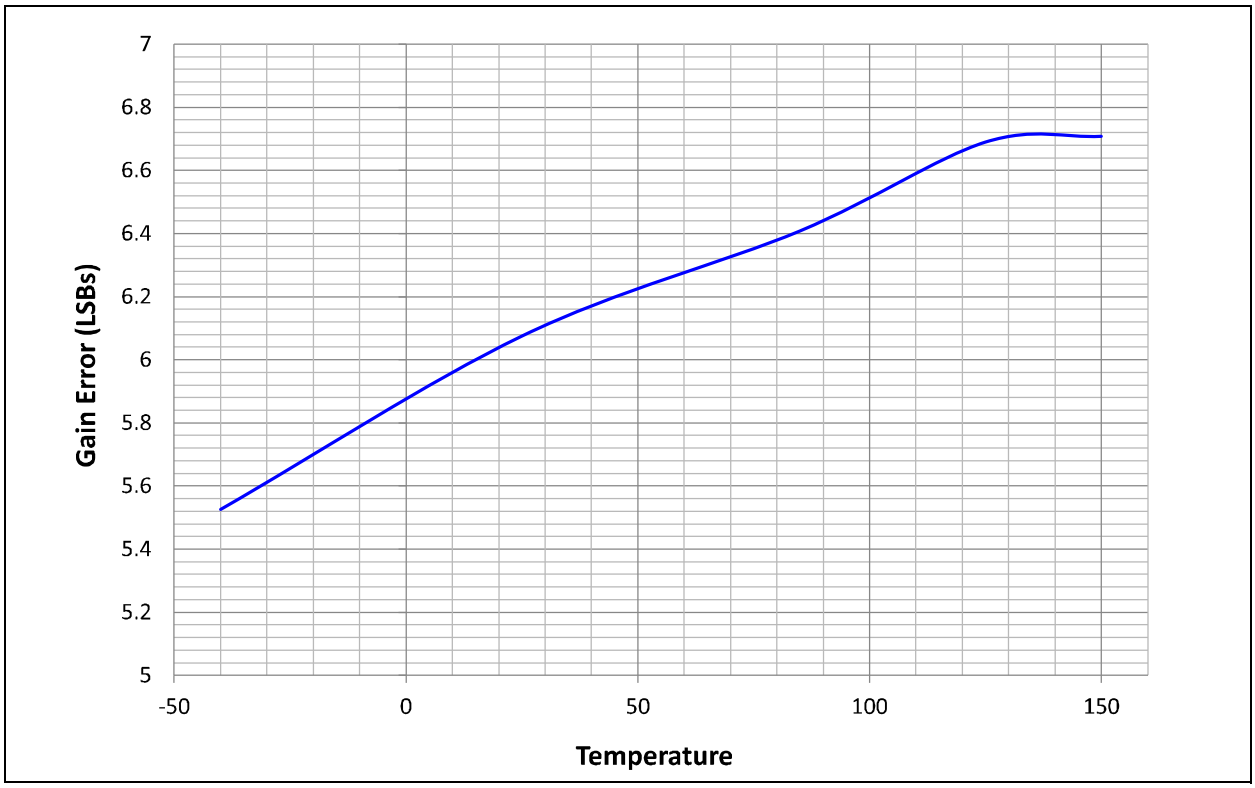
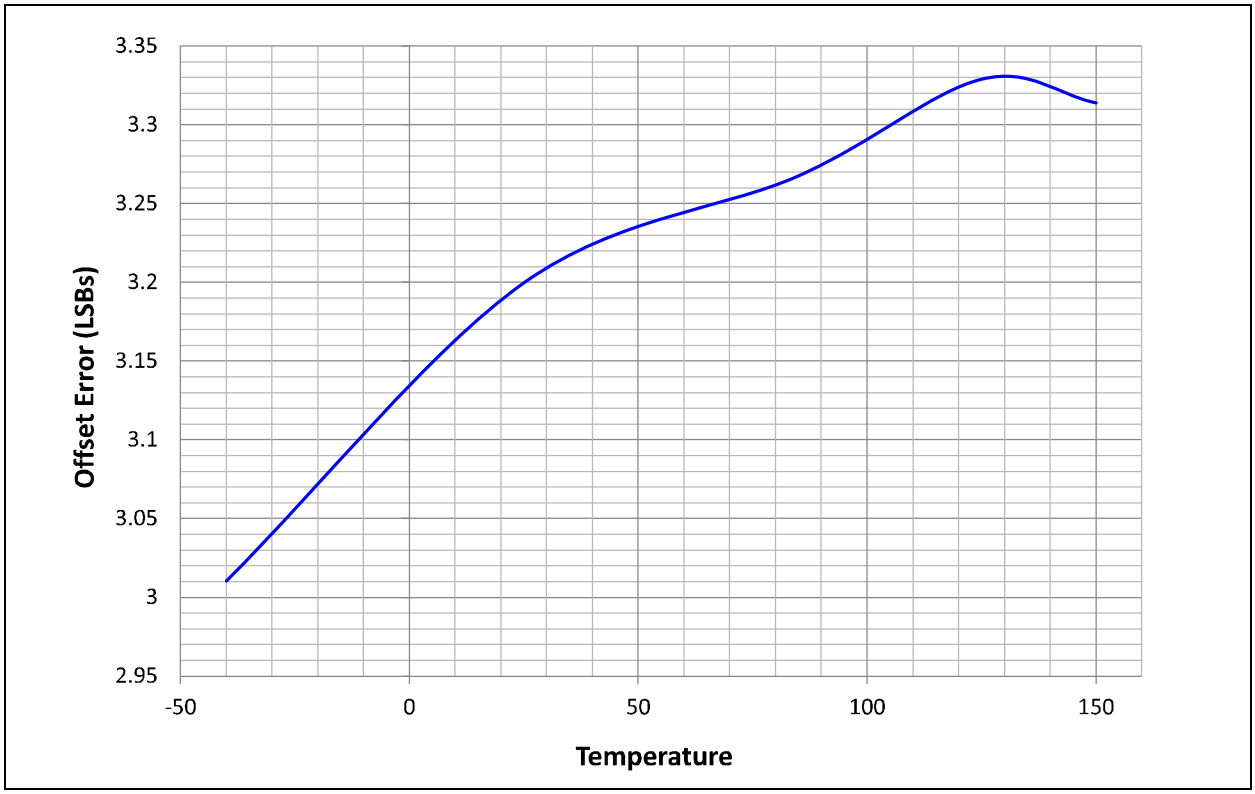


FIGURE 32-50: TYPICAL ADC OFFSET ERROR vs. TEMPERATURE



NOTES:

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33.0 CHARACTERISTICS FOR HIGH-TEMPERATURE DEVICES (+150°C)

33.1 IDD

FIGURE 33-1: TYPICAL/MAXIMUM IDD vs. FOSC (EC MODE 10 MHz TO 40 MHz, 5.5V MAX)

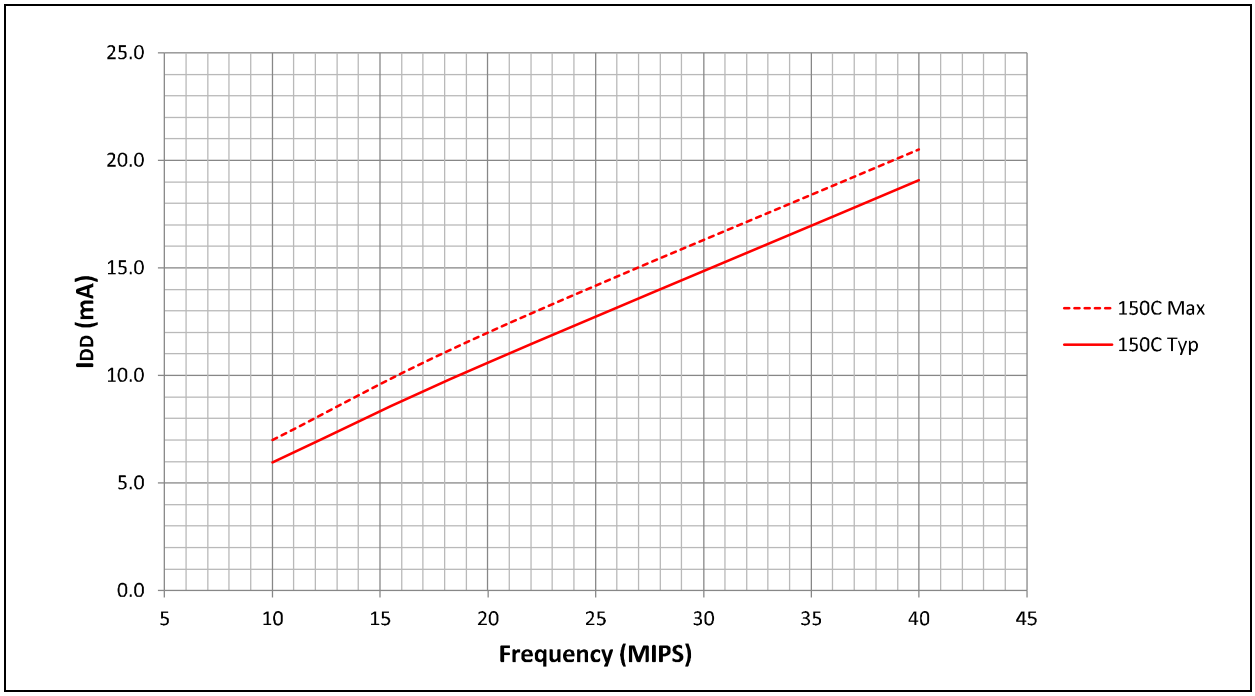


FIGURE 33-2: TYPICAL IDD vs. VDD (EC MODE, 10 MIPS)

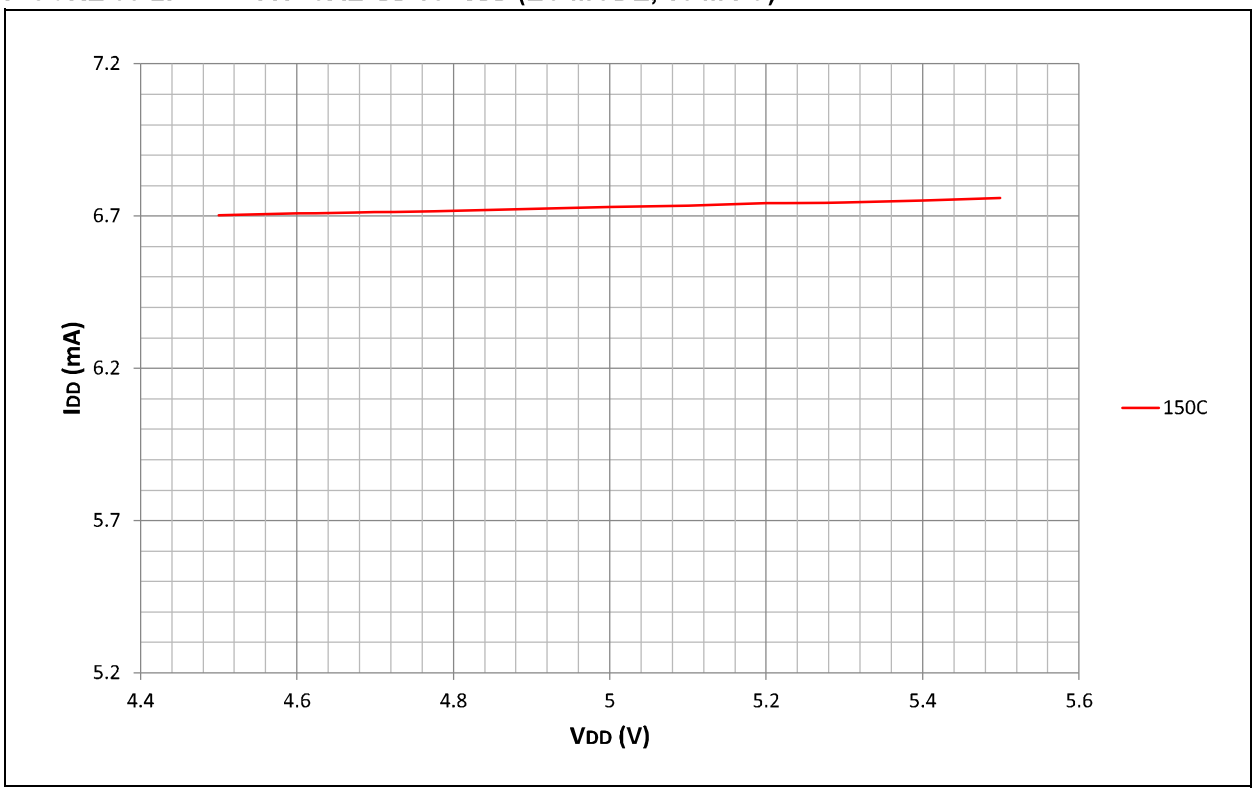


FIGURE 33-3: TYPICAL IDD vs. VDD (EC MODE, 20 MIPS)

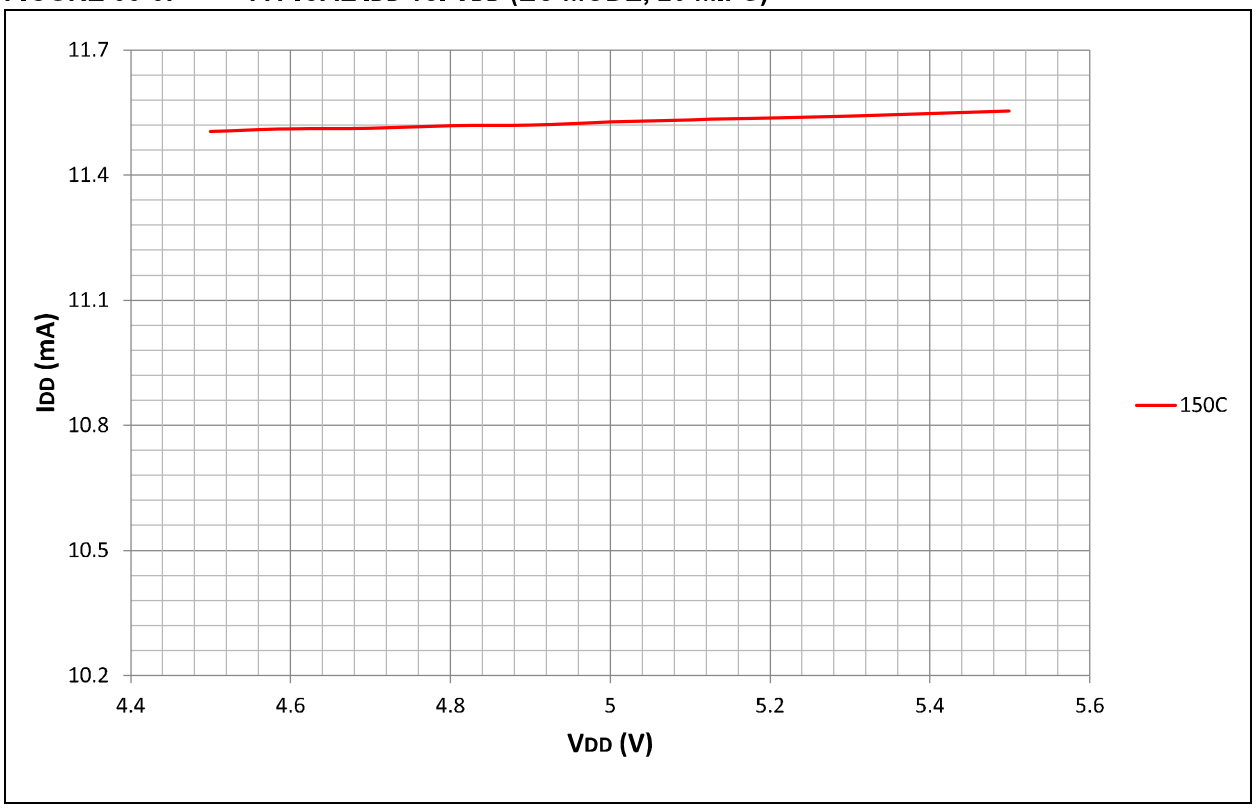
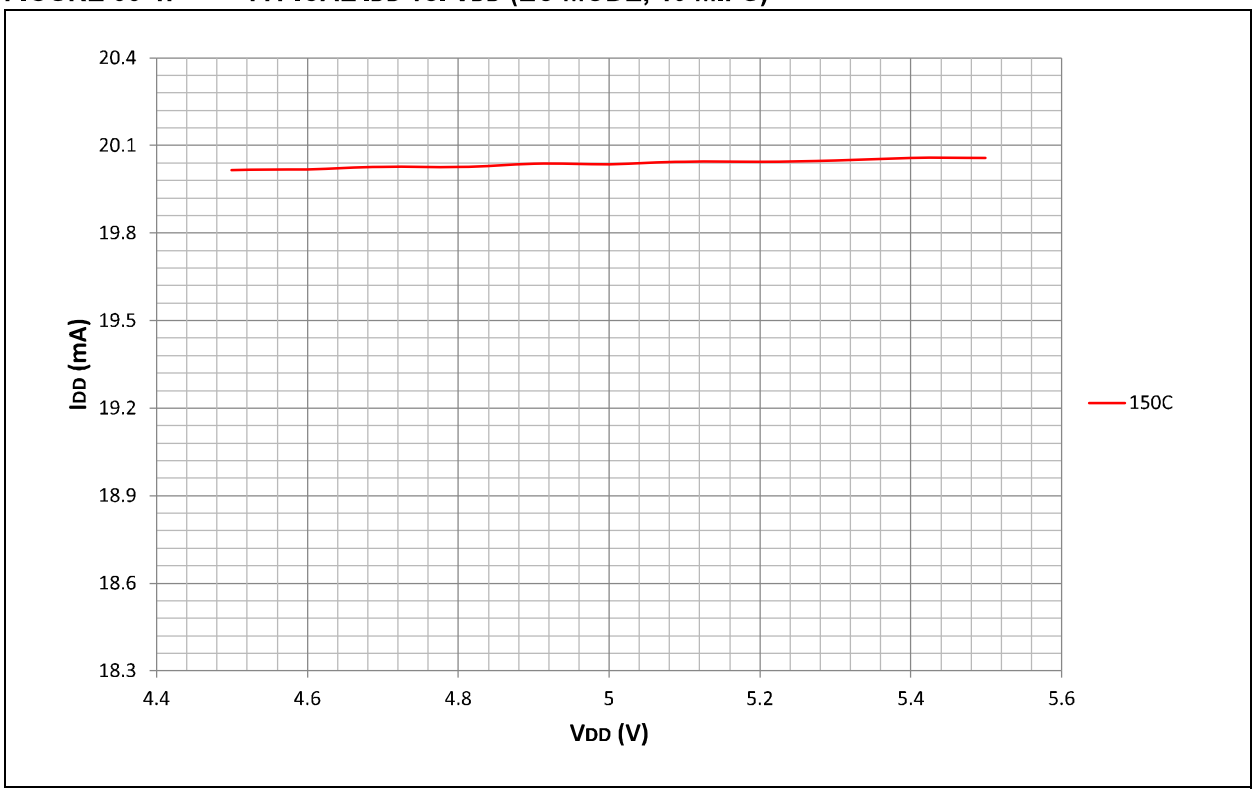


FIGURE 33-4: TYPICAL IDD vs. VDD (EC MODE, 40 MIPS)



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33.2 IIDLE

FIGURE 33-5: TYPICAL/MAXIMUM IIDLE vs. FOSC (EC MODE 10 MHz TO 40 MHz, 5.5V MAX)

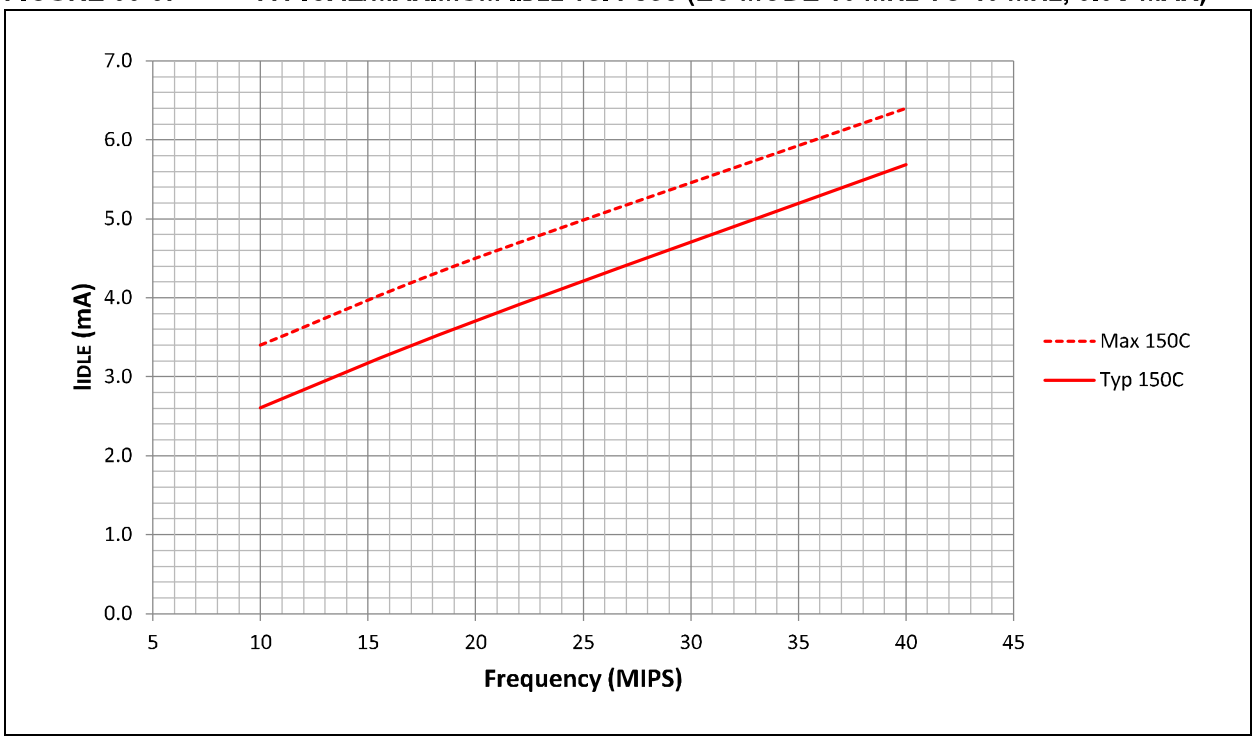


FIGURE 33-6: TYPICAL IIDLE vs. VDD (EC MODE, 10 MIPS)

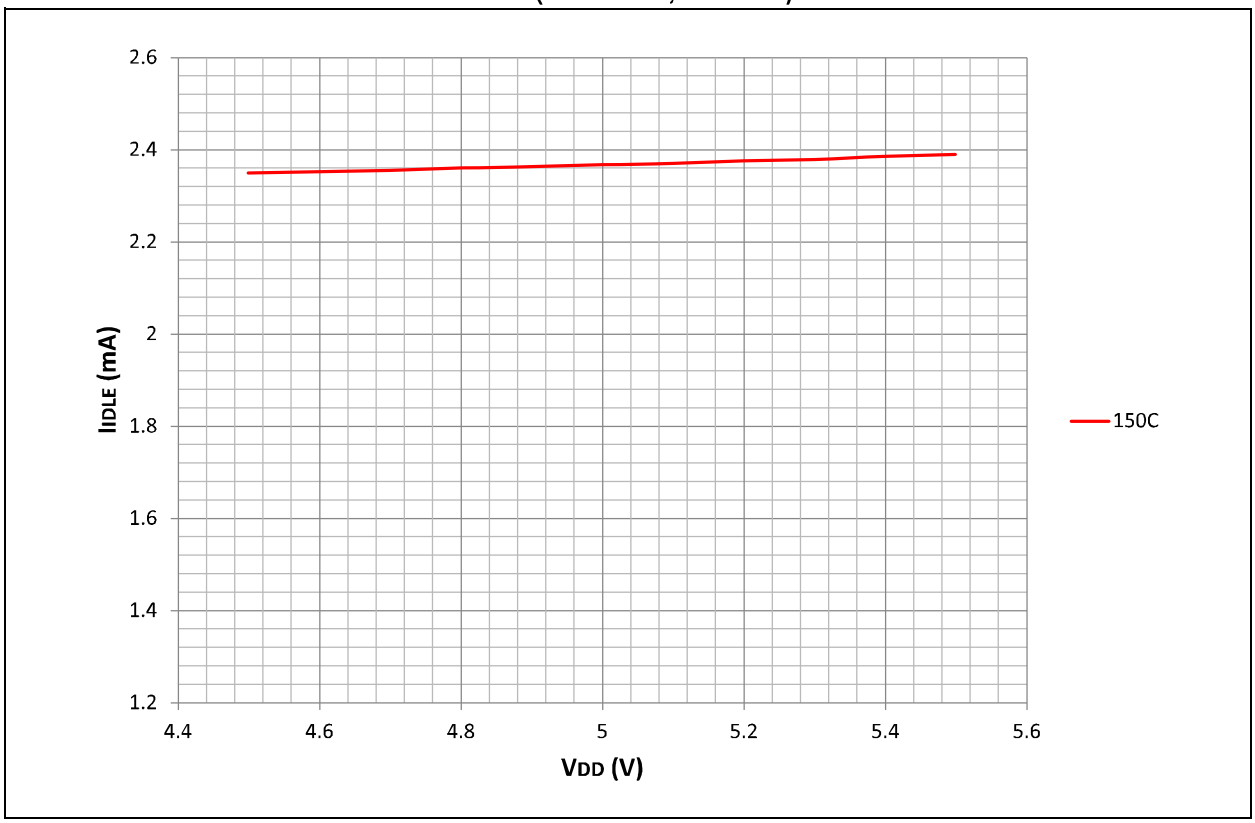


FIGURE 33-7: TYPICAL IIDLE vs. VDD (EC MODE, 20 MIPS)

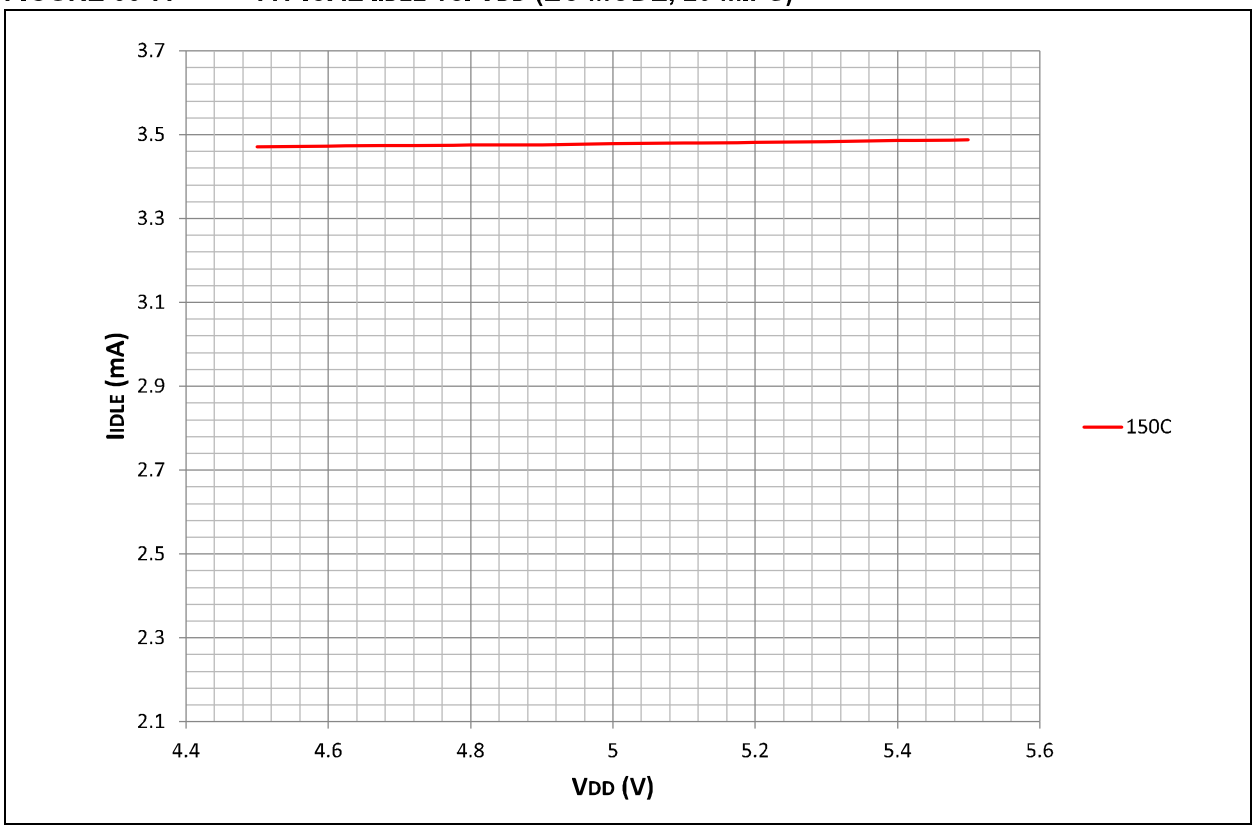
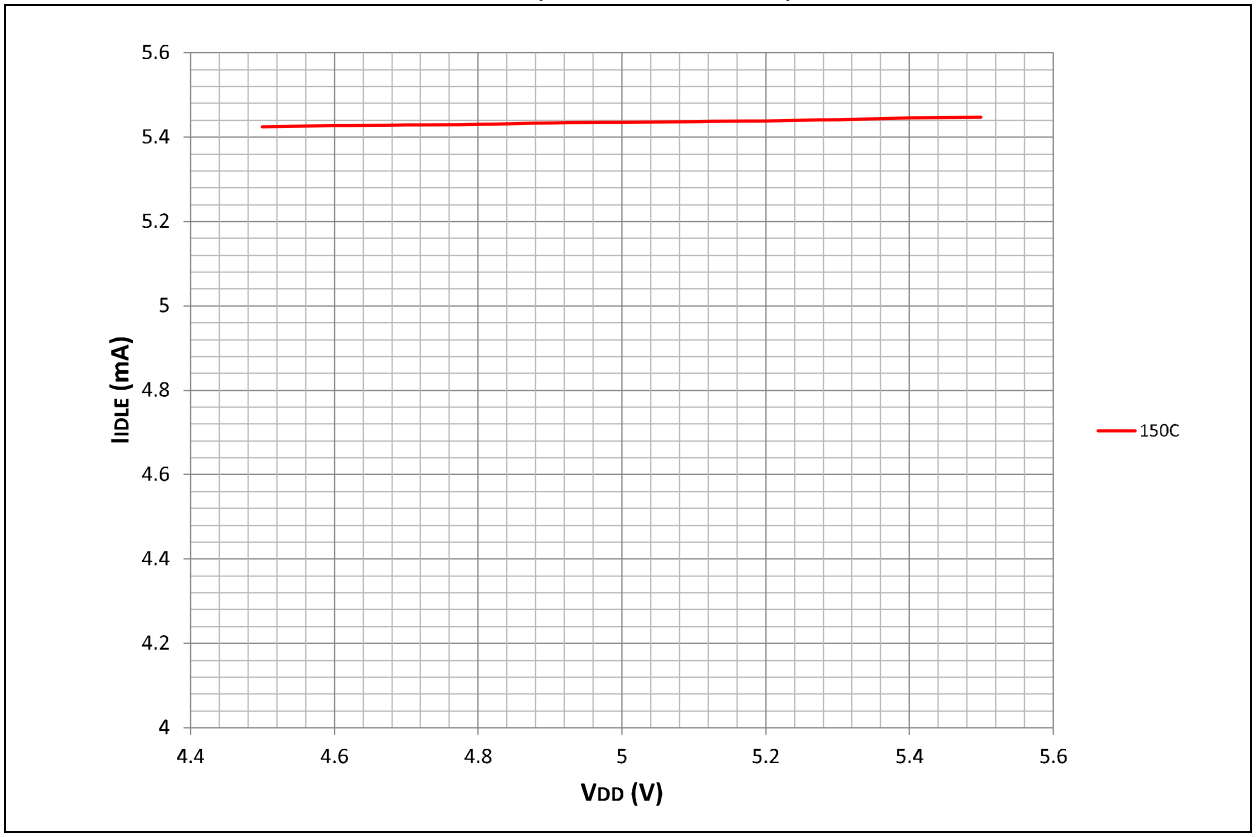


FIGURE 33-8: TYPICAL IIDLE vs. VDD (EC MODE, 40 MIPS)



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33.3 IDOZE

FIGURE 33-9: TYPICAL IDOZE vs. VDD (DOZE 1:2, 70 MIPS)

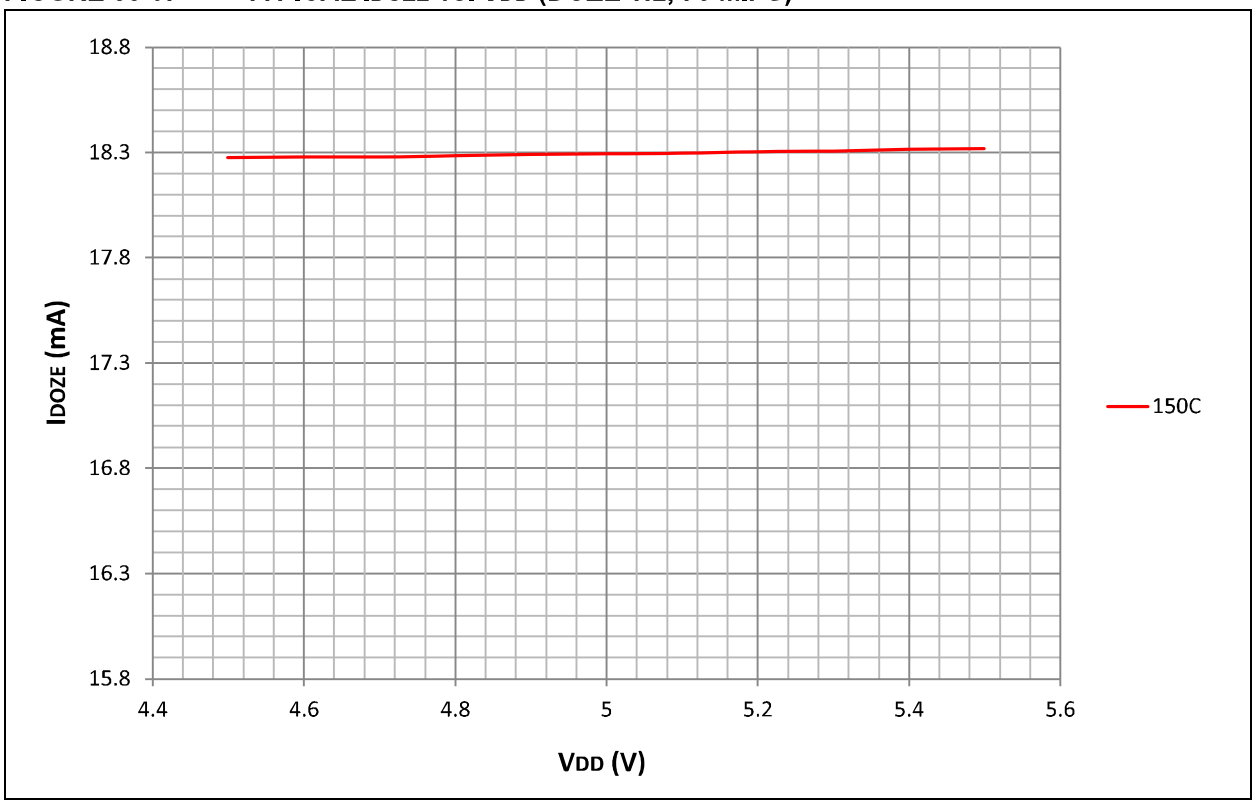


FIGURE 33-10: TYPICAL/MAXIMUM IDOZE vs. TEMPERATURE (DOZE 1:2, 70 MIPS)

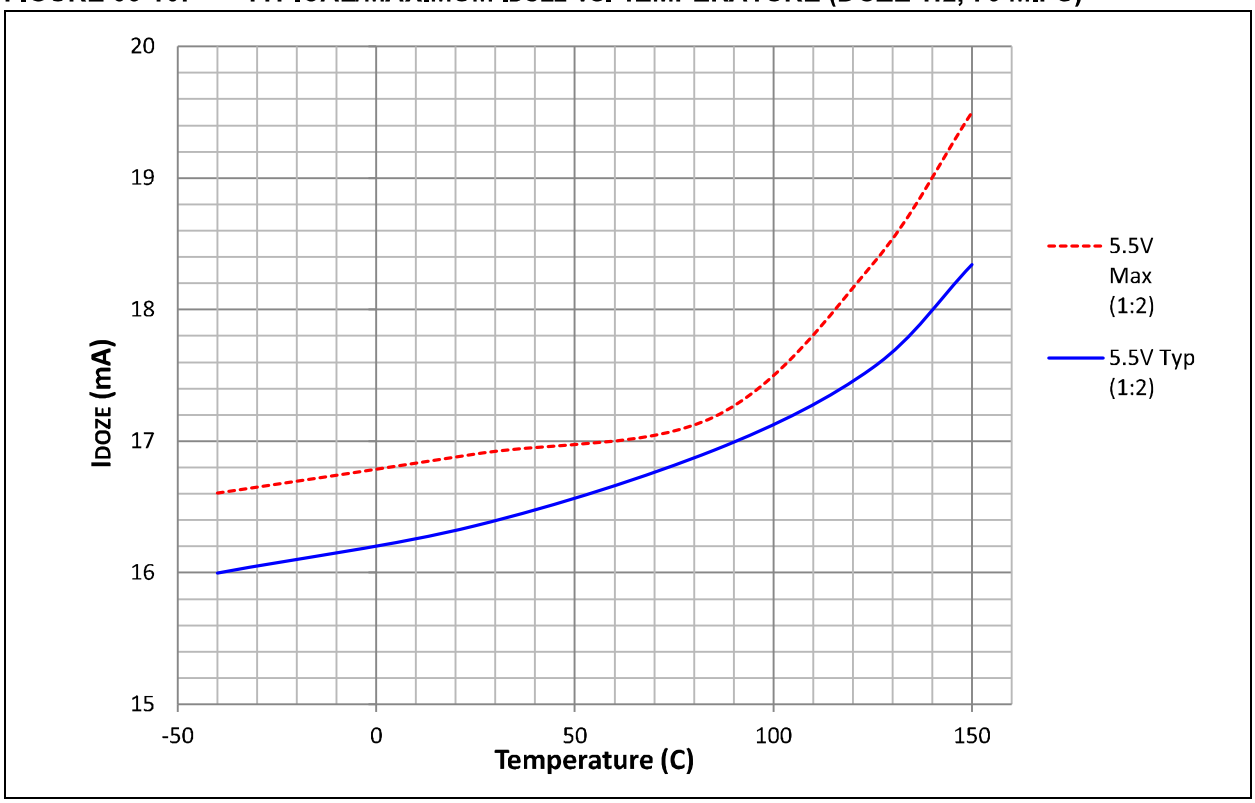


FIGURE 33-11: TYPICAL IDOZE vs. VDD (DOZE 1:128, 70 MIPS)

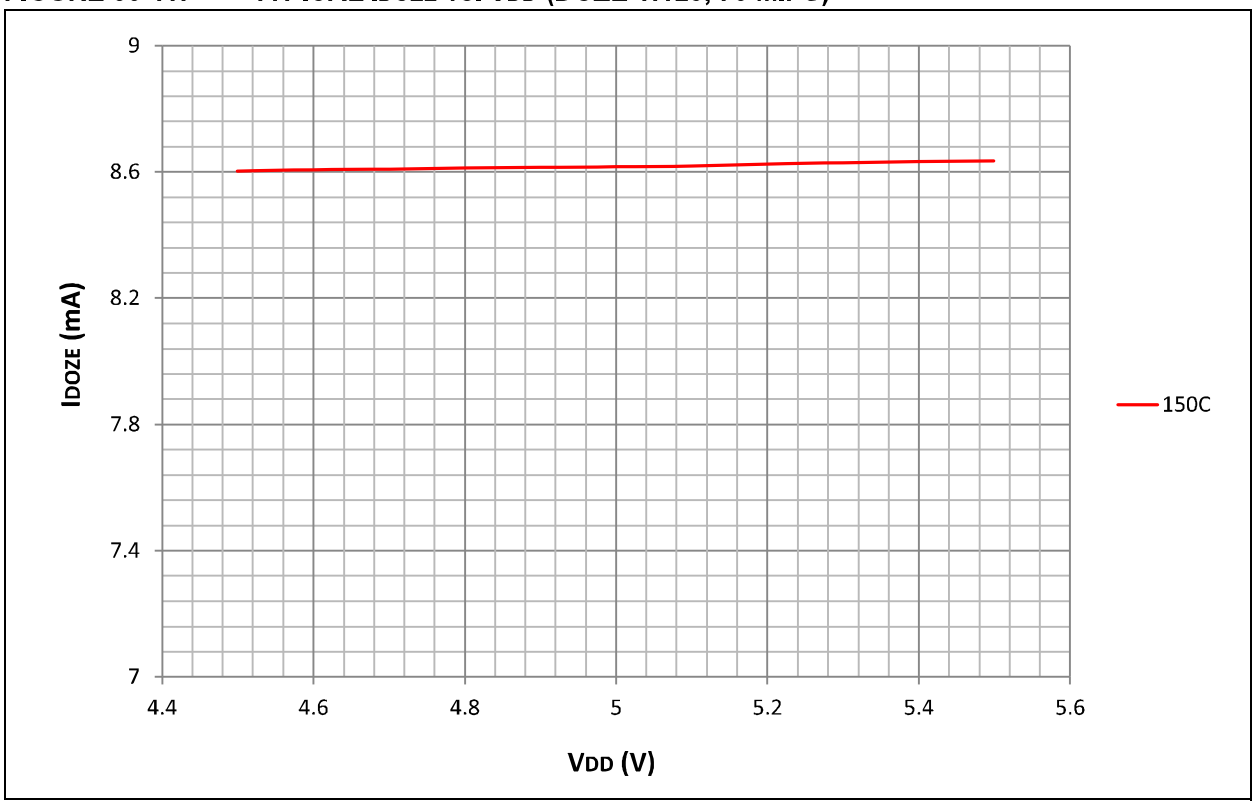
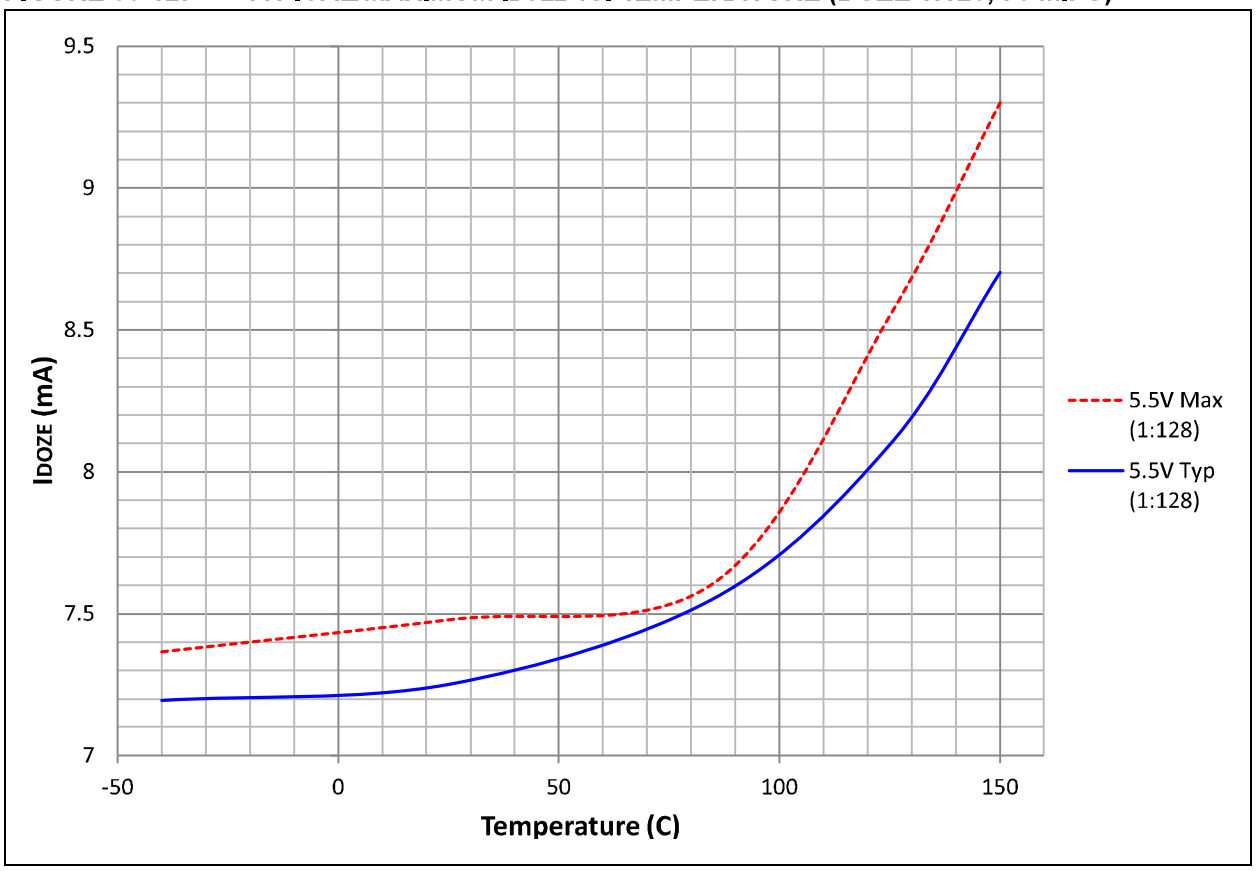


FIGURE 33-12: TYPICAL/MAXIMUM IDOZE vs. TEMPERATURE (DOZE 1:128, 70 MIPS)



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33.4 IPD

FIGURE 33-13: TYPICAL IPD vs. VDD

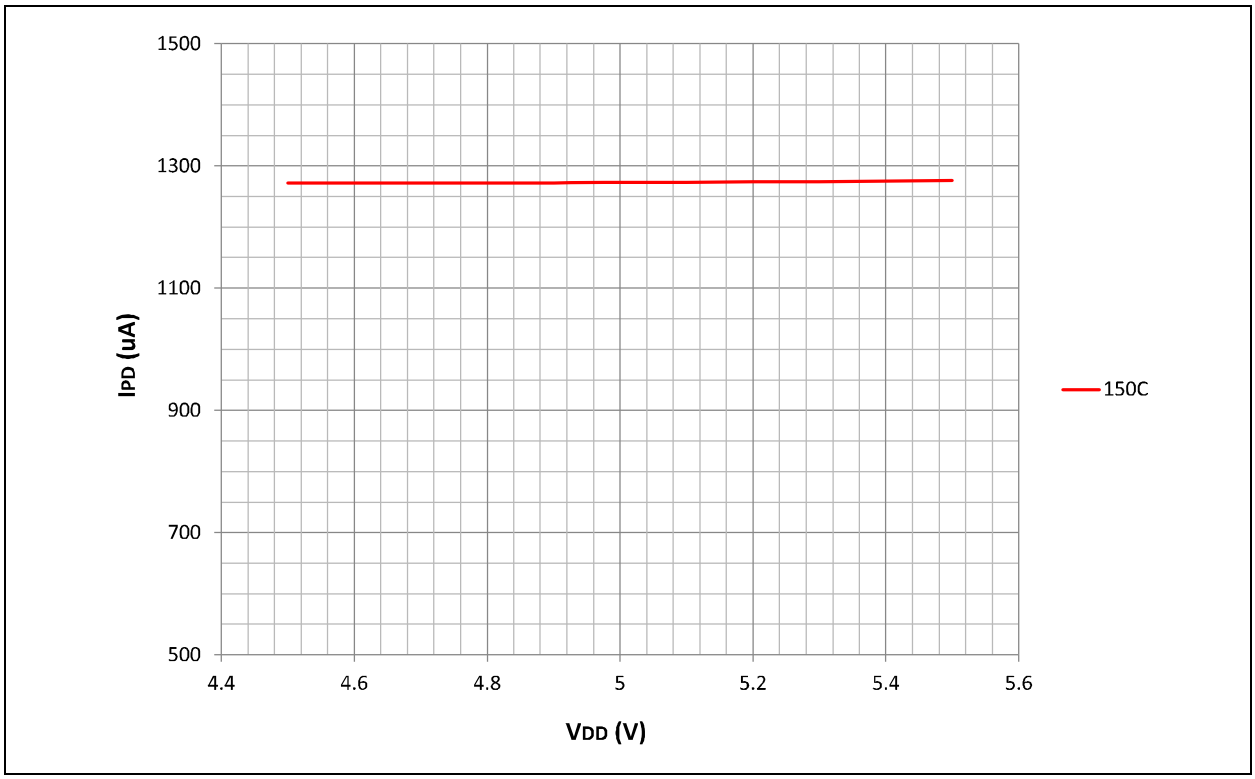


FIGURE 33-14: TYPICAL/MAXIMUM IPD vs. TEMPERATURE

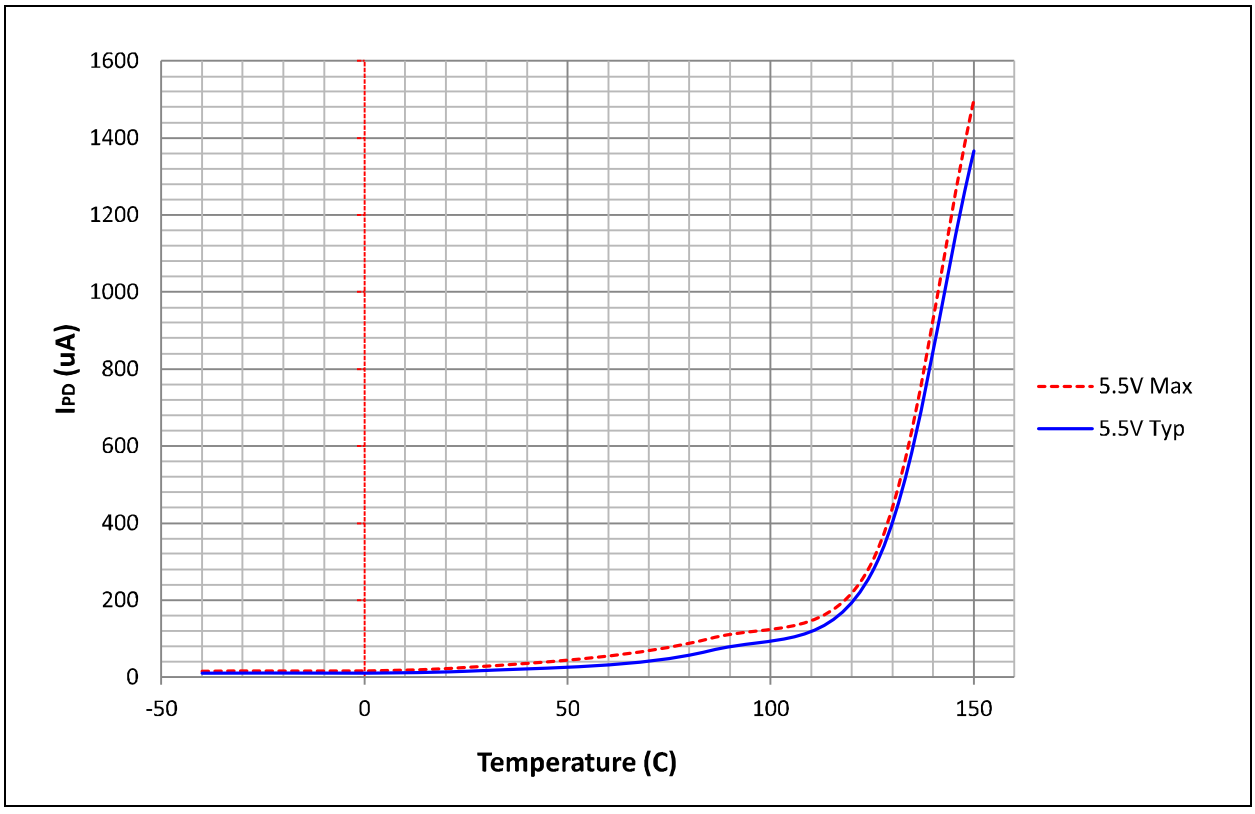
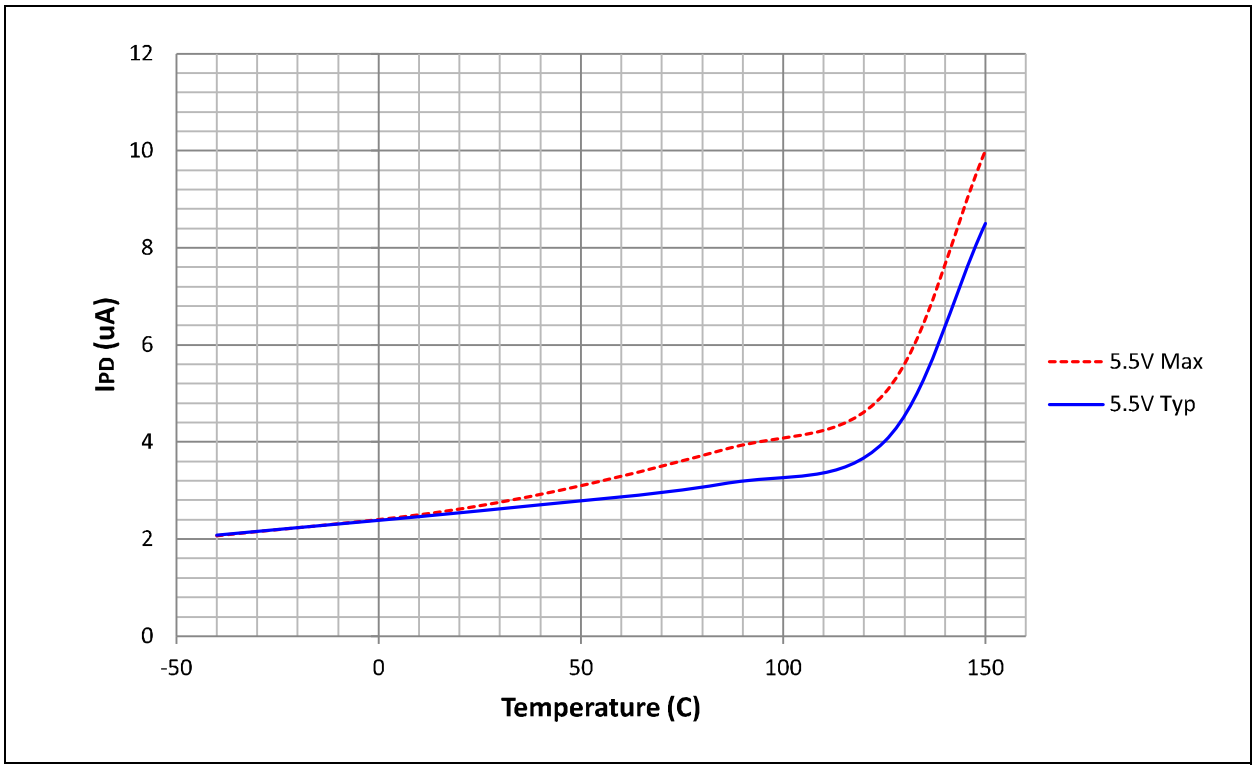
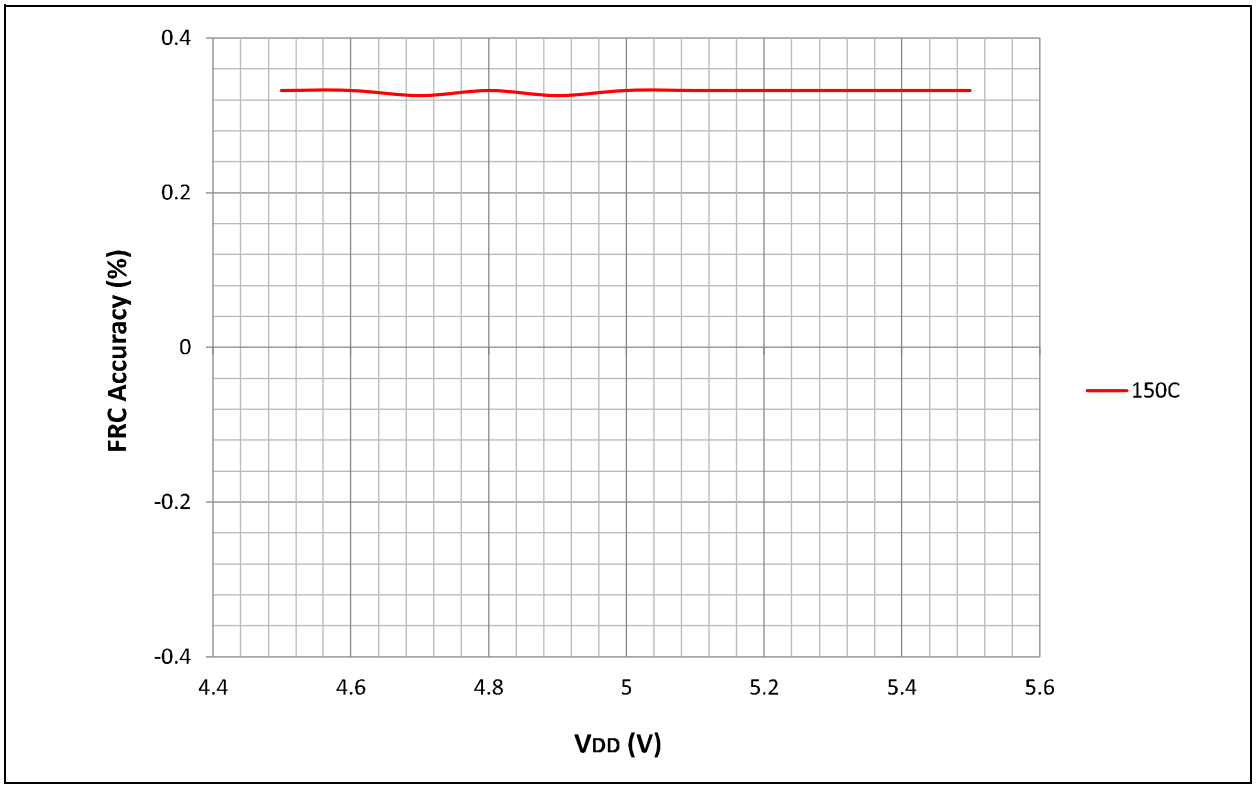


FIGURE 33-15: TYPICAL/MAXIMUM ΔIWDT vs. TEMPERATURE



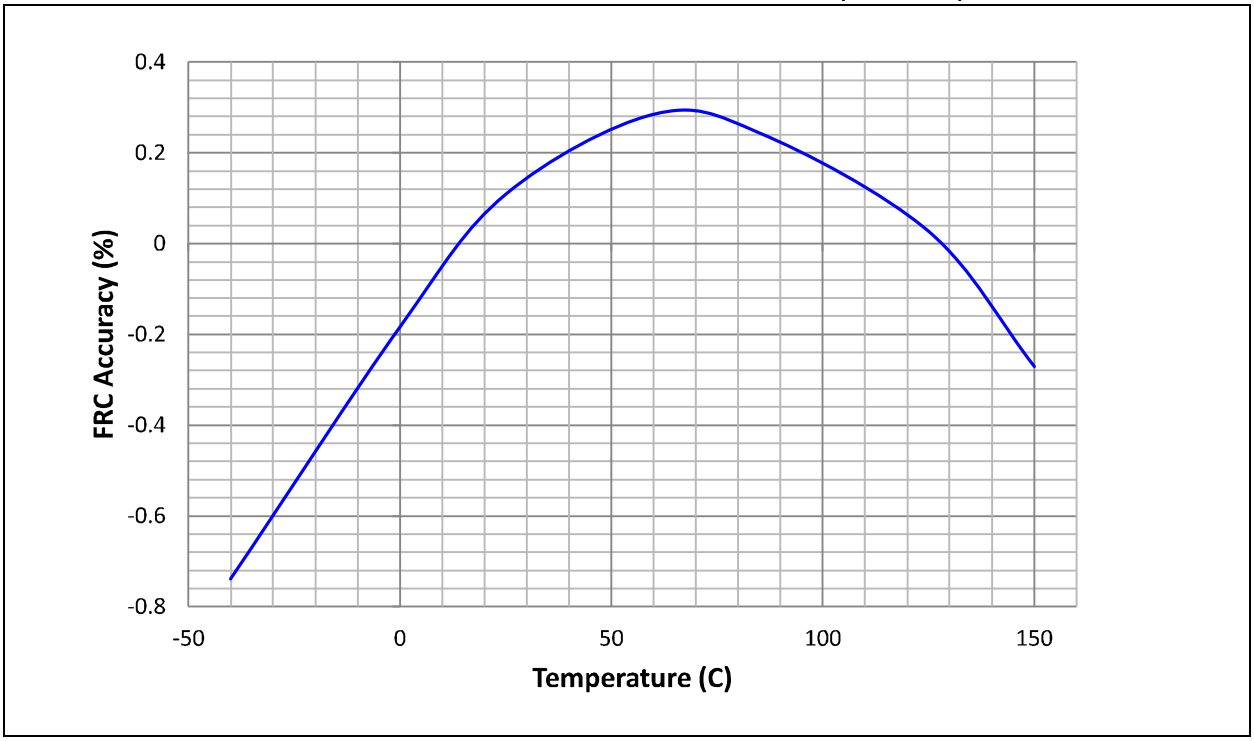
33.5 FRC

FIGURE 33-16: TYPICAL FRC ACCURACY vs. VDD



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FIGURE 33-17: TYPICAL FRC ACCURACY vs. TEMPERATURE (5.5V VDD)



33.6 LPRC

FIGURE 33-18: TYPICAL LPRC ACCURACY vs. VDD

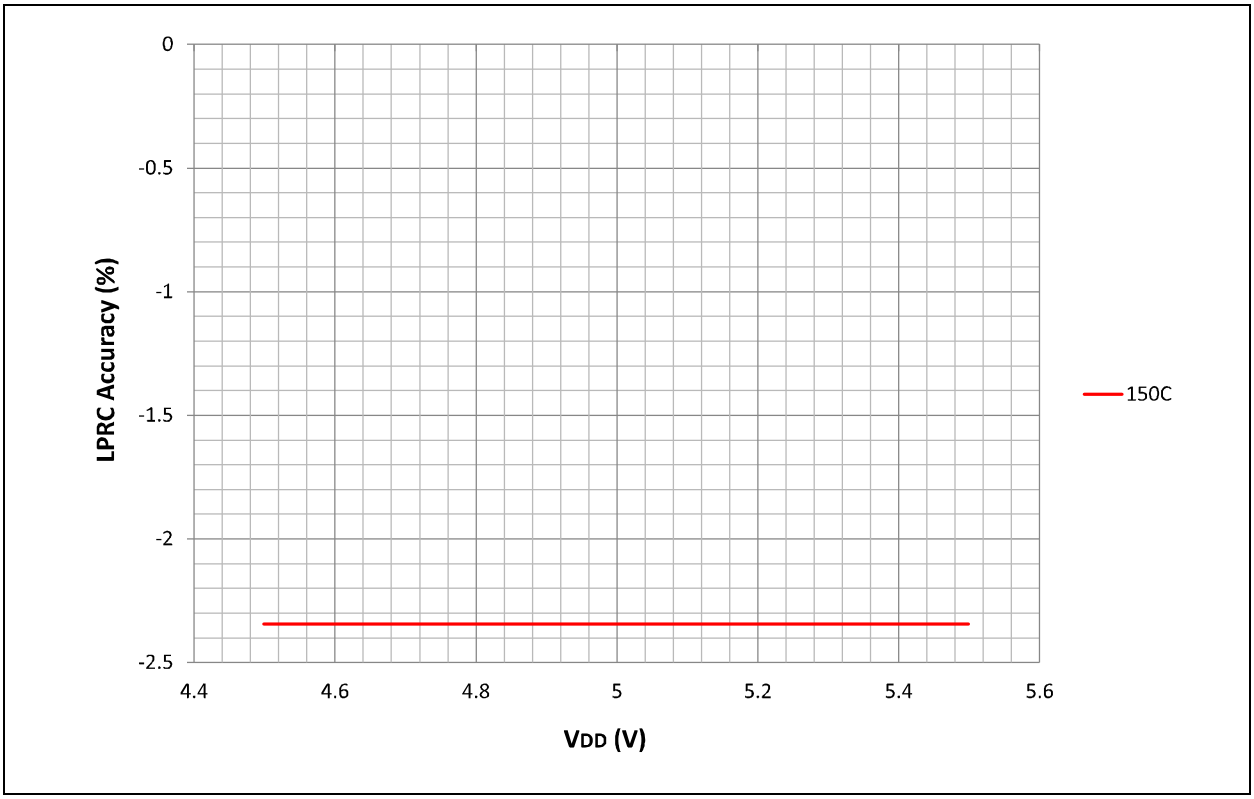
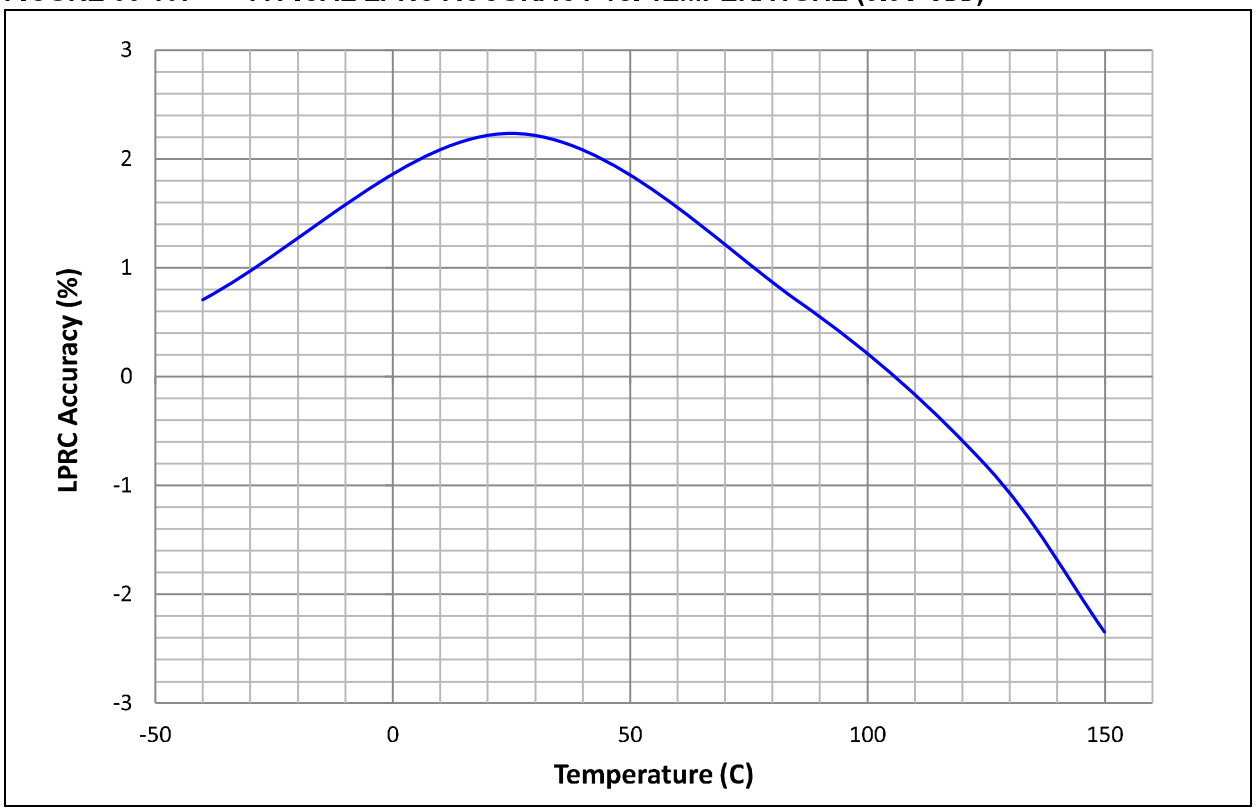
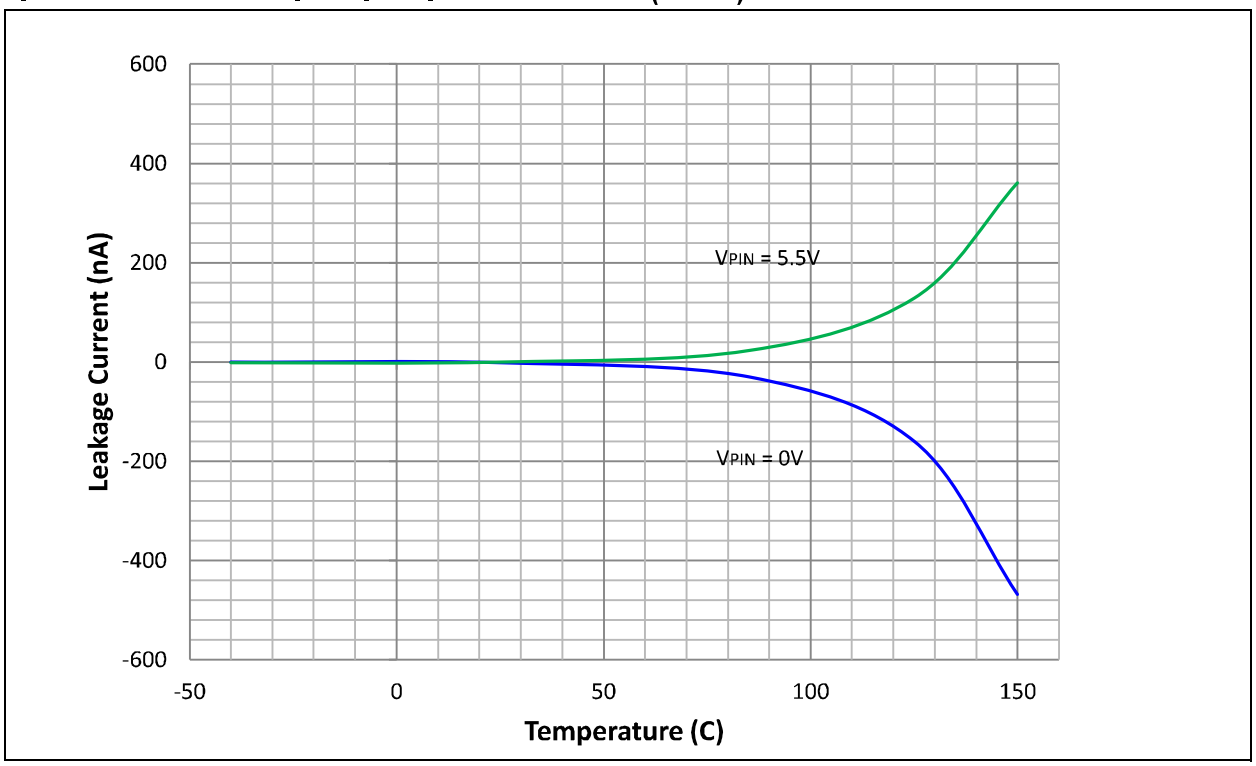


FIGURE 33-19: TYPICAL LPRC ACCURACY vs. TEMPERATURE (5.5V VDD)



33.7 Leakage Current

FIGURE 33-20: TYPICAL IIL vs. TEMPERATURE ($\overline{MCLR}$)



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FIGURE 33-21: TYPICAL I_{IL} vs. TEMPERATURE (OSC1)

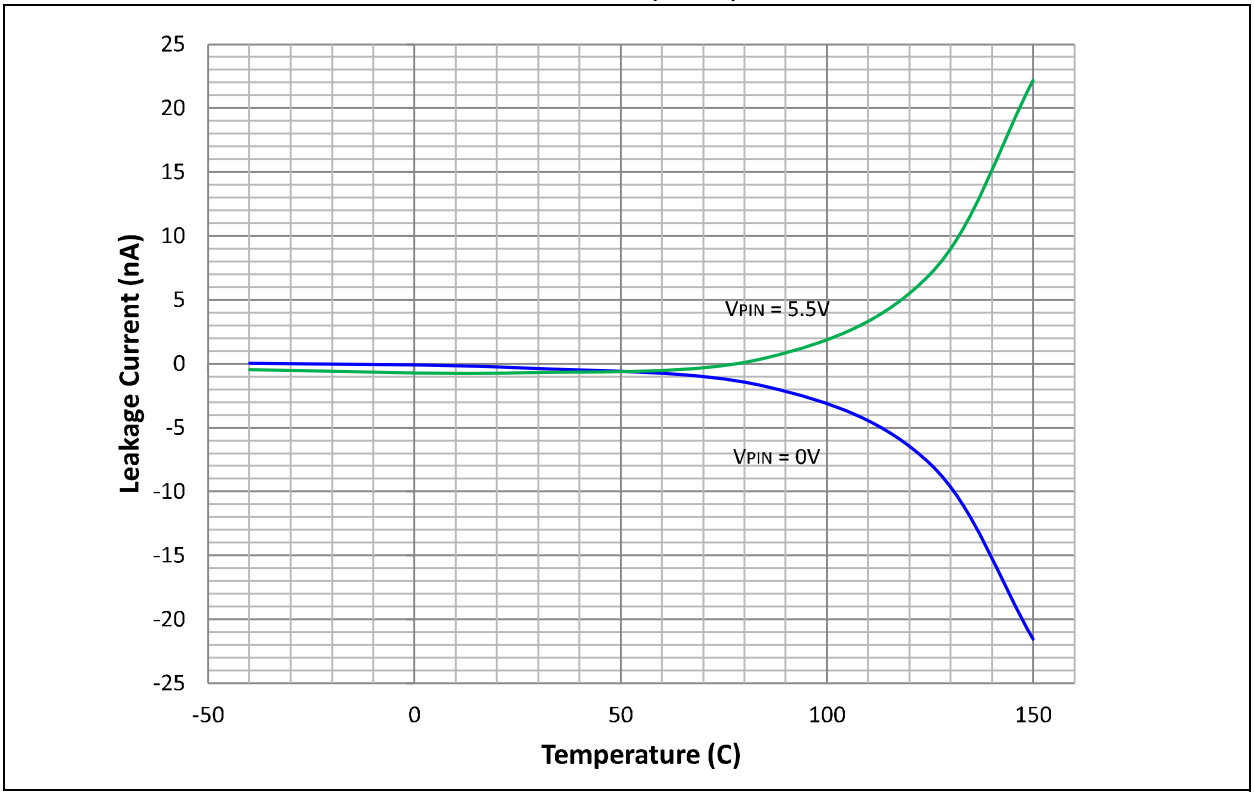
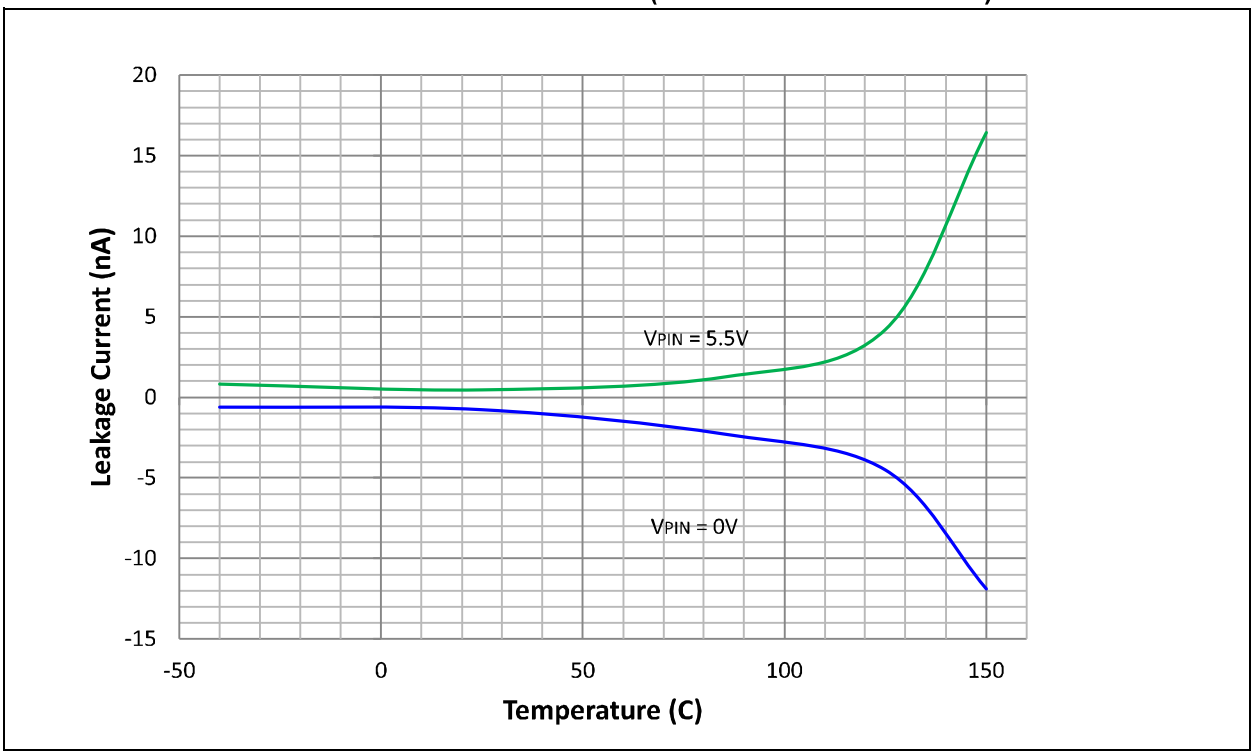


FIGURE 33-22: TYPICAL I_{IL} vs. TEMPERATURE (GENERAL PURPOSE I/Os)



33.8 Pull-up/Pull-Down Current

FIGURE 33-23: TYPICAL PULL-DOWN CURRENT (VPIN = 5.5V) vs. TEMPERATURE

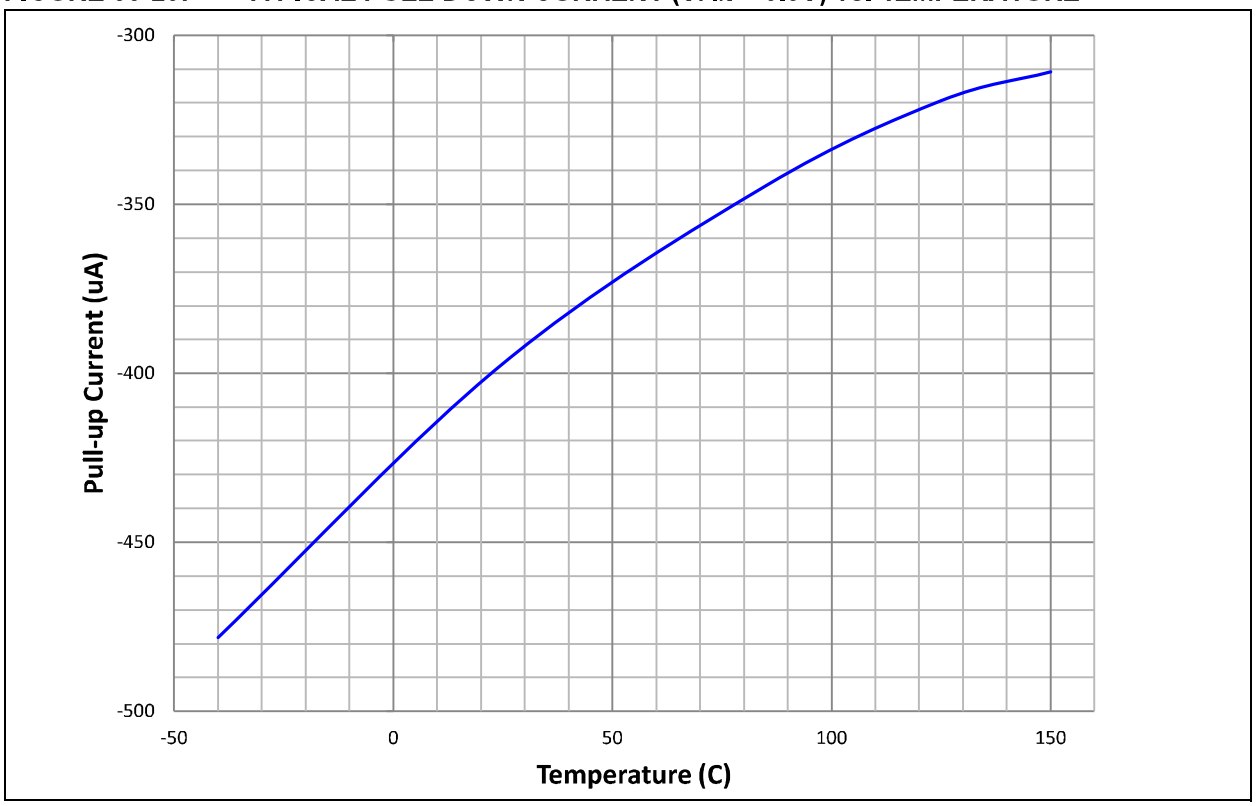
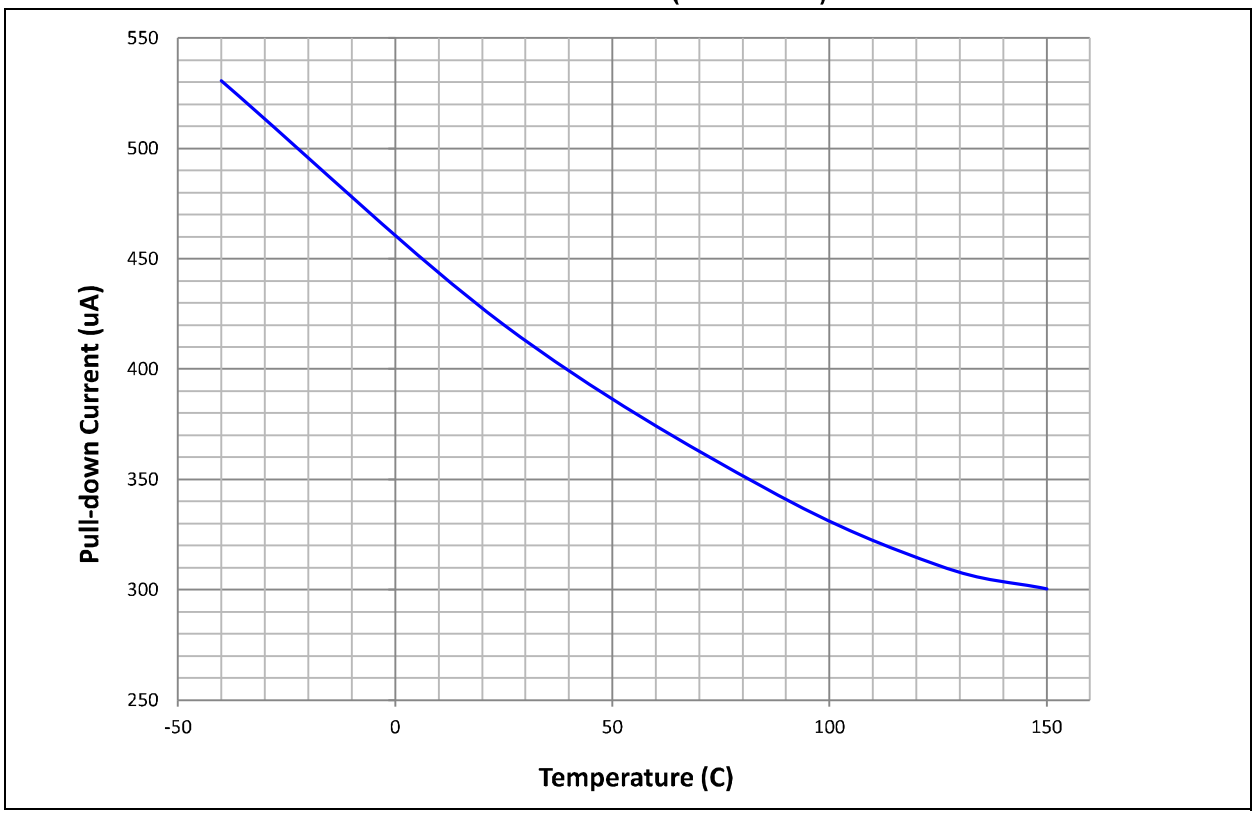


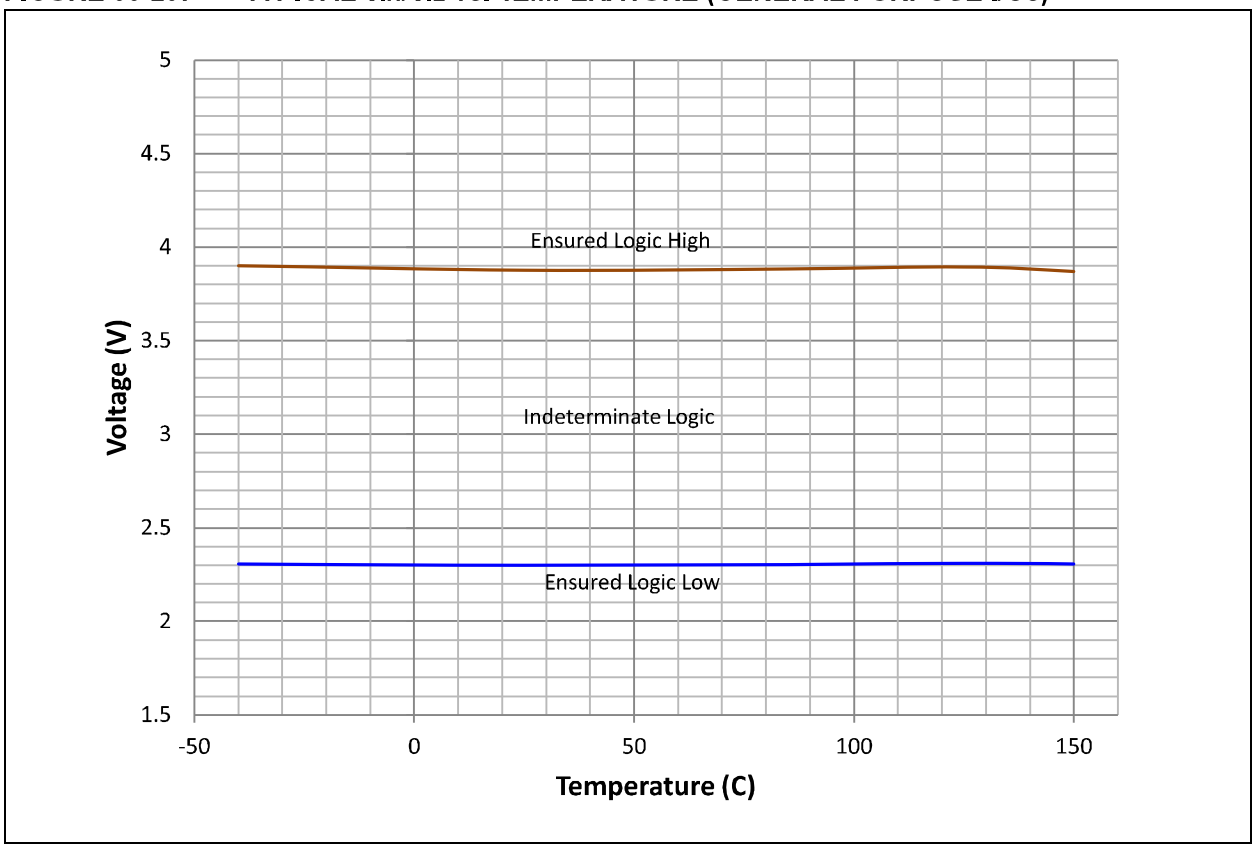
FIGURE 33-24: TYPICAL PULL-DOWN CURRENT (VPIN = 5.5V) vs. TEMPERATURE



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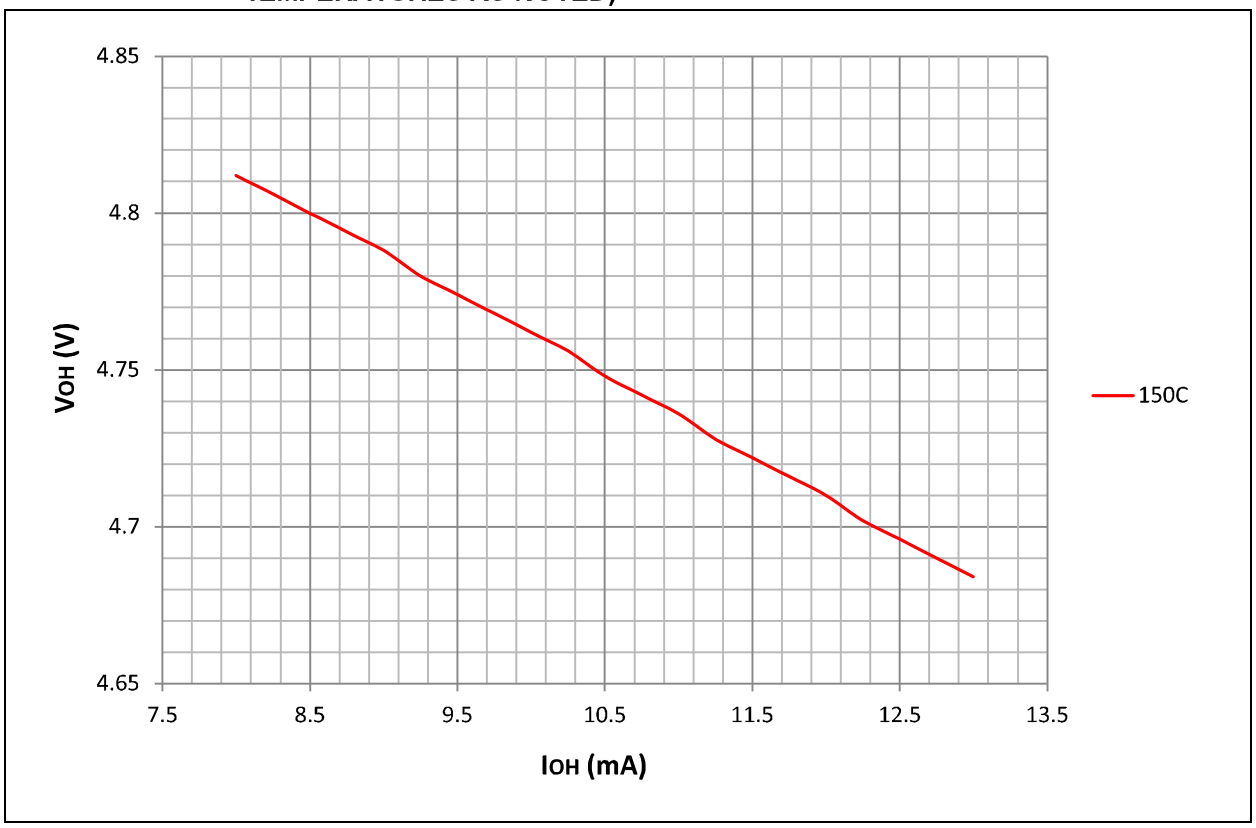
33.9 Voltage Input High (VIH) – Voltage Input Low (VIL)

FIGURE 33-25: TYPICAL VIH/VIL vs. TEMPERATURE (GENERAL PURPOSE I/Os)



33.10 Voltage Output Low (VOL) – Voltage Output High (VOH)

FIGURE 33-26: TYPICAL VOH 8x DRIVER PINS vs. IOH (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



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FIGURE 33-27: TYPICAL V_{OH} 4x DRIVER PINS vs. I_{OH} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

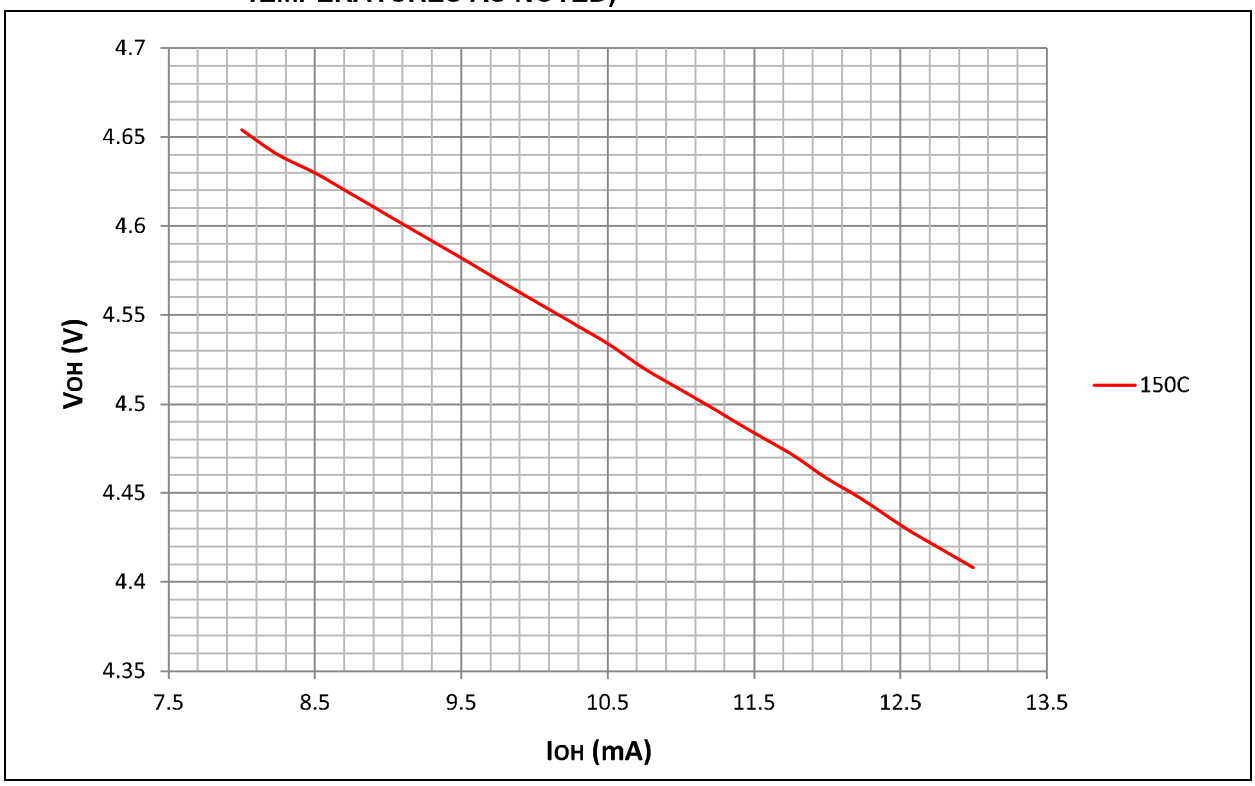


FIGURE 33-28: TYPICAL V_{OL} 8x DRIVER PINS vs. I_{OL} (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)

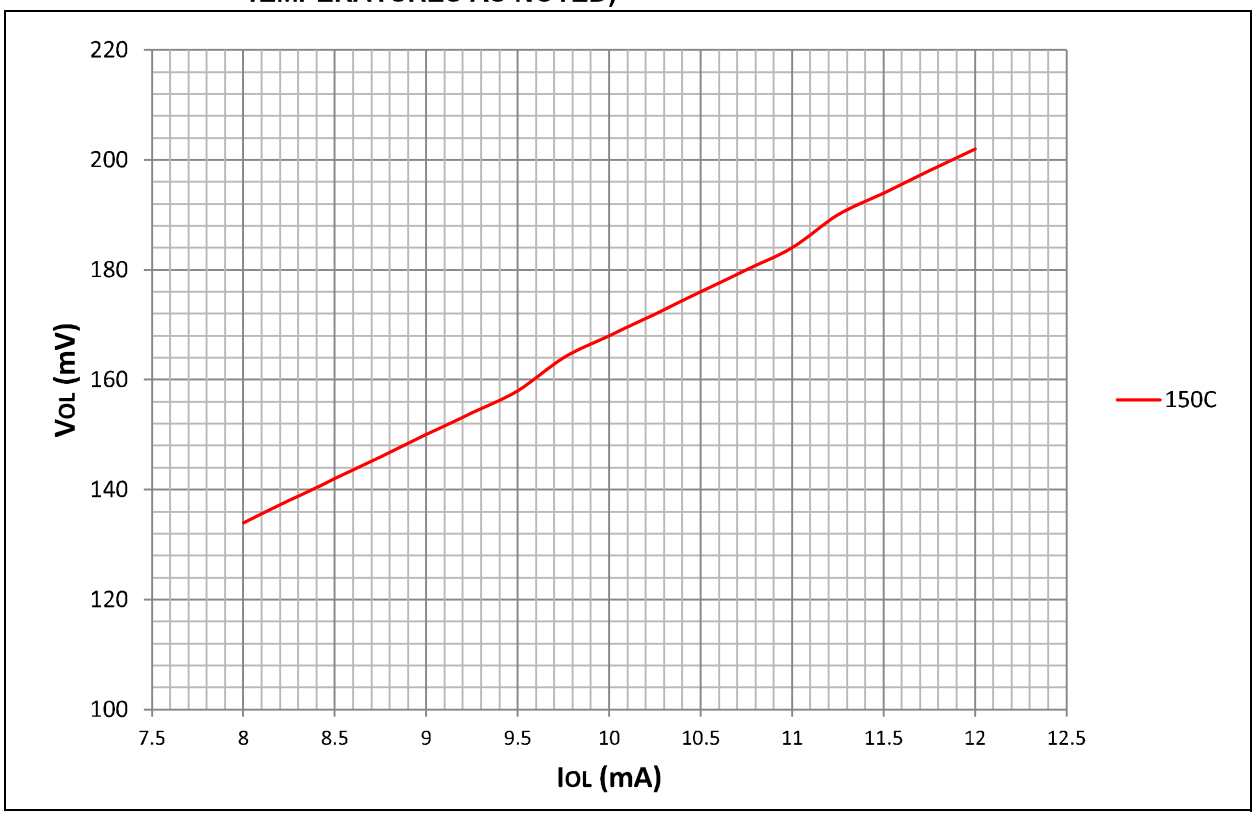
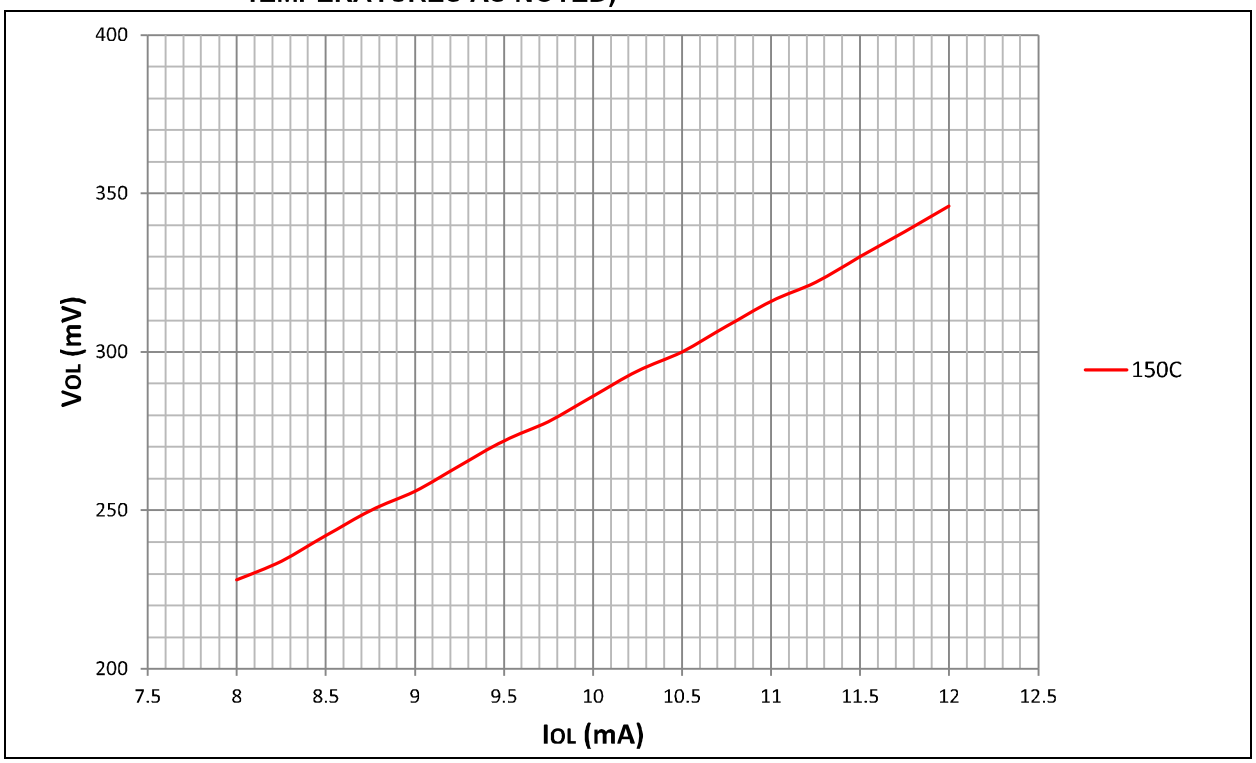
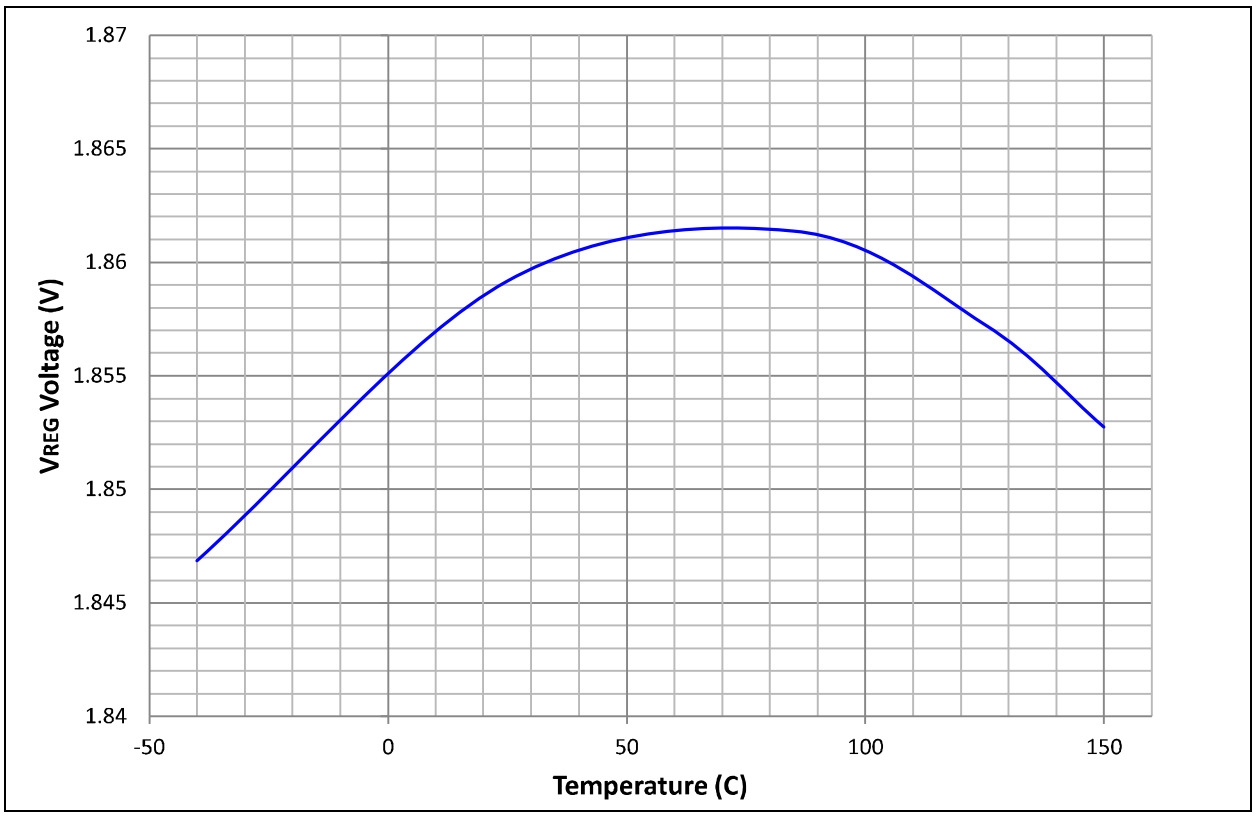


FIGURE 33-29: TYPICAL VOL 4x DRIVER PINS vs. IOL (GENERAL PURPOSE I/Os, TEMPERATURES AS NOTED)



33.11 VREG

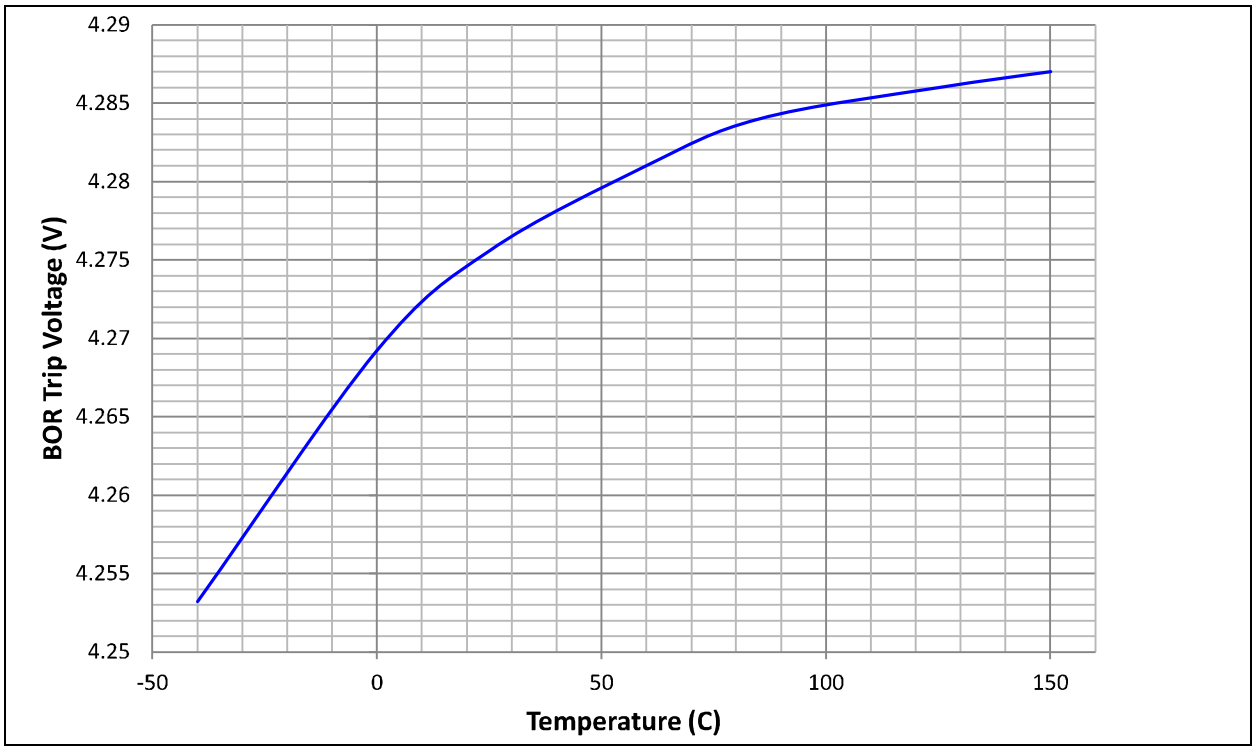
FIGURE 33-30: TYPICAL REGULATOR VOLTAGE vs. TEMPERATURE



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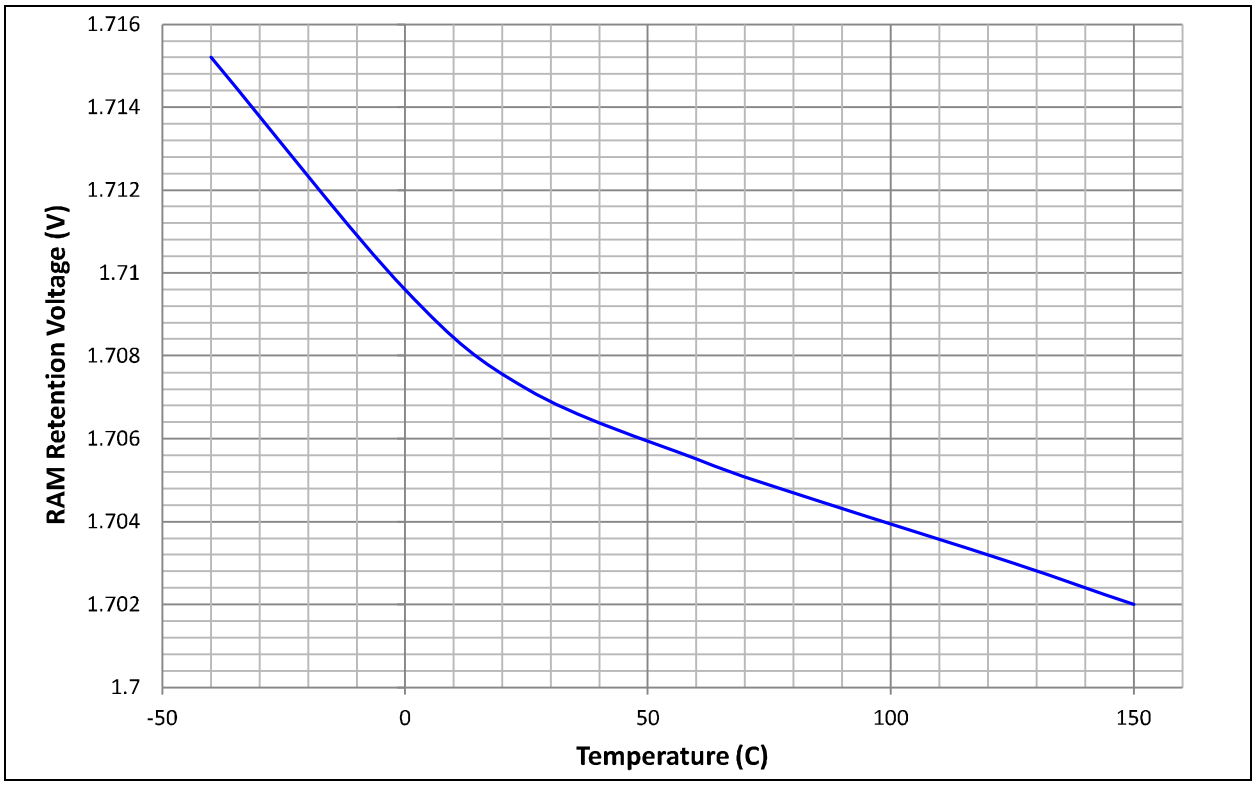
33.12 VBOR

FIGURE 33-31: TYPICAL BOR TRIP RANGE vs. TEMPERATURE



33.13 RAM Retention

FIGURE 33-32: TYPICAL RAM RETENTION VOLTAGE vs. TEMPERATURE



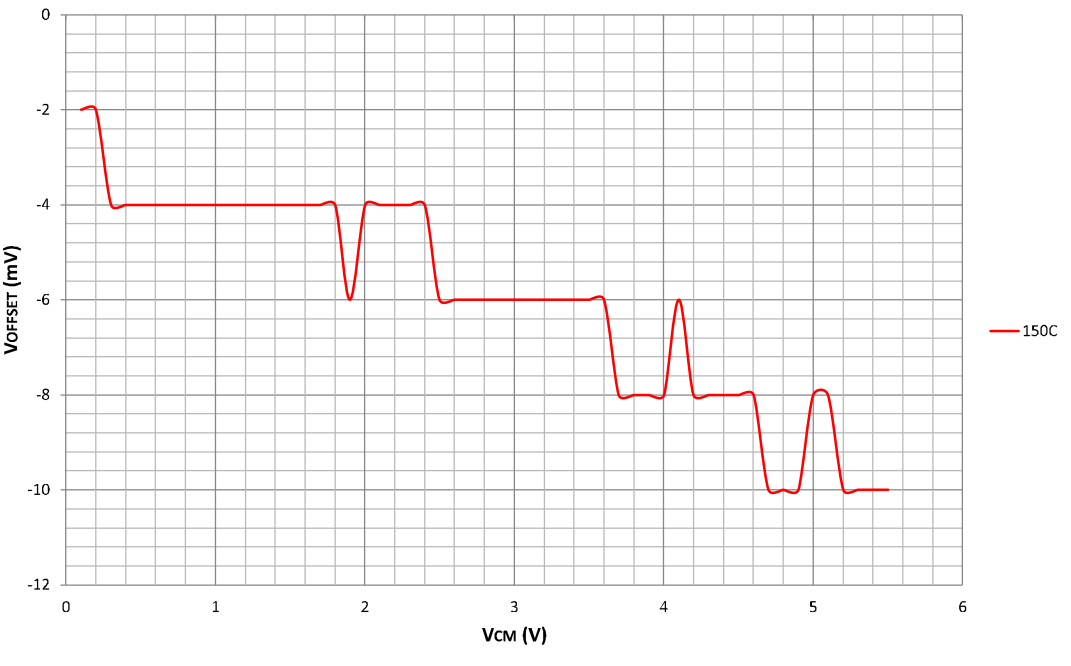
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33.14 Comparator Op Amp Offset

FIGURE 33-33: TYPICAL COMPARATOR OFFSET vs. VCM



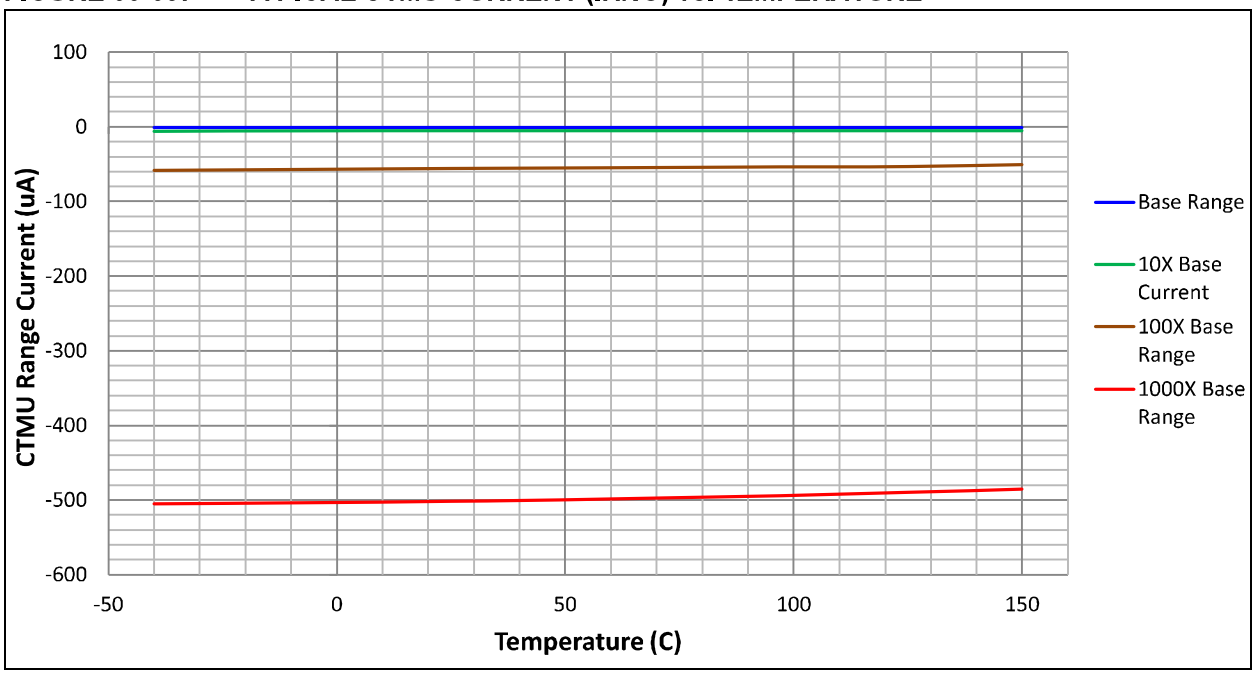
FIGURE 33-34: TYPICAL OP AMP OFFSET vs. VCM



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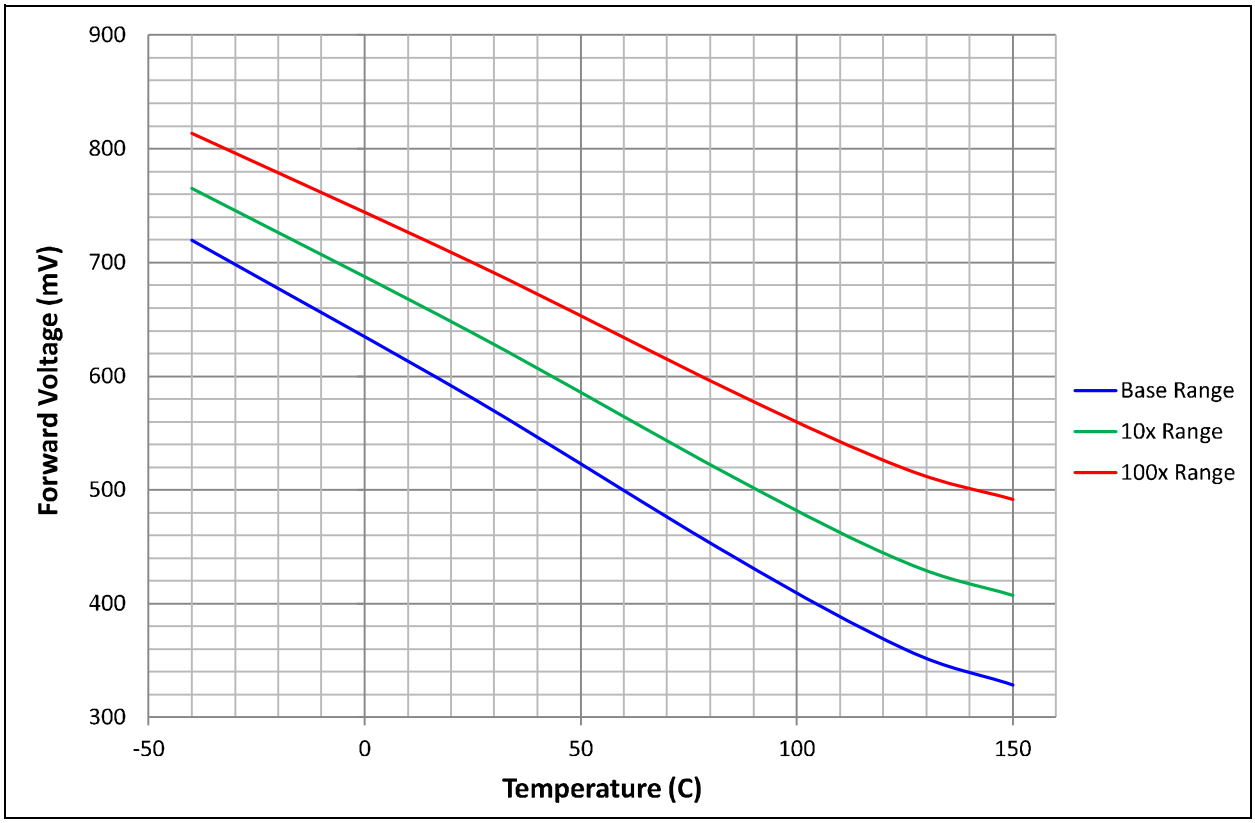
33.15 CTMU Current V/S Temperature

FIGURE 33-35: TYPICAL CTMU CURRENT (IRNG) vs. TEMPERATURE



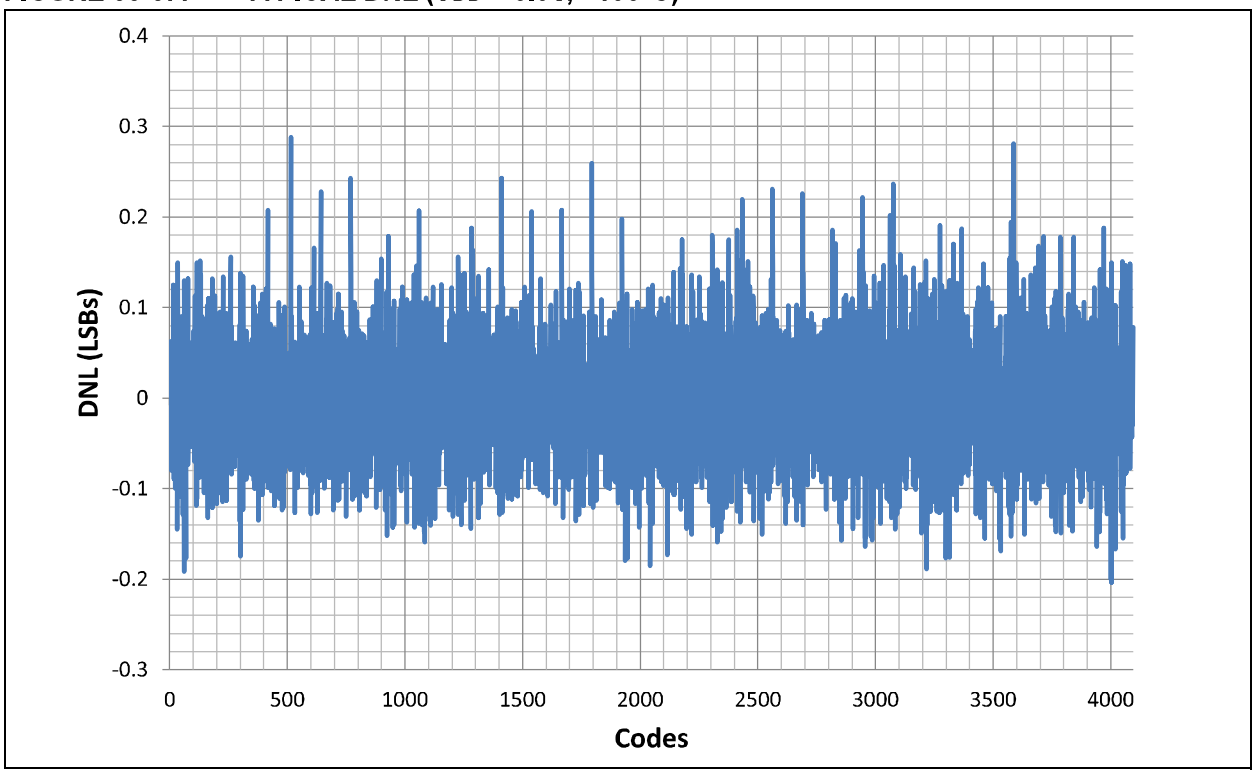
33.16 CTMU Temperature Forward Diode (V)

FIGURE 33-36: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE vs. TEMPERATURE



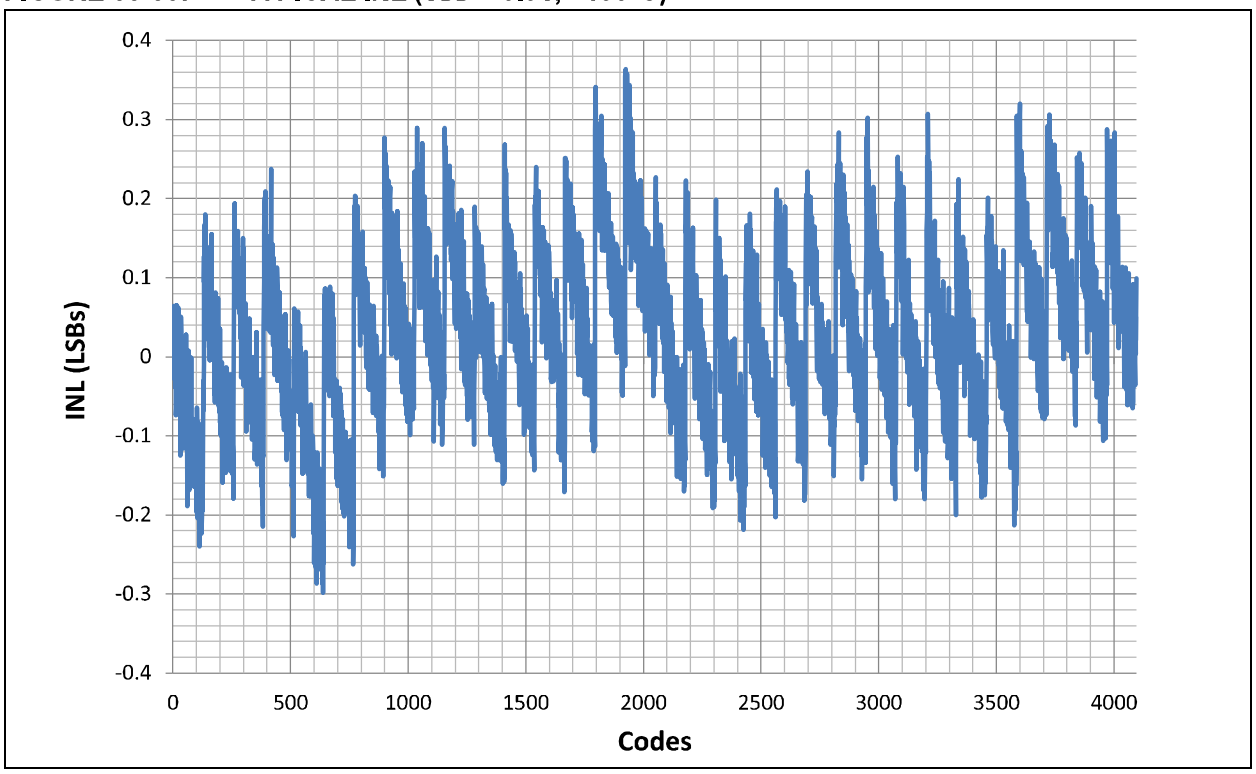
33.17 ADC DNL

FIGURE 33-37: TYPICAL DNL (VDD = 5.5V, +150°C)



33.18 ADC INL

FIGURE 33-38: TYPICAL INL (VDD = 5.5V, +150°C)



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33.19 ADC Gain Offset Error

FIGURE 33-39: TYPICAL ADC GAIN ERROR vs. TEMPERATURE

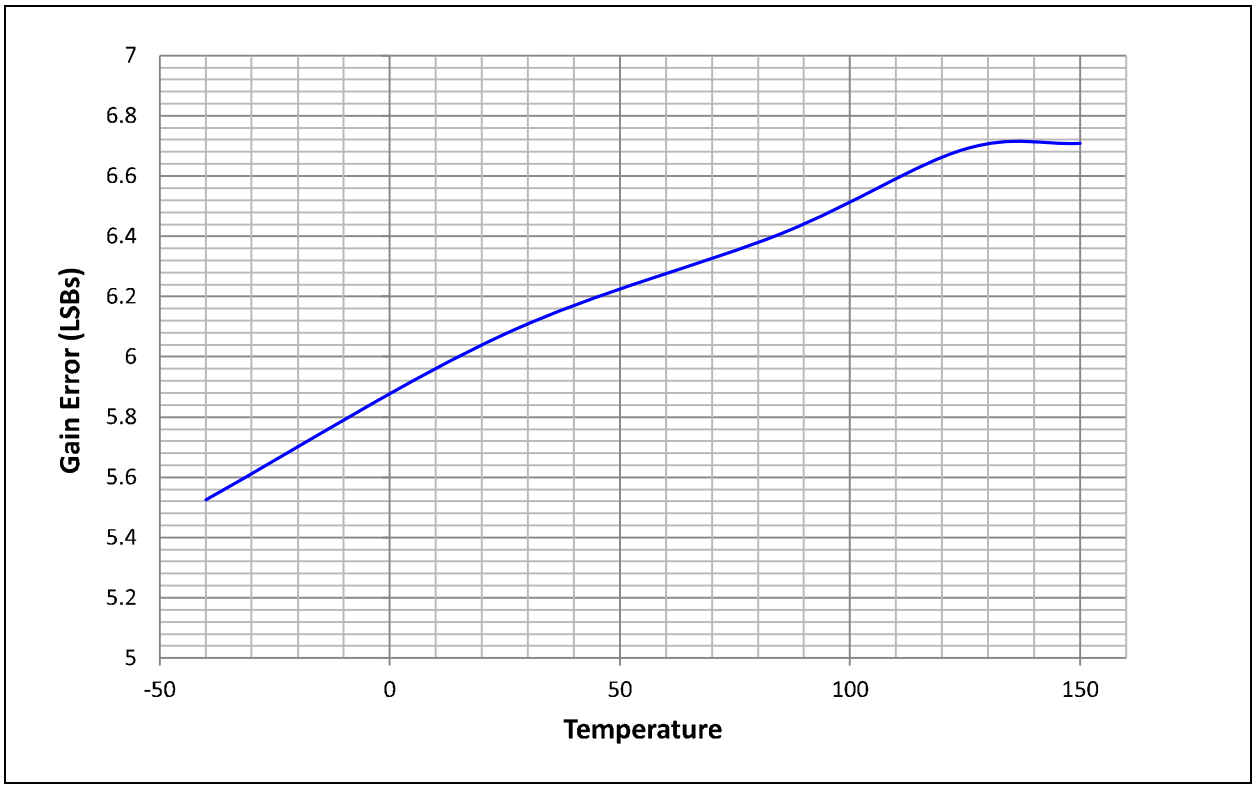
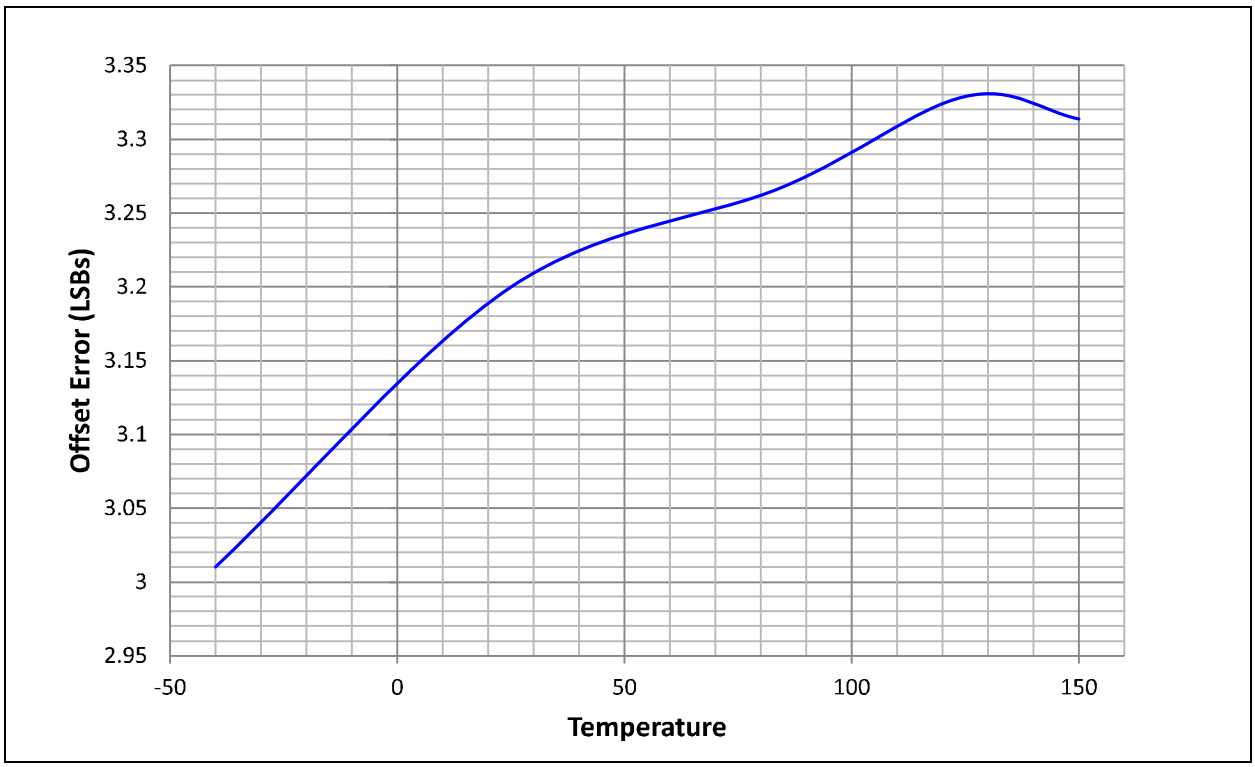


FIGURE 33-40: TYPICAL ADC OFFSET ERROR vs. TEMPERATURE



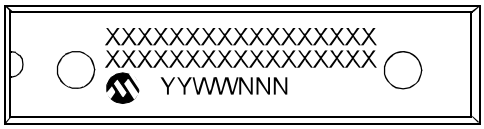
NOTES:

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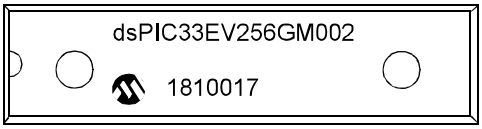
34.0 PACKAGING INFORMATION

34.1 Package Marking Information

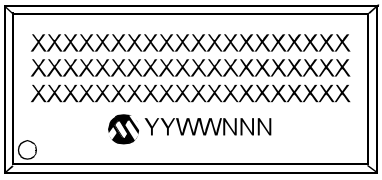
28-Lead SPDIP (.300")



Example



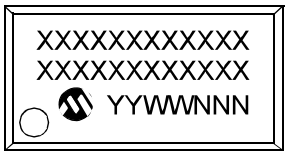
28-Lead SOIC (.300")



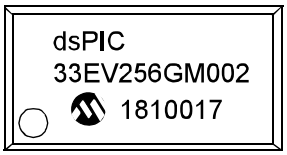
Example



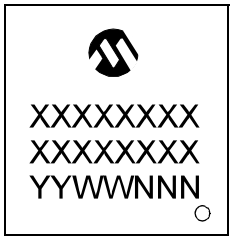
28-Lead SSOP



Example



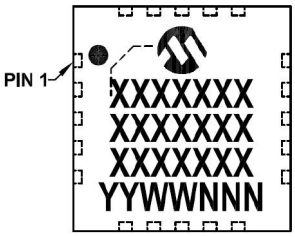
28-Lead QFN-S (6x6x0.9 mm)



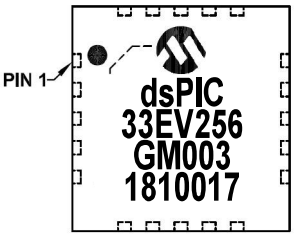
Example



36-Lead UQFN (5x5 mm)



Example

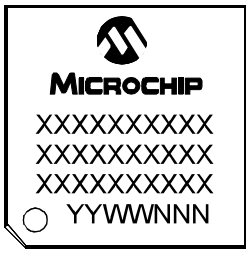


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

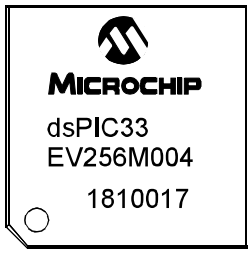
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

34.1 Package Marking Information (Continued)

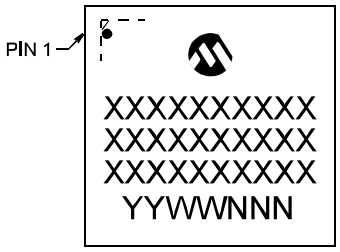
44-Lead TQFP (10x10x1 mm)



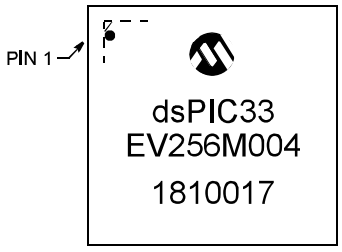
Example



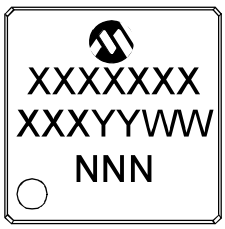
44-Lead QFN (8x8 mm)



Example



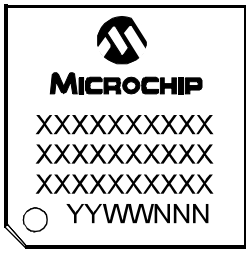
48-Lead TQFP (7x7x1.0 mm)



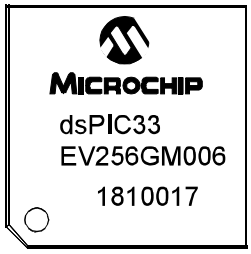
Example



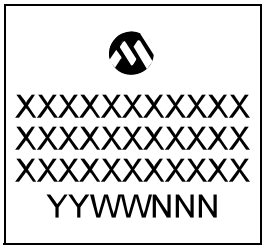
64-Lead TQFP (10x10x1 mm)



Example



64-Lead QFN (9x9x0.9 mm)



Example



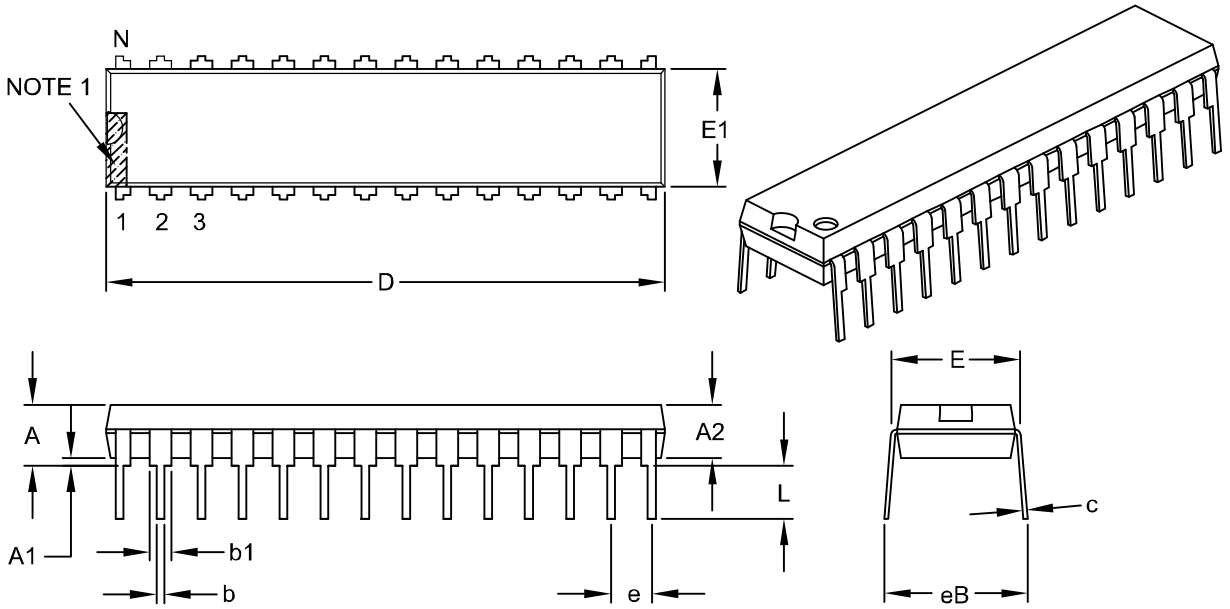
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34.2 Package Details

The following sections give the technical details of the packages.

28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.200
Molded Package Thickness	A2	.120	.135	.150
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.335
Molded Package Width	E1	.240	.285	.295
Overall Length	D	1.345	1.365	1.400
Tip to Seating Plane	L	.110	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.050	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

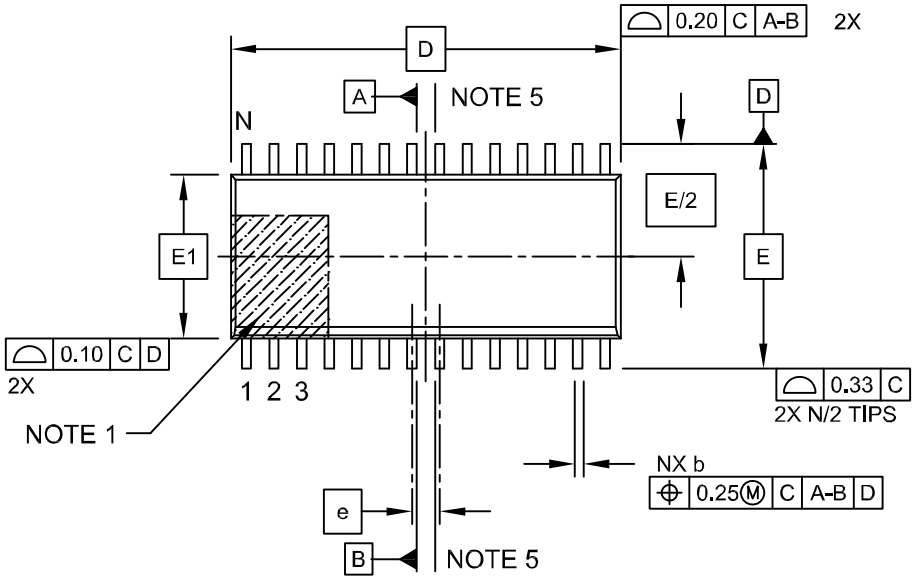
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

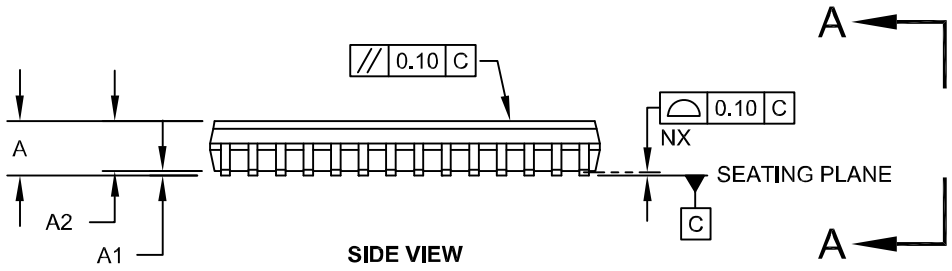
Microchip Technology Drawing C04-070B

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

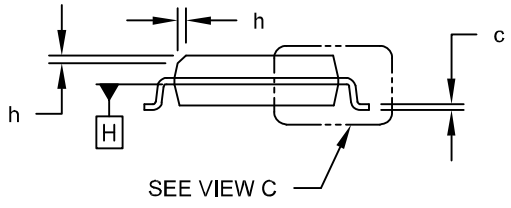
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



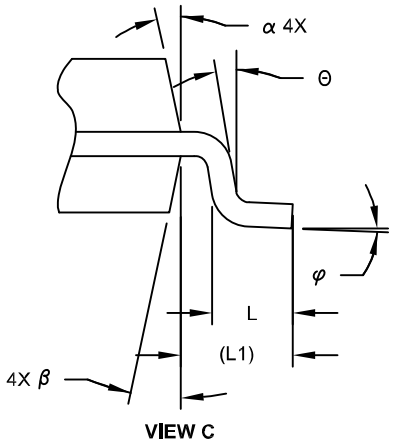
VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2

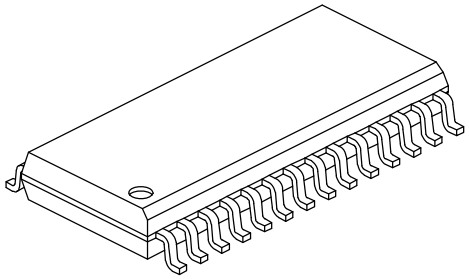
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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		17.90 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.18	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

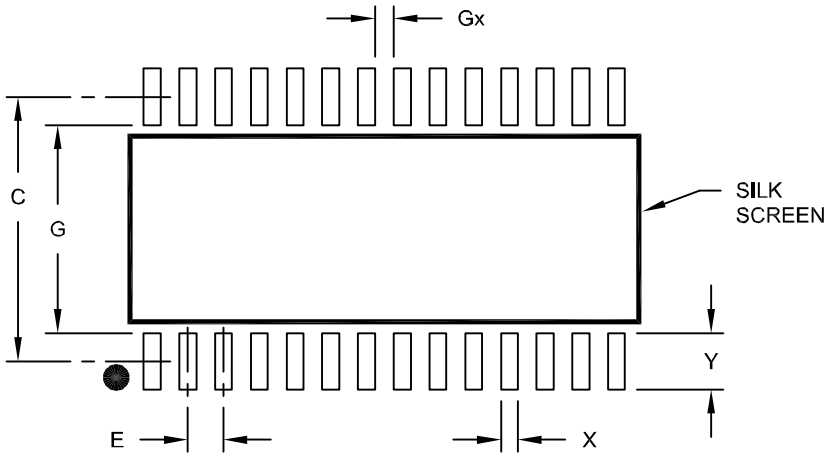
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2

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28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

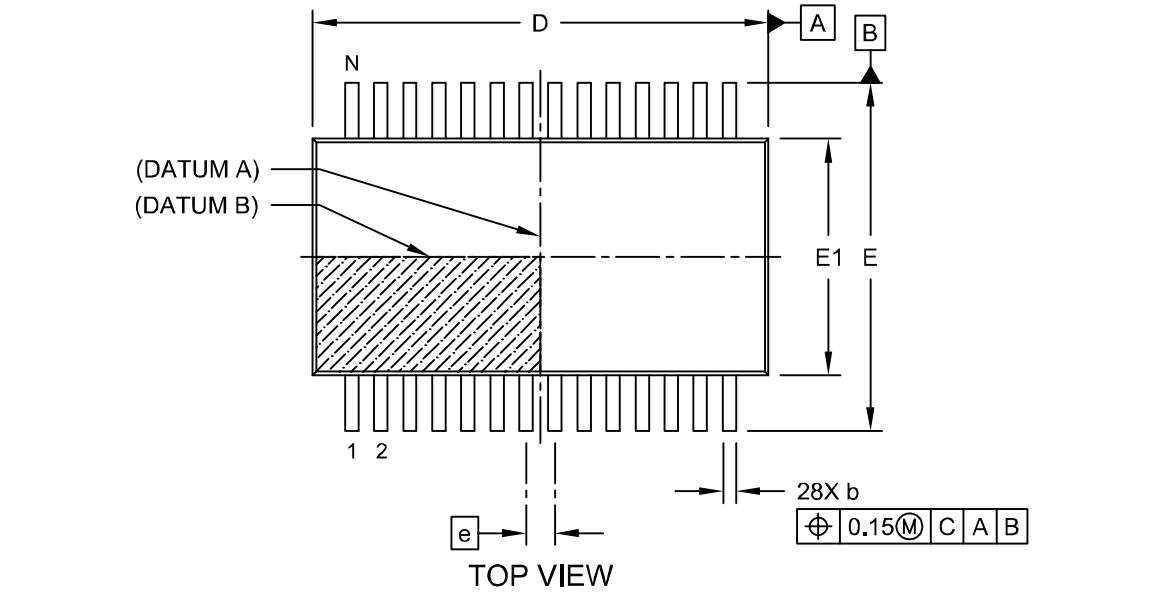
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

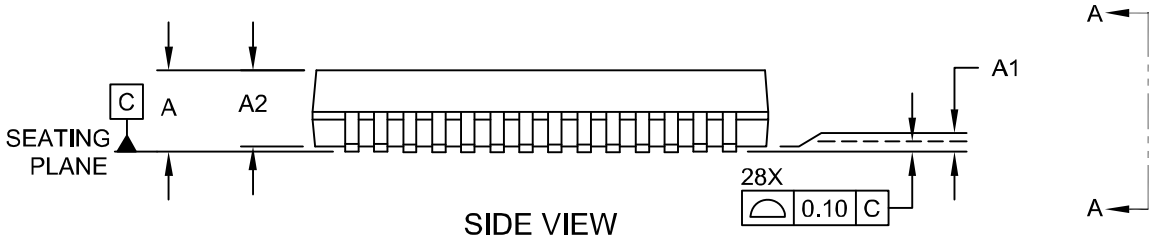
Microchip Technology Drawing No. C04-2052A

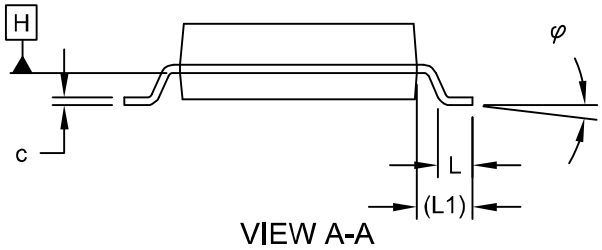
© 2013-2019 Microchip Technology Inc.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



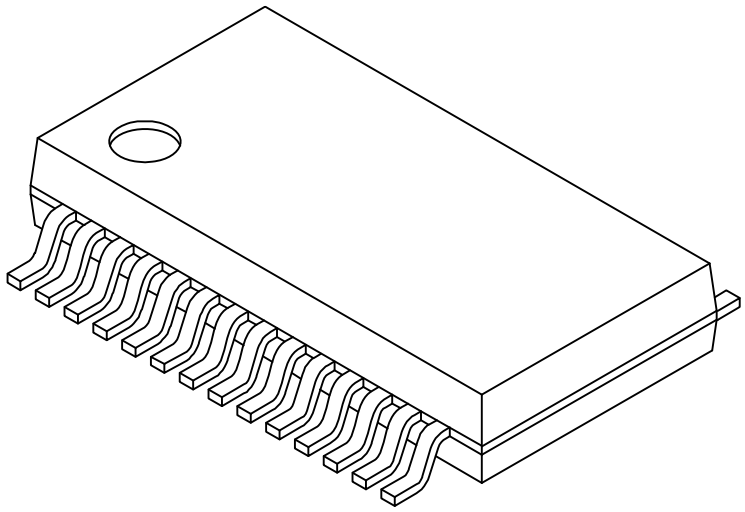




Microchip Technology Drawing C04-073 Rev C Sheet 1 of 2

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	-	-
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	-	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	-	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

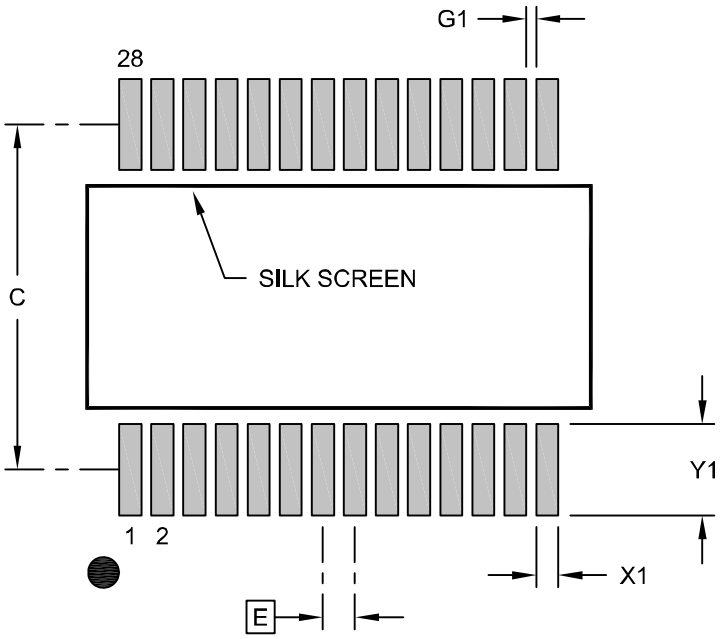
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073 Rev C Sheet 2 of 2

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28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.00	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.85
Contact Pad to Center Pad (X26)	G1	0.20		

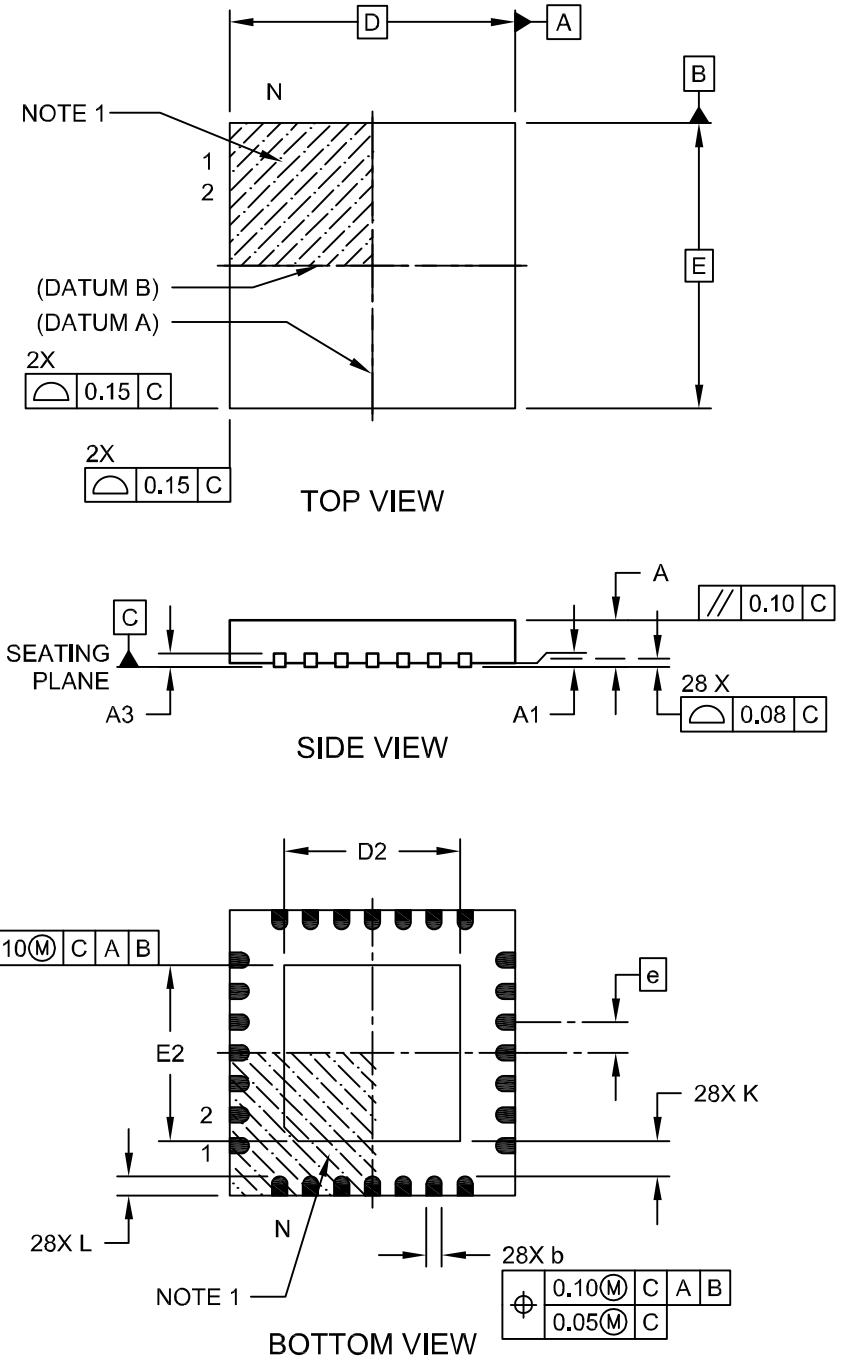
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2073 Rev B

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S]
With 0.40 mm Terminal Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

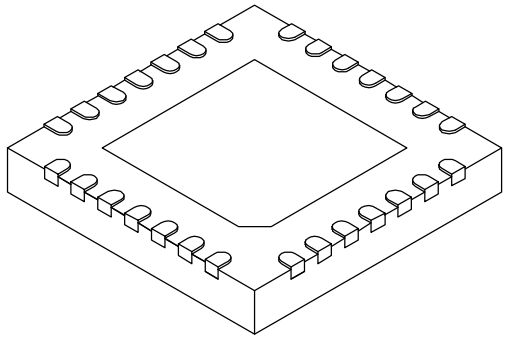


Microchip Technology Drawing C04-124C Sheet 1 of 2

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28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.70
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.70
Terminal Width	b	0.23	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and toleranding per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

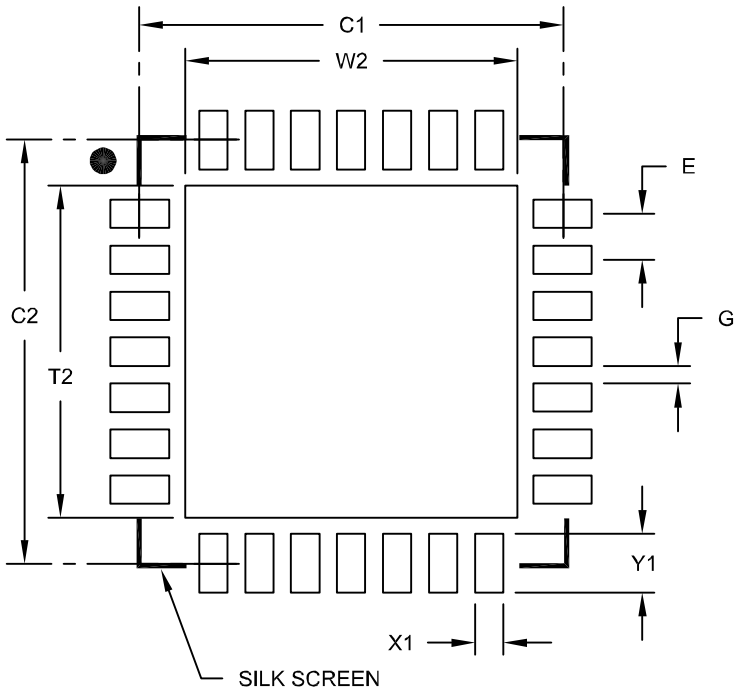
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2

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28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

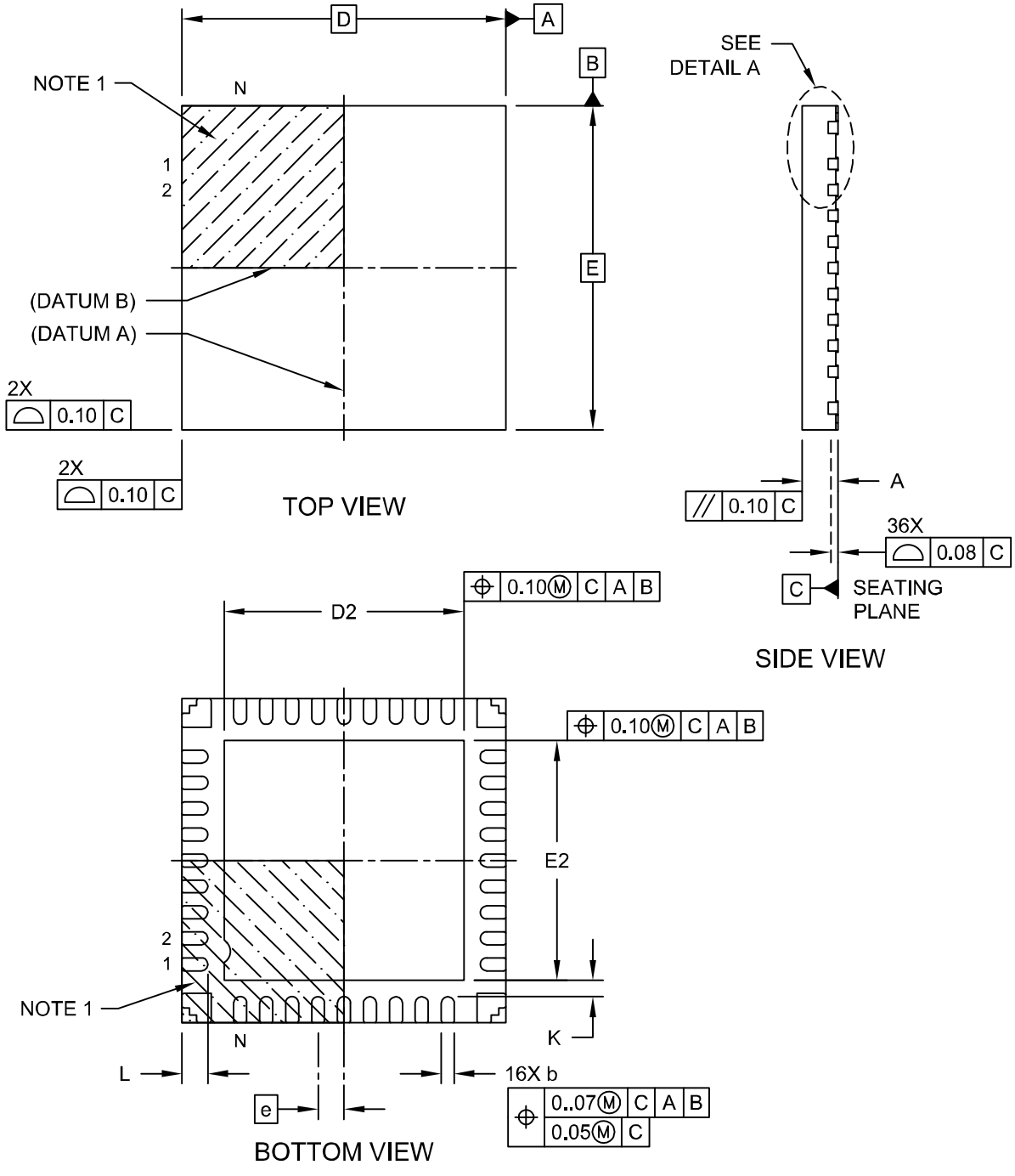
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

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36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

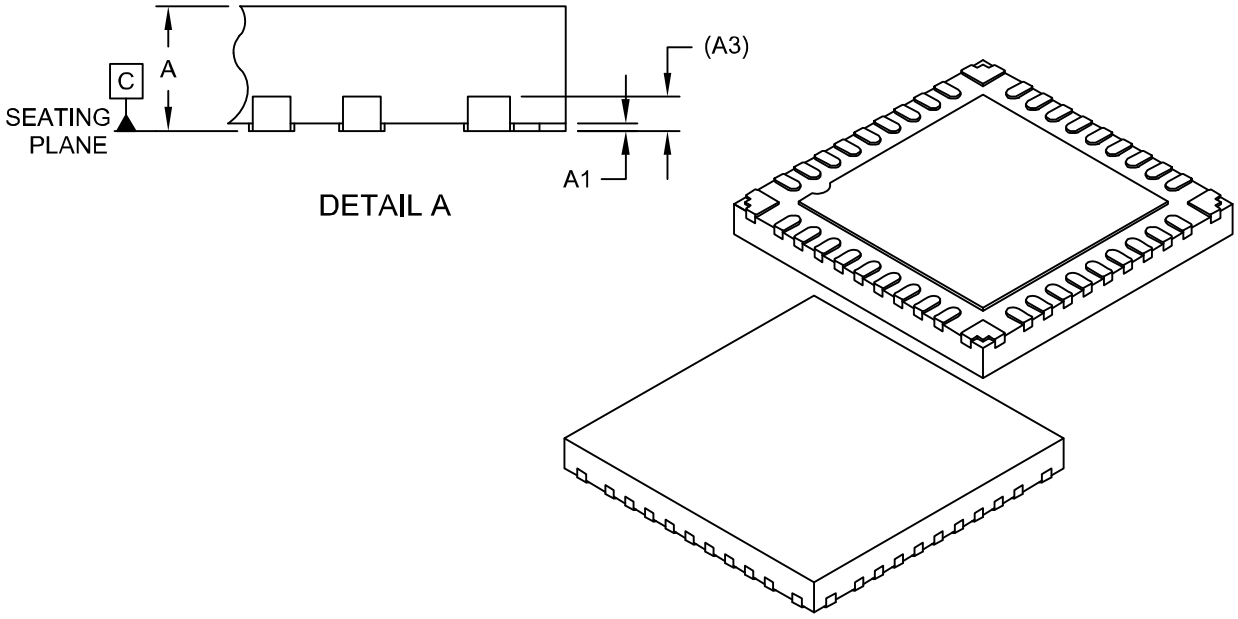
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-436–M5 Rev B Sheet 1 of 2

36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K		0.25 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

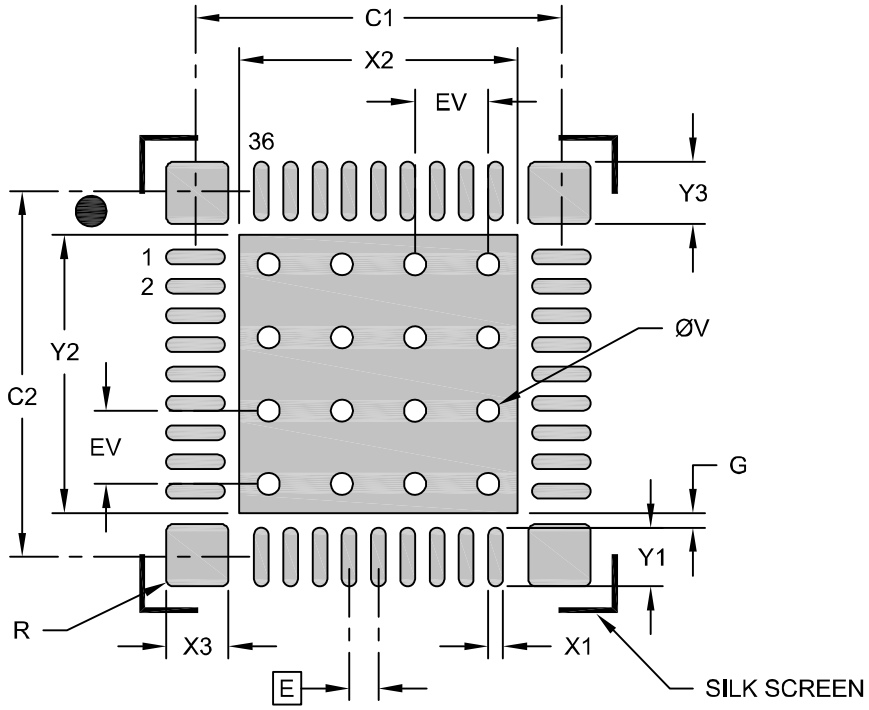
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-436–M5 Rev B Sheet 2 of 2

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36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			3.80
Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X36)	X1			0.20
Contact Pad Length (X36	Y1			0.80
Corner Pad Width (X4)	X3			0.85
Corner Pad Length (X4)	Y3			0.85
Corner Pad Radius	R		0.10	
Contact Pad to Center Pad (X36)	G	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

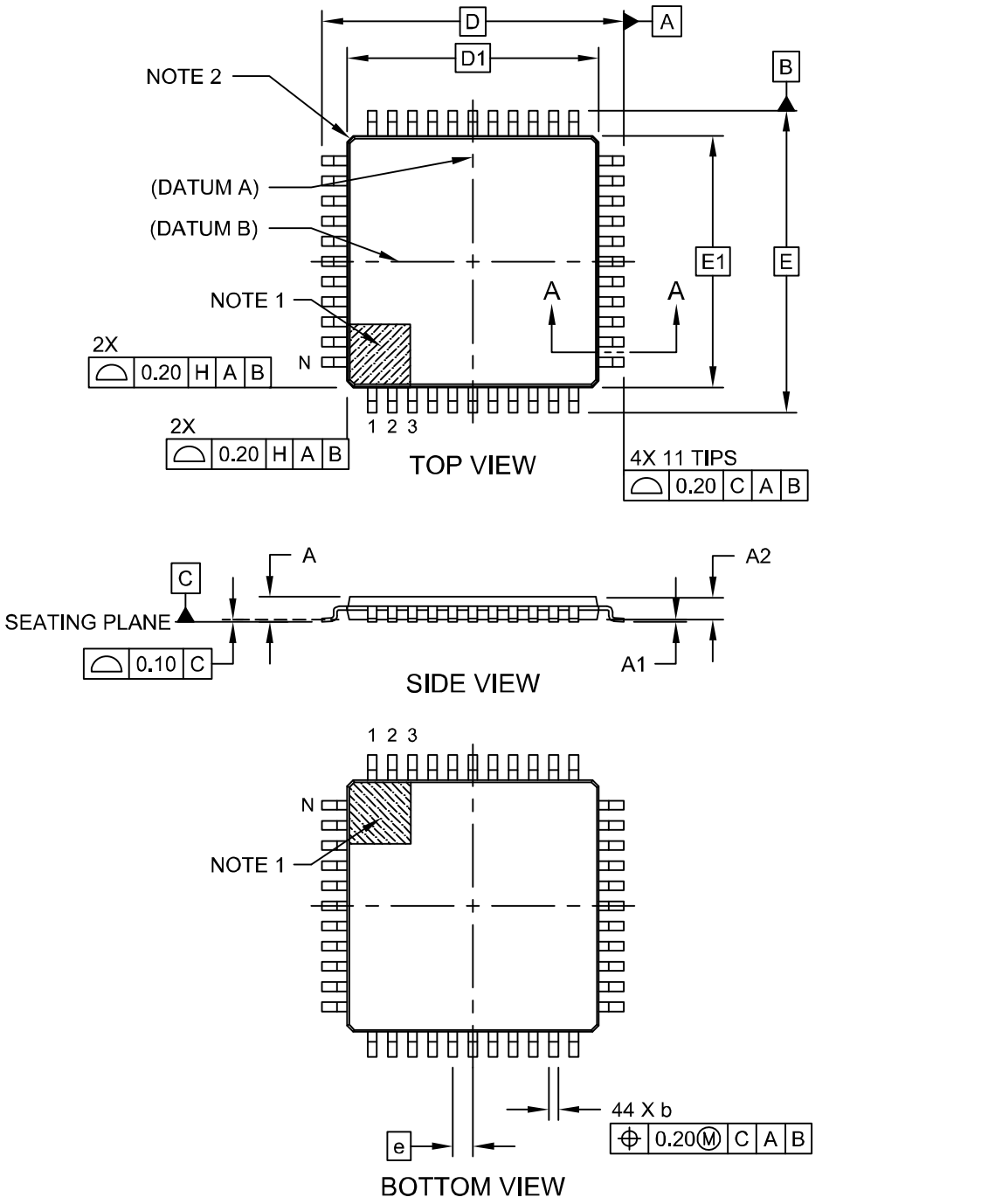
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2436–M5 Rev B

44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

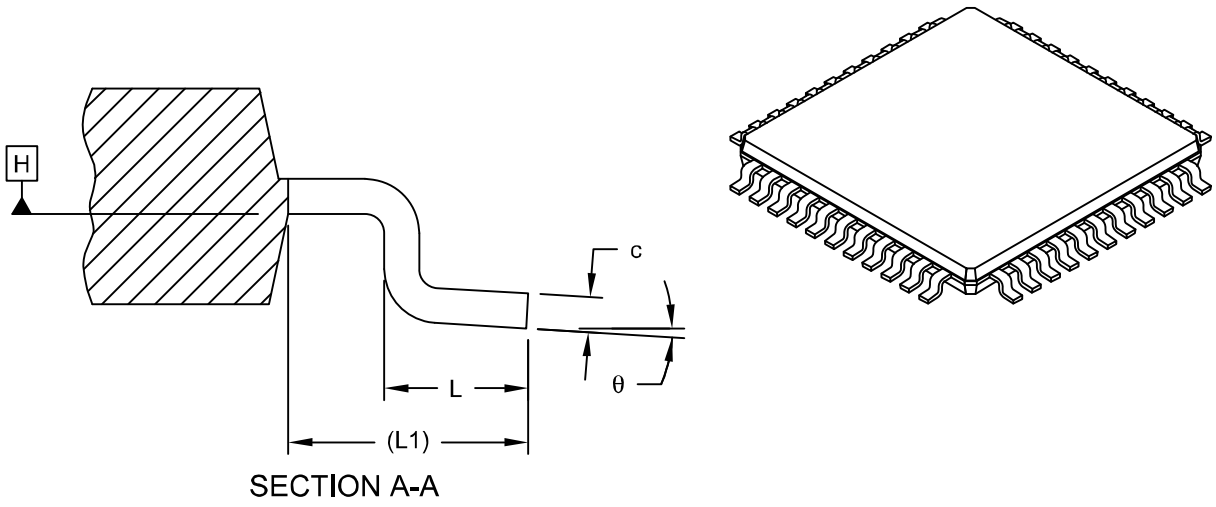


Microchip Technology Drawing C04-076C Sheet 1 of 2

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44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

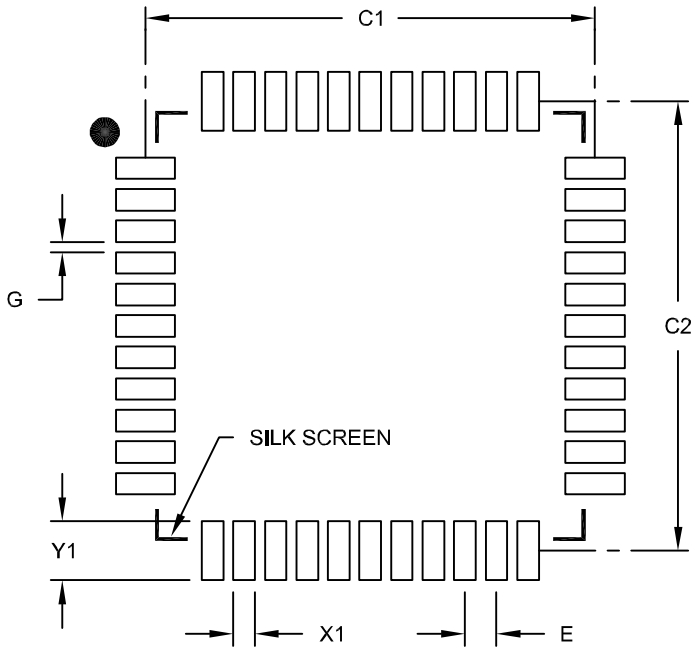
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2

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44-Lead Plastic Thin Quad Flatpack (PT) 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

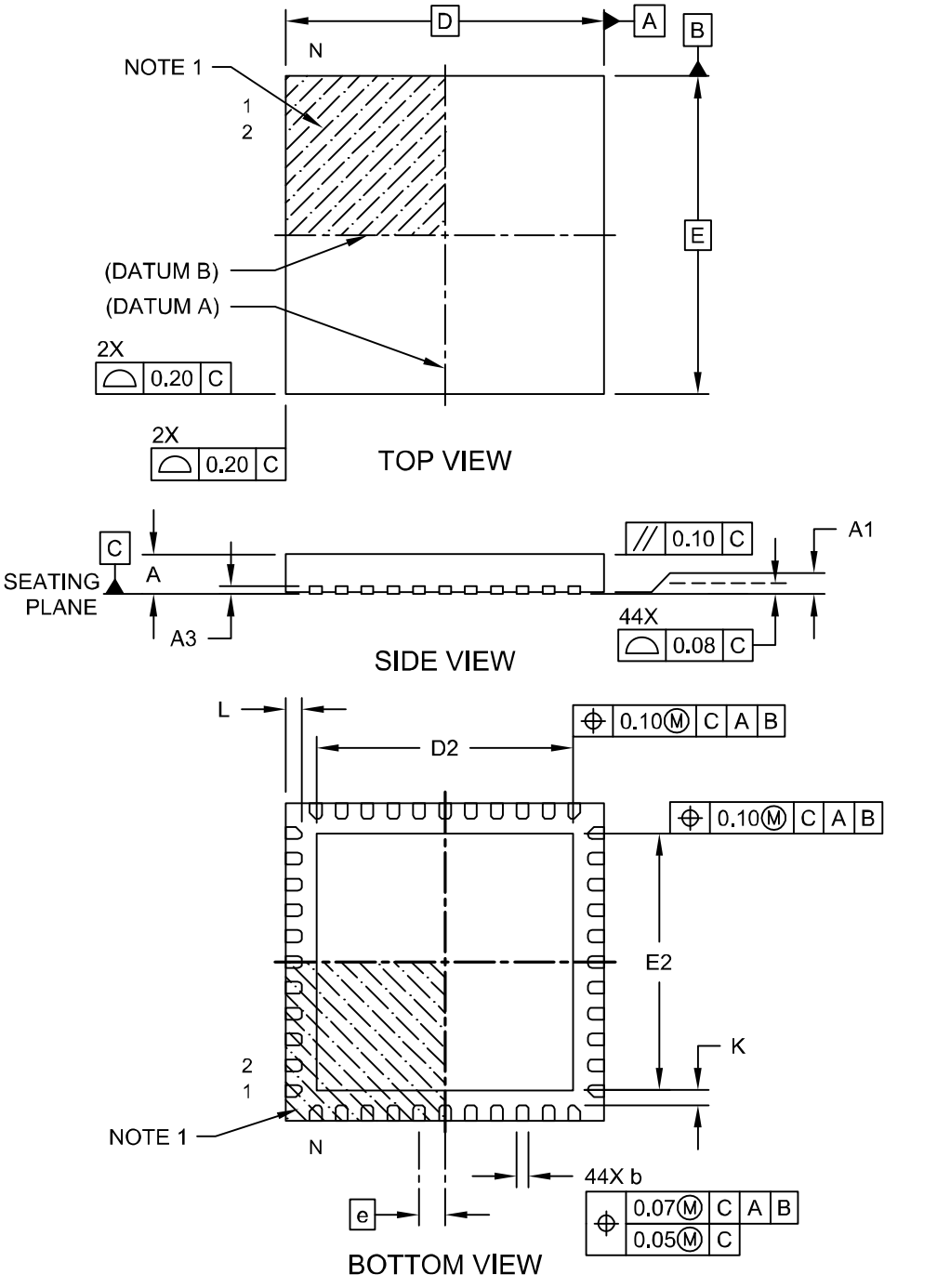
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

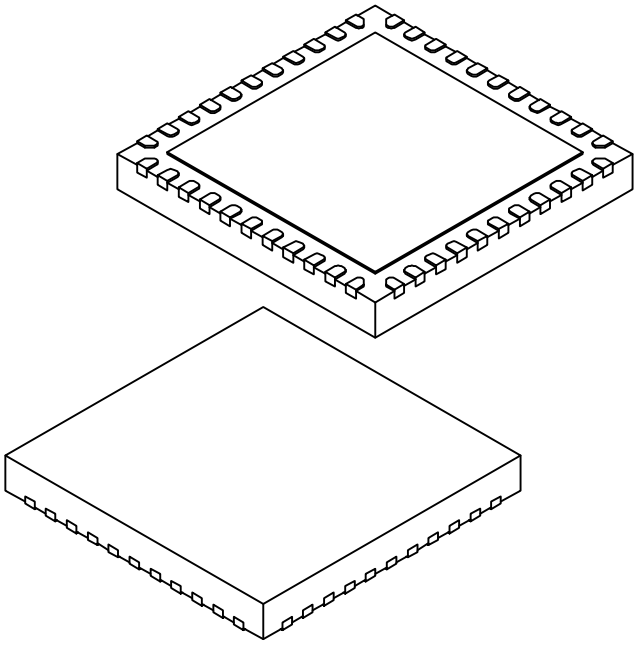
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-103D Sheet 1 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

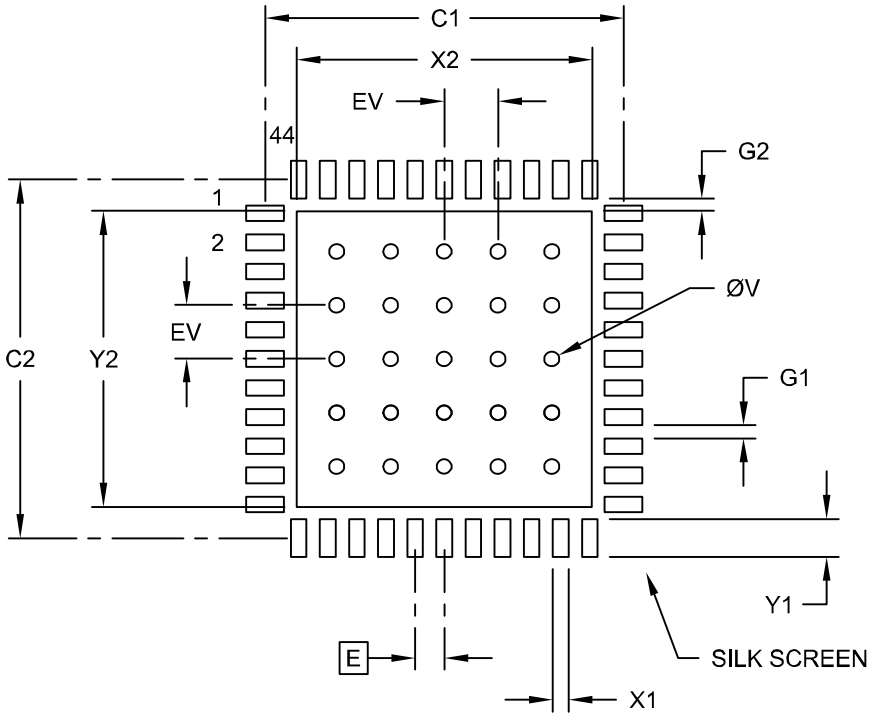
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2

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44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Contact Pad to Contact Pad (X40)	G1	0.30		
Contact Pad to Center Pad (X44)	G2	0.28		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

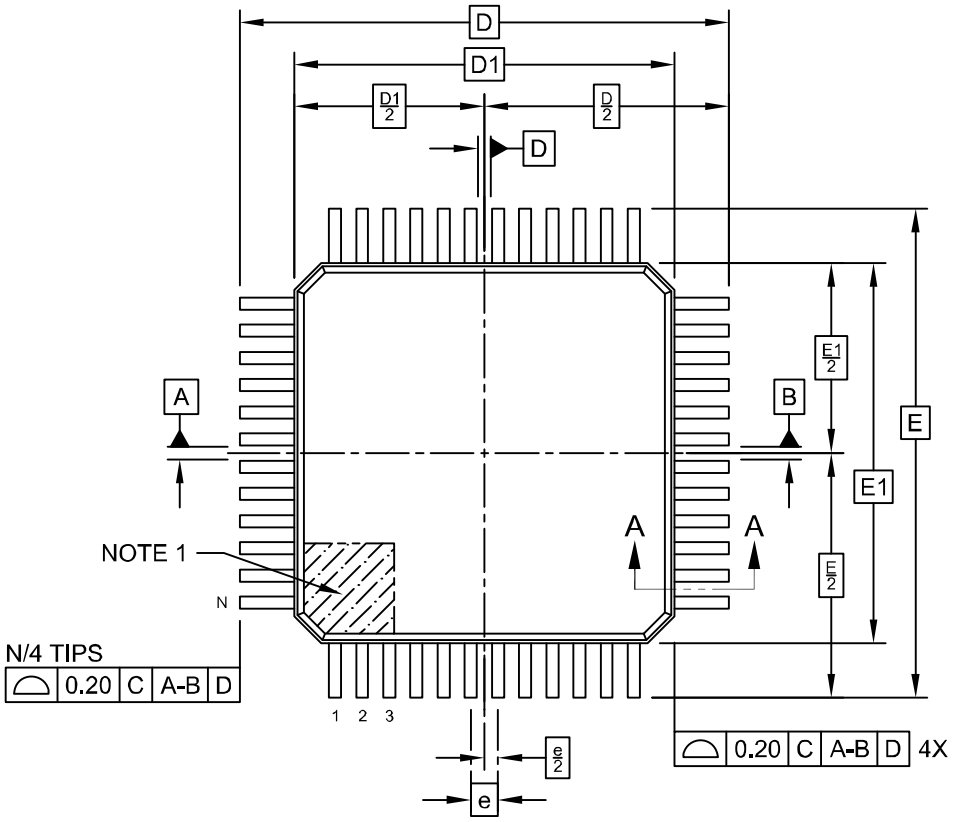
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

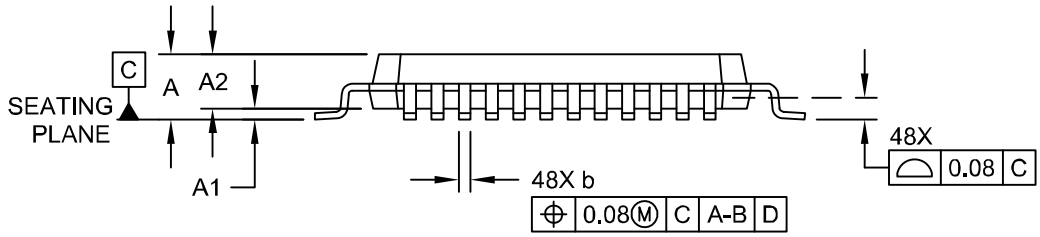
Microchip Technology Drawing No. C04-2103C

48-Lead Plastic Thin Quad Flatpack (P8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



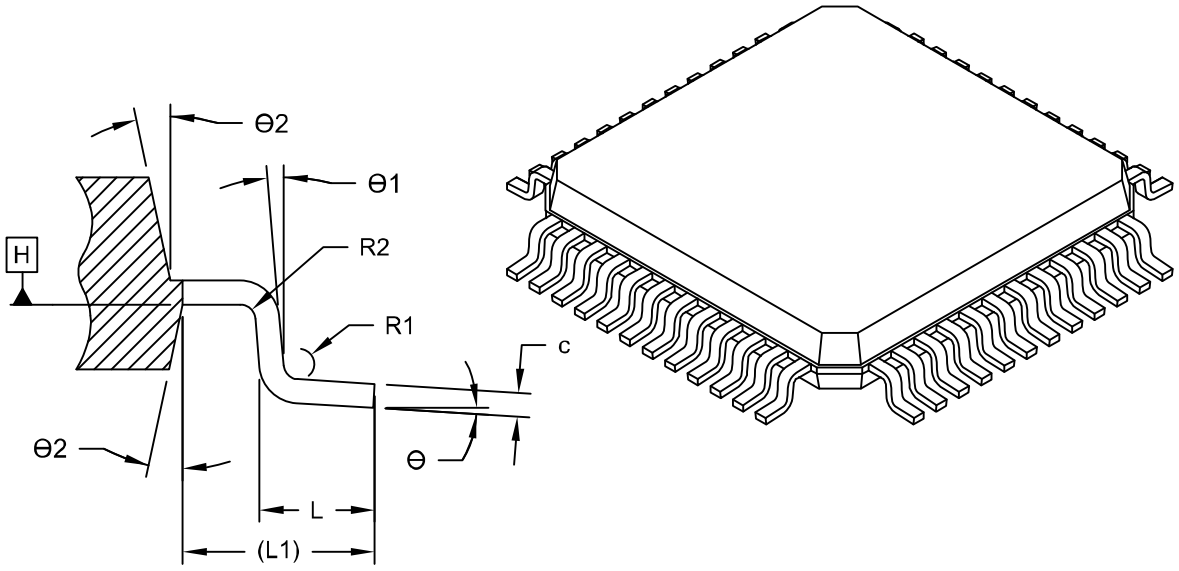
SIDE VIEW

Microchip Technology Drawing C04-300-P8 Rev C Sheet 1 of 2

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48-Lead Plastic Thin Quad Flatpack (P8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		9.00 BSC	
Molded Package Length	D1		7.00 BSC	
Overall Width	E		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Terminal Width	b	0.17	0.22	0.27
Terminal Thickness	c	0.09	-	0.16
Terminal Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Lead Bend Radius	R1	0.08	-	-
Lead Bend Radius	R2	0.08	-	0.20
Foot Angle	Θ	0°	3.5°	7°
Lead Angle	Θ1	0°	-	-
Mold Draft Angle	Θ2	11°	12°	13°

Notes:

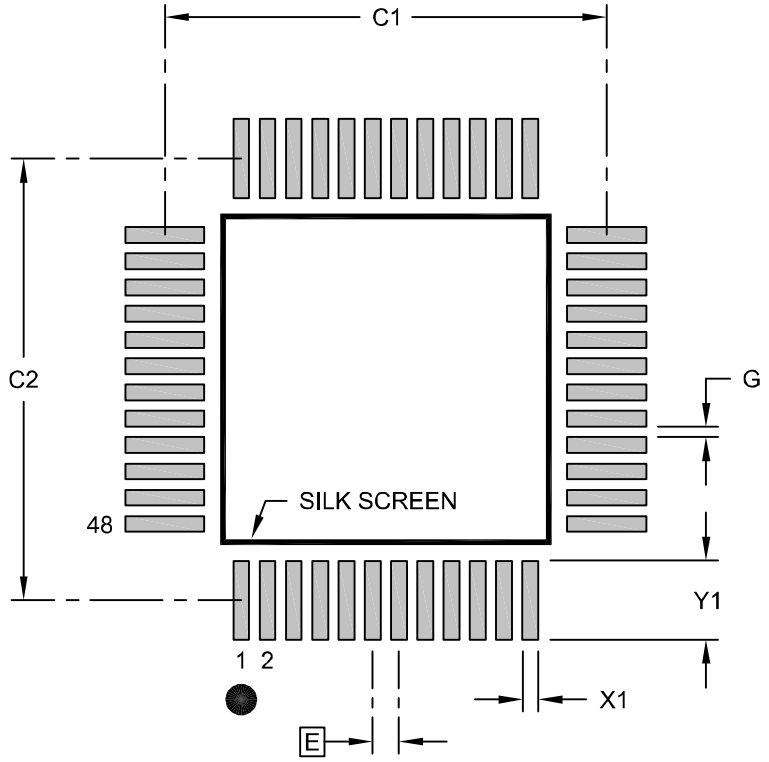
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-300-P8 Rev C Sheet 2 of 2

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48-Lead Plastic Thin Quad Flatpack (P8) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

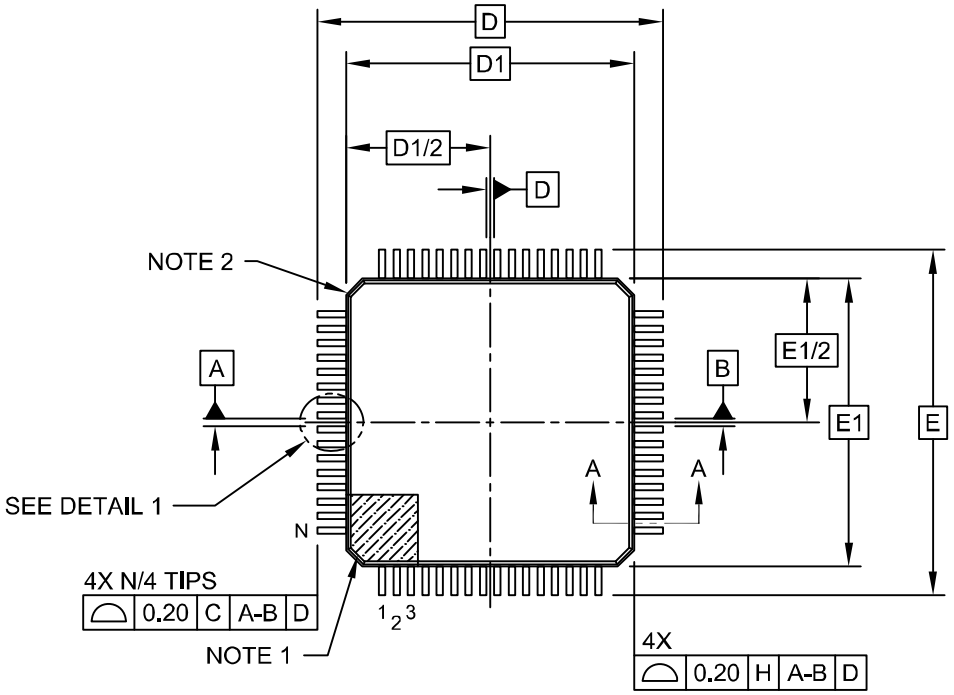
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-P8 Rev B

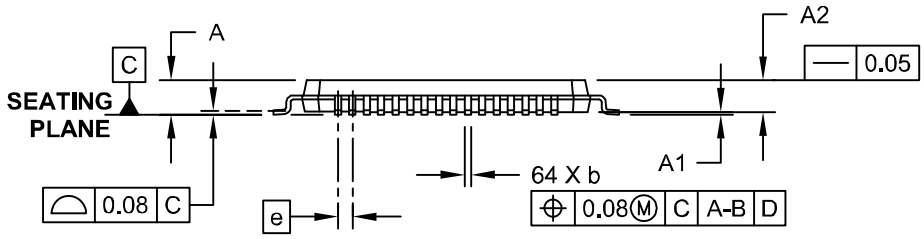
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64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

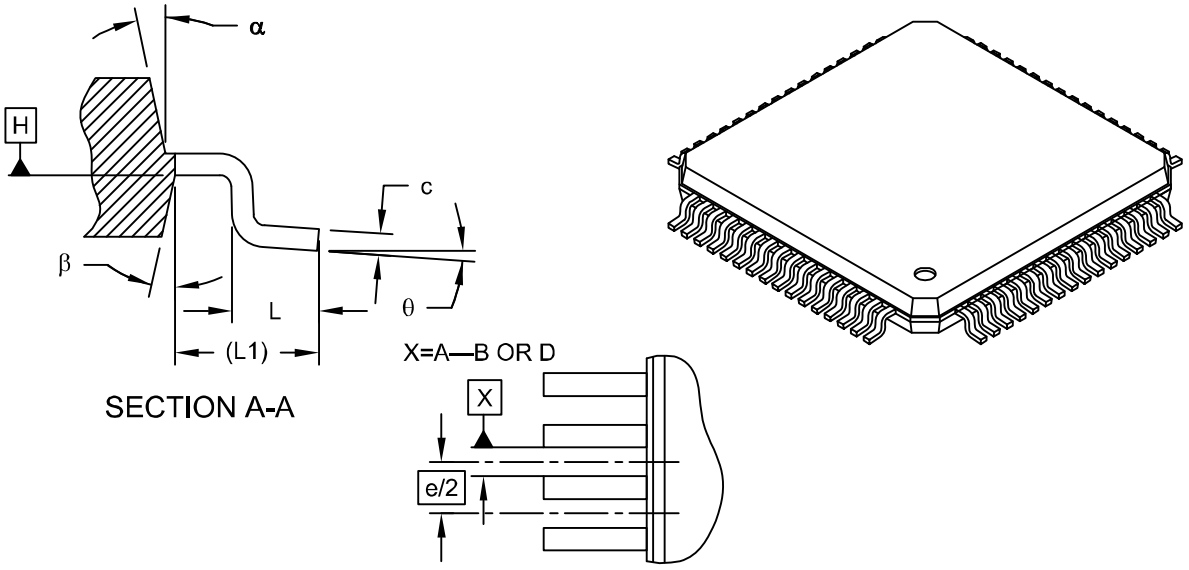


SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

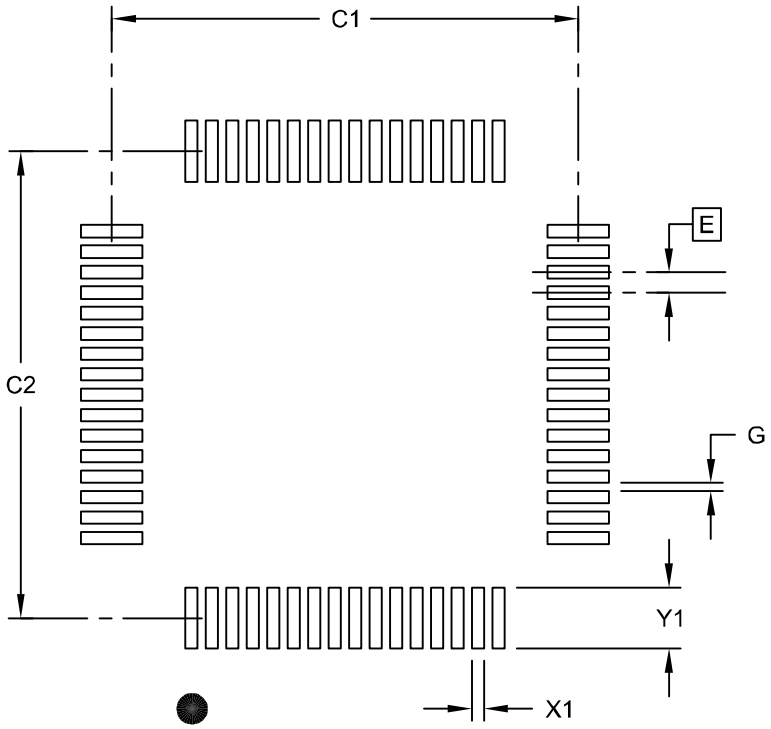
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

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64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

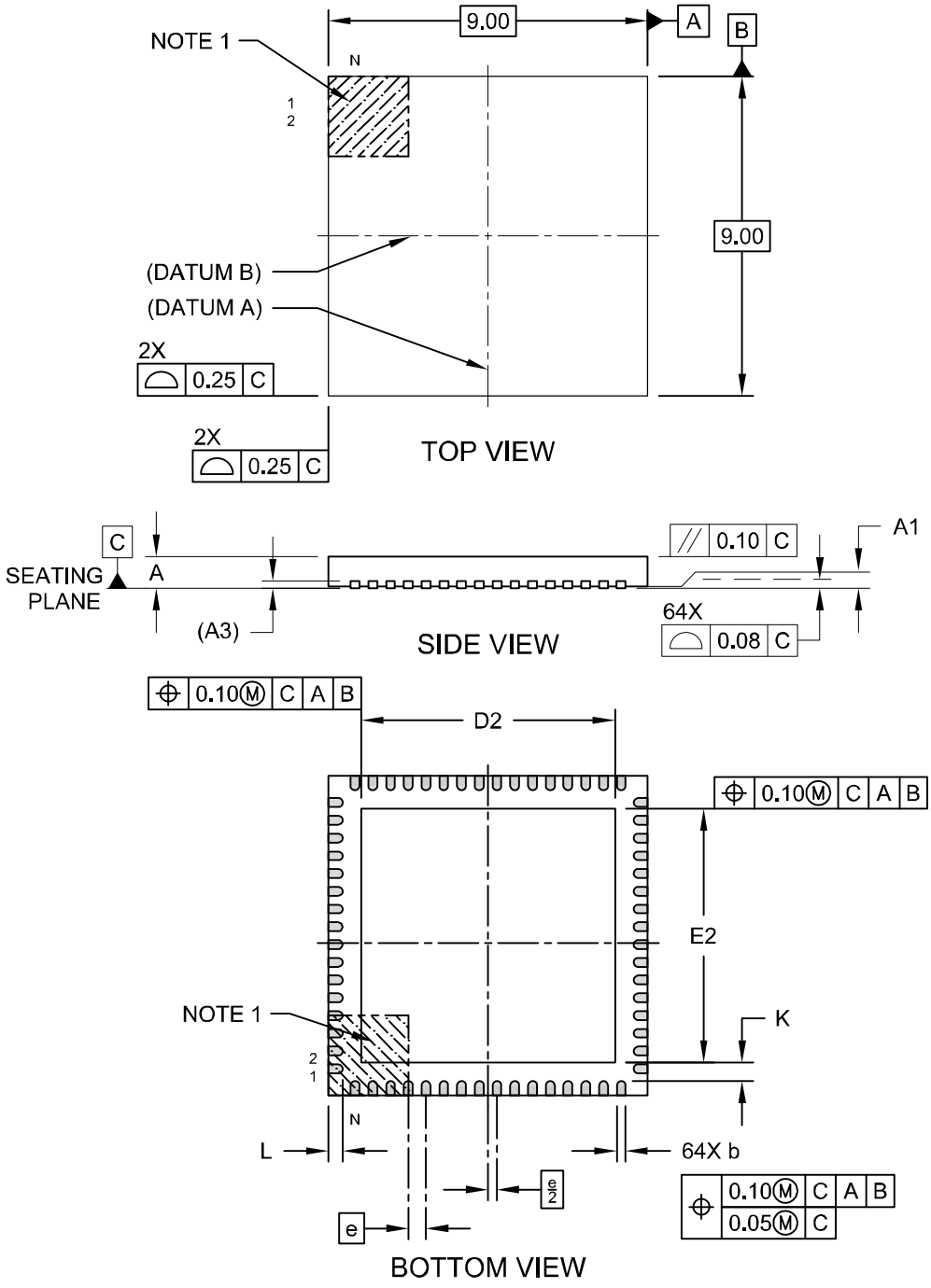
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1

64-Lead Very Thin Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

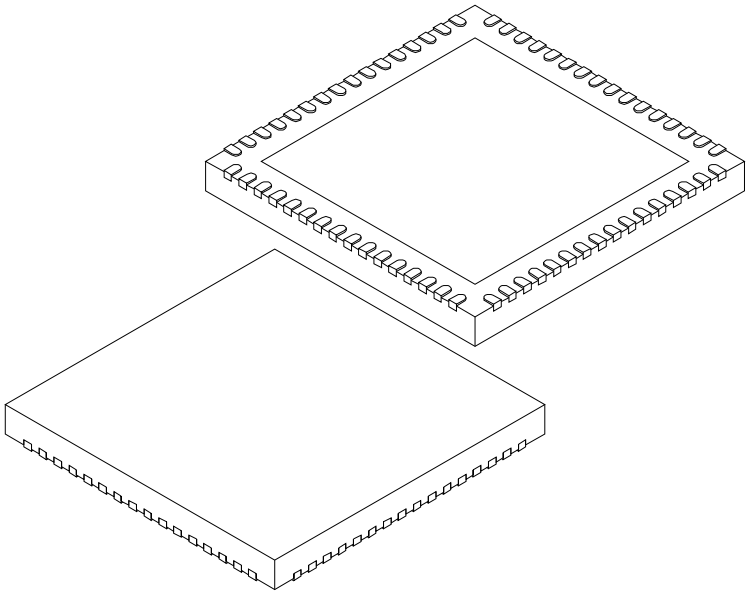


Microchip Technology Drawing C04-149D [MR] Sheet 1 of 2

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64-Lead Very Thin Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.25
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.25
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

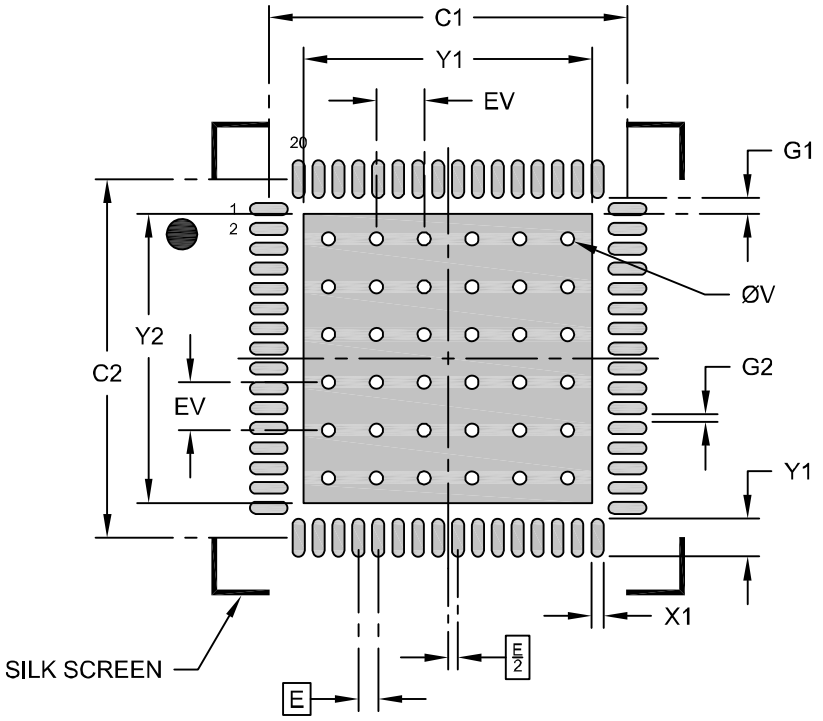
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149D [MR] Sheet 2 of 2

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64-Lead Very Thin Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [VQFN]
With 7.15 x 7.15 Exposed Pad [Also called QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			7.25
Optional Center Pad Length	Y2			7.25
Contact Pad Spacing	C1		9.00	
Contact Pad Spacing	C2		9.00	
Contact Pad Width (X64)	X1			0.30
Contact Pad Length (X64)	Y1			0.95
Contact Pad to Center Pad (X64)	G1	0.40		
Spacing Between Contact Pads (X60)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2149C [MR]

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APPENDIX A: REVISION HISTORY

Revision A (December 2013)

This is the initial version of this document.

Revision B (June 2014)

This revision incorporates the following updates:

- Sections:
  - Added **Section 31.0 "High-Temperature Electrical Characteristics"**
  - Updated the **"Power Management"**section, the **"Input/Output"** section, **Section 3.3 "Data Space Addressing"**, **Section 4.2 "Data Address Space"**, **Section 4.3.2 "Extended X Data Space"**, **Section 4.6.1 "Bit-Reversed Addressing Implementation"**, **Section 7.4.1 "INTCON1 through INTCON4"**, **Section 11.7 "I/O Helpful Tips"**
  - Updated note in **Section 17.0 "High-Speed PWM Module"**, **Section 18.0 "Serial Peripheral Interface (SPI)"**, **Section 27.8 "Code Protection and CodeGuard™ Security"**
  - Updated title of **Section 20.0 "Single-Edge Nibble Transmission (SENT)"**
  - Updated **Section 34.0 "Packaging Information"**. Deleted e3, Pb-free and Industrial (I) temperature range indication throughout the section, and updated the packaging diagrams
  - Updated the **"Product Identification System"** section
- Registers:
  - Updated Register 3-2, Register 7-2, Register 7-6, Register 9-2, Register 11-3, Register 14-1, Register 14-3, Register 14-11, Register 15-1, Register 22-4
- Figures:
  - Added Figure 4-6, Figure 4-8, Figure 4-14, Figure 4-15, Figure 14-1, Figure 16-1, Figure 17-2, Figure 23-1, Figure 24-1
- Tables:
  - Updated Table 1, Table 27-1, Table 27-2, Table 30-6, Table 30-7, Table 30-8, Table 30-9, Table 30-10, Table 30-11, Table 30-12, Table 30-38, Table 30-50, Table 30-53 and added Table 31-11
- Changes to text and formatting were incorporated throughout the document

Revision C (November 2014)

This revision incorporates the following updates:

- Sections:
  - Added note in **Section 5.2 "RTSP Operation"**
  - Updated "**Section 5.4 "Error Correcting Code (ECC)"**
  - Deleted 44-Terminal Very Thin Leadless Array Package (TL) - 6x6x0.9 mm Body With Exposed Pad (VTLA).
- Registers
  - Updated Register 7-6
- Figures:
  - Updated Figure 4-1, Figure 4-3, Figure 4-4
- Tables:
  - Updated Table 27-2, Table 31-13, Table 31-14, Table 31-15
  - Added Table 31-16, Table 31-17

Revision D (April 2015)

This revision incorporates the following updates:

- Sections:
  - Updated the Clock Management, Timers/Output Compare/Input Capture, Communication Interfaces and Input/Output sections at the beginning of the data sheet (Page 1 and Page 2).
  - Updated all pin diagrams at the beginning of the data sheet (Page 5 through Page 12).
  - Added **Section 11.6 "High-Voltage Detect (HVD)"**
  - Updated **Section 13.0 "Timer2/3 and Timer4/5"**
  - Corrects all Buffer heading numbers in **Section 22.4 "CAN Message Buffers"**
- Registers
  - Updated Register 3-2, Register 25-2, Register 26-2
- Figures
  - Updated Figure 26-1, Figure 30-5, Figure 30-32
- Tables
  - Updated Table 1, Table 4-25, Table 30-10, Table 30-22, Table 30-53 and Table 31-8
- Changes to text and formatting were incorporated throughout the document

Revision E (September 2016)

This revision incorporates the following updates:

- Sections:
  - Added new **Section 32.0 "Characteristics for Industrial/Extended Temperature Devices (-40°C to +125°C)"** and **Section 33.0 "Characteristics for High-Temperature Devices (+150°C)"**.
  - Updated the **"Qualification and Class B Support"** section.
  - Updated **Section 27.6 "In-Circuit Serial Programming"**.
  - Updated **Section 34.0 "Packaging Information"** with the addition of the 28-Lead SSOP package information and new packaging diagram revisions.
  - Updated the **"Product Identification System"** section with the addition of the 28-Lead SSOP package.
- Figures:
  - Updated Figure 4-6
- Registers:
  - Updated Register 25-2, Register 25-3, Register 27-1 and Register 27-2
- Tables:
  - Updated Table 30-7, Table 30-9, Table 30-39, Table 30-40, Table 30-41, Table 30-42, Table 30-43, Table 30-44 and Table 30-45

Revision F (March 2018)

This revision incorporates the following updates:

- Sections:
  - **"Pin Diagrams"**
  - **Section 16.0 "Output Compare"**
  - **Section 17.1 "PWM Faults"**
  - **Section 18.0 "Serial Peripheral Interface (SPI)"**
  - **Section 23.0 "Charge Time Measurement Unit (CTMU)"**
  - **Section 31.0 "High-Temperature Electrical Characteristics"**
  - **Section 34.0 "Packaging Information"**
  - **"Product Identification System"**
- Figures:
  - Figure 26-1
- Tables:
  - Table 4-1, Table 4-25, Table 27-2, Table 28-2, Table 30-3, Table 30-8, Table 30-11, Table 31-9
- Registers:
  - Register 23-2, Register 23-3, Register 24-6, Register 24-7, Register 26-2

Revision G (May 2018)

This revision incorporates the following updates:

- Sections:
  - **"Operating Conditions"**
- Tables:
  - Table 30-1

Revision H (May 2019)

This revision incorporates the following updates:

- Sections:
  - Updated **Section 17.1 "PWM Faults"**, **Section 34.2 "Package Details"** and **Section 29.0 "Development Support"**.
- Registers:
  - Updated Register 21-2 and Register 22-10.
- Tables:
  - Updated Table 1, Table 30-3, Table 30-8, Table 30-11, Table 30-22, Table 31-4 and Table 31-9.
- Figures:
  - Updated Figure 26-1.
- Added 48-Pin package marking information.

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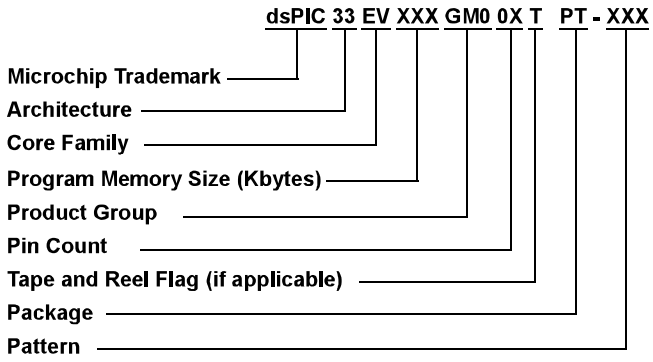
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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Architecture:	33	=	16-Bit Digital Signal Controller
Family:	EV	=	Enhanced Voltage
Product Group:	GM	=	General Purpose plus Motor Control Family
Pin Count:	02	=	28-Pin
	03	=	36-Pin
	04	=	44-Pin or 48-Pin
	06	=	64-Pin
Temperature Range:	I	=	-40°C to +85°C (Industrial)
	E	=	-40°C to +125°C (Extended)
	H	=	-40°C to +150°C (High)
Package:	MM	=	Plastic Quad Flat, No Lead Package – (28-pin) 6x6x0.9 mm body (QFN-S)
	SO	=	Plastic Small Outline – (28-pin) 7.50 mm body (SOIC)
	SS	=	Plastic Shrink Small Outline – (28-pin) 5.30 mm body (SSOP)
	SP	=	Skinny Plastic Dual In-Line – (28-pin) 300 mil body (SPDIP)
	M5	=	Ultra Thin Plastic Quad Flat, No Lead Package - (36-pin) 5x5 mm body (UQFN)
	ML	=	Plastic Quad Flat, No Lead Package – (44-pin) 8x8 mm body (QFN)
	PT	=	Plastic Thin Quad Flatpack – (44-pin) 10x10x1 mm body (TQFP)
	P8	=	Plastic Thin Quad Flatpack – (48-pin) 7x7x1 mm body (TQFP)
	PT	=	Plastic Thin Quad Flatpack – (64-pin) 10x10x1 mm body (TQFP)
	MR	=	Plastic Quad Flat, No Lead Package – (64-pin) 9x9x0.9 mm body (QFN)

Example:

dsPIC33EV256GM006-I/PT:
dsPIC33, Enhanced Voltage,
256-Kbyte Program Memory, 64-Pin,
Industrial Temperature, TQFP Package.

NOTES:

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ISBN: 978-1-5224-4488-6

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