Product Change Notification - SYST-31RUBG366

Date:

01 Feb 2019

Product Category:

Driver / Interface ICs

Affected CPNs:

Notification subject:

Data Sheet - HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs

Notification text:

SYST-31RUBG366

Microchip has released a new DeviceDoc for the HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs of devices. If you are using one of these devices please read the document located at HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs.

Notification Status: Final

Description of Change:

1. Converted Supertex Doc# DSFP-HV7620 to Microchip DS20005779A
2. Removed “HVCMOS® Technology” from the Features section
3. Changed the package marking format
4. Made minor text changes throughout the document

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 01 Feb 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs

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HV7620

40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs

Features

- 5V Logic and 12V Supply Rail
- Up to +200V Output Voltage
- Low-power Level Shifting
- 50 mA Minimum Source and Sink Currents
- 40 MHz Equivalent Data Rate
- Latched Data Outputs
- Forward and Reverse Shifting Options (DIR Pin)
- Chip Select
- Polarity Function

Applications

- Display Driver
- Print Head Driver
- MEMS Applications

General Description

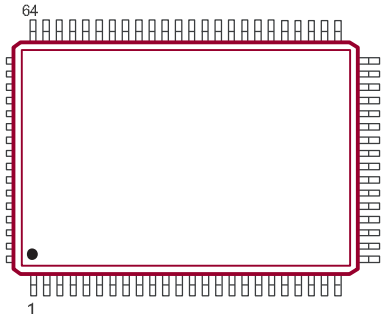
The HV7620 is a low-voltage serial-to-high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has four parallel 8-bit shift registers permitting data rates four times the speed of one. The data is clocked in simultaneously on all four data inputs with a single clock. Data is shifted in on a low-to-high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to V_{DD1} and counterclockwise (CCW) shifting when connected to LVGND. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable) input. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ input is high. Data is stored in the latches when $\overline{LE}$ is low. The current source on the logic inputs provides active pull up when the input pins are open.

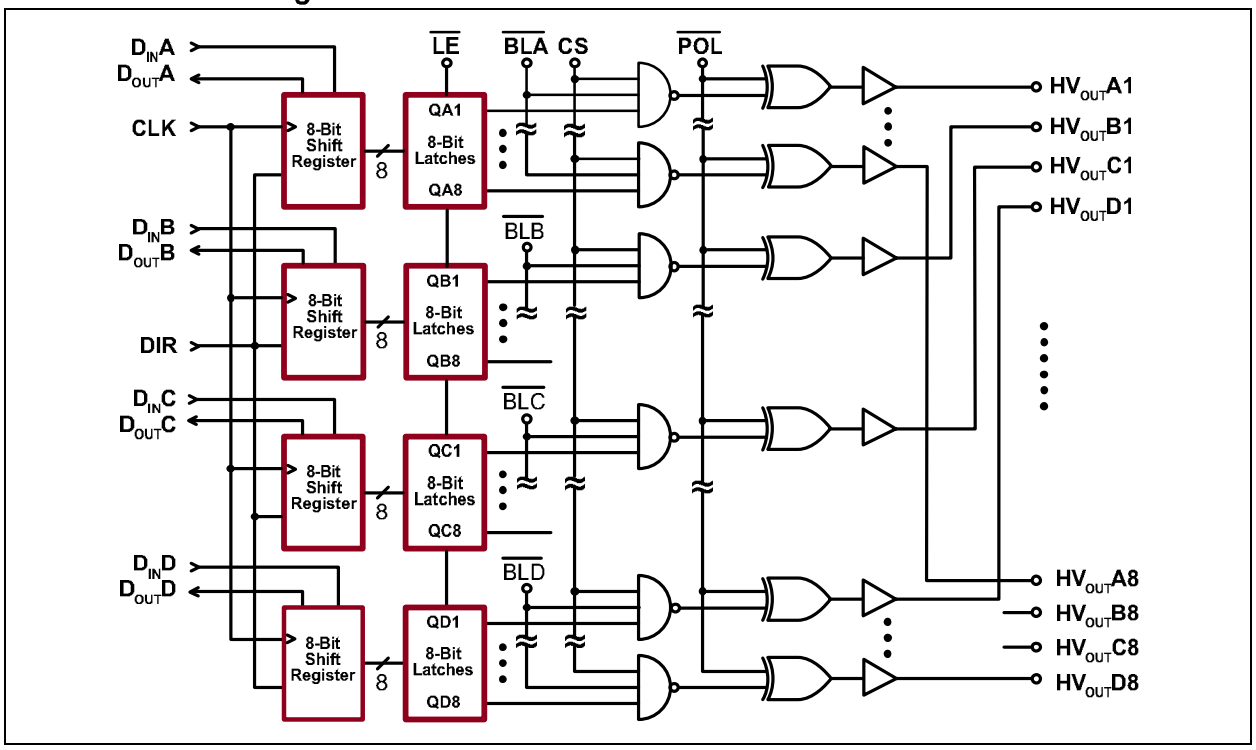
Package Type

64-lead PQFP
(Top view)



See Table 2-1 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD1} ..... –0.5V to +14V
Supply Voltage, V_{DD2} ..... –0.5V to +14V
Supply Voltage, V_{PP} ..... –0.5V to +225V
Logic Input Levels ..... –2V to V_{DD1} +2V
Maximum Junction Temperature, $T_{J(MAX)}$ ..... +125°C
Storage Temperature, T_S ..... –65°C to +150°C
Continuous Total Power Dissipation:
64-lead PQFP (**Note 1**) ..... 1200 mW
ESD Rating (**Note 2**) ..... ESD Sensitive

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: For operations above 25°C ambient, derate linearly to maximum operating temperature at 20 mW/°C.
2: Device is ESD sensitive. Handling precautions are recommended.

RECOMMENDED OPERATING CONDITIONS

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage		V_{DD1}	4.5	—	V_{DD2}	V	
12V Supply Voltage		V_{DD2}	10.8	—	13.2	V	
High-Voltage Supply Voltage		V_{PP}	50	—	200	V	
High-Level Input Voltage		V_{IH}	V_{DD1} –0.5V	—	V_{DD1}	V	
Low-Level Input Voltage		V_{IL}	0	—	0.5	V	
Clock Frequency	V_{DD1} = 5V	f_{CLK}	—	—	10	MHz	
	V_{DD1} = 12V		—	—	5	MHz	
Operating Junction Temperature Range		T_A	–40	—	+85	°C	
Allowable Pulsed Current through Output Diodes		I_{OD}	—	—	500	mA	**Note 1**
Allowable Pulsed V_{PP} or HVGND Current		$I_{GND(VPP)}$	—	—	16	A	**Note 1**
Slew Rate of V_{PP}		$V_{PP(SLEW)}$	—	—	340	V/µs	

Note 1: Current pulse width = 500 ns; duty cycle = 5%

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating supply voltages and temperature, unless otherwise noted, V_{DD1} = 5V, V_{DD2} = 12V, V_{PP} = 200V and T_J = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD1} Supply Current		I_{DD1}	—	—	5	mA	f_{CLK} = 10 MHz
V_{DD2} Supply Current		I_{DD2}	—	—	22	mA	V_{DD2} = 13.2V, f_{CLK} = 10 MHz
High Voltage Supply Current		I_{PP}	—	—	2	mA	All outputs high or low
Quiescent V_{DD1} Supply Current		I_{DD1Q}	—	—	100	µA	All input = V_{DD1}
Quiescent V_{DD2} Supply Current		I_{DD2Q}	—	—	100	µA	All input = V_{DD1}
High-Level Output	HV_{OUT}	V_{OH}	185	—	—	V	I_O = –50 mA
	Data OUT		V_{DD} –1	—	—	V	I_O = –100 µA
Low-Level Output	HV_{OUT}	V_{OL}	—	—	20	V	I_O = +50 mA
	Data OUT		—	—	1	V	I_O = +100 µA
High-Level Logic Input Current		I_{IH}	—	—	1	µA	V_{IN} = V_{DD1}
Low-Level Logic Input Current		I_{IL}	—	—	–10	µA	V_{IN} = 0V
HVGND to LVGND Voltage Difference		V_{GG}	–1	—	1	V	

AC ELECTRICAL CHARACTERISTICS

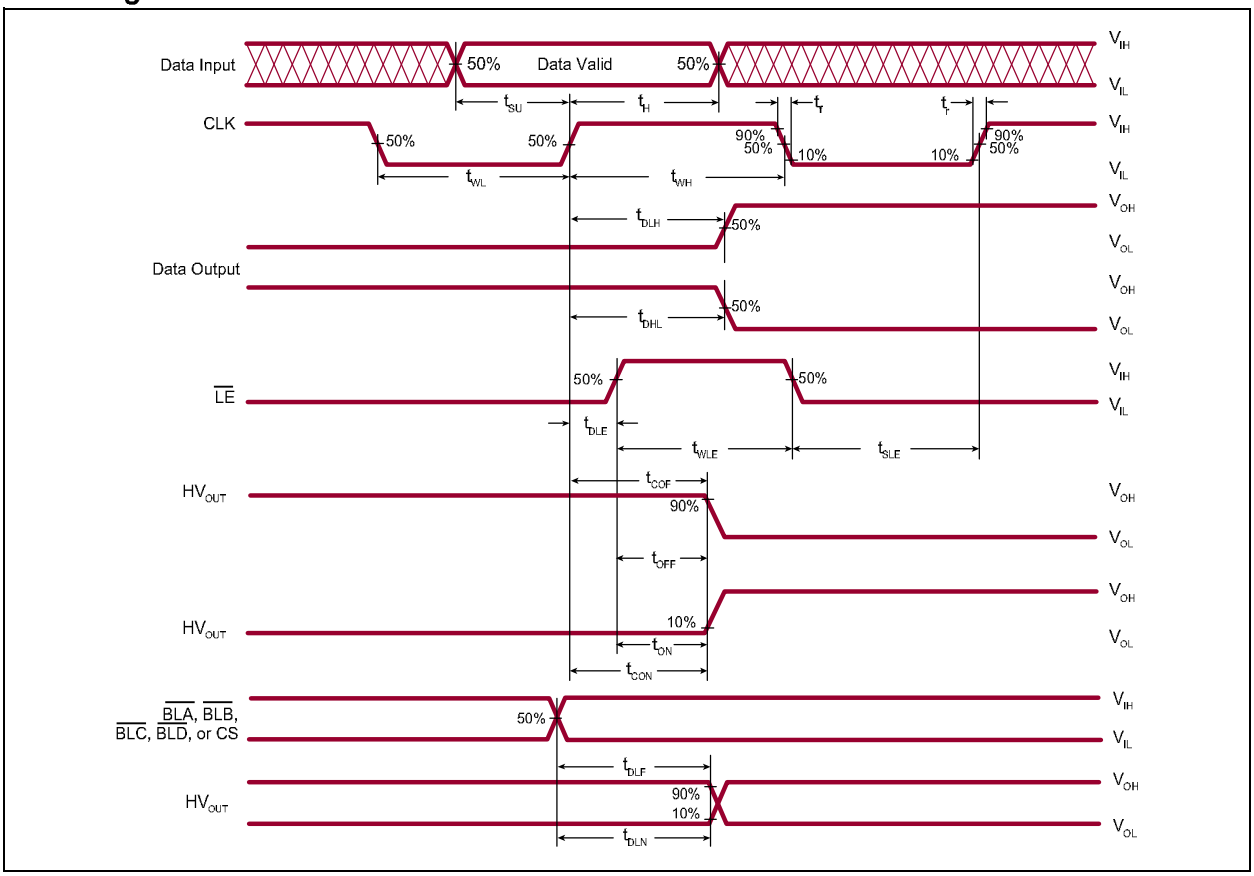
Electrical Specifications: Logic signal inputs and data inputs have t_r, $t_f \leq 5$ ns. V_{DD1} = 5V or 12V, V_{DD2} = 12V, V_{PP} = 200V and T_J = 25°C.

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	V_{DD1} = 5V	f_{CLK}	—	—	10	MHz	Per register, C_L = 15 pF
	V_{DD1} = 12V		—	—	5	MHz	
Clock Width High or Low		t_{WL}, t_{WH}	40	—	—	ns	
Data Set-Up Time Before Clock Rises		t_{SU}	20	—	—	ns	
Data Hold Time after Clock Rises		t_H	20	—	—	ns	
Time from Latch Enable to HV_{OUT}		t_{ON}, t_{OFF}	—	—	275	ns	C_L = 15 pF
$\overline{LE}$ Pulse Width		t_{WLE}	25	—	—	ns	
Delay Time Clock to $\overline{LE}$ Low to High		t_{DLE}	50	—	—	ns	
$\overline{LE}$ Set-Up Time before Clock Rises		t_{SLE}	20	—	—	ns	
$\overline{BL}$ or CS Low to High to HV_{OUT}		t_{DLF}, t_{DLN}	—	—	250	ns	
Clock to HV_{OUT}		t_{COF}, t_{CON}	—	—	275	ns	
Delay Time Clock to Data Low to High	V_{DD1} = 5V	t_{DLH}	—	—	250	ns	C_L = 15 pF
	V_{DD1} = 12V		—	—	100	ns	
Delay Time Clock to Data High to Low	V_{DD1} = 5V	t_{DHL}	—	—	250	ns	C_L = 15 pF
	V_{DD1} = 12V		—	—	100	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	T_J	–40	—	+85	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
64-lead PQFP	θ_{JA}	—	41	—	°C/W	

Switching Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HV7620 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: 64-LEAD PQFP PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVGND	High-voltage supply ground
2	VPP	High-voltage power supply
3	$HV_{OUT}D8$	High-voltage output
4	$HV_{OUT}C8$	High-voltage output
5	$HV_{OUT}B8$	High-voltage output
6	$HV_{OUT}A8$	High-voltage output
7	$HV_{OUT}D7$	High-voltage output
8	$HV_{OUT}C7$	High-voltage output
9	$HV_{OUT}B7$	High-voltage output
10	$HV_{OUT}A7$	High-voltage output
11	$HV_{OUT}D6$	High-voltage output
12	$HV_{OUT}C6$	High-voltage output
13	$HV_{OUT}B6$	High-voltage output
14	$HV_{OUT}A6$	High-voltage output
15	$HV_{OUT}D5$	High-voltage output
16	$HV_{OUT}C5$	High-voltage output
17	$HV_{OUT}B5$	High-voltage output
18	$HV_{OUT}A5$	High-voltage output
19	V_{PP}	High-voltage power supply
20	HVGND	High-voltage supply ground
21	HVGND	High-voltage supply ground
22	VDD2	12V power supply
23	$\overline{BLC}$	Blanking pins
24	$\overline{BLD}$	Blanking pins
25	$\overline{LE}$	Latch enable pin
26	$D_{OUT}D$	Data output pin
27	$D_{IN}D$	Data input pin
28	$D_{IN}C$	Data input pin
29	$D_{OUT}C$	Data output pin
30	$\overline{POL}$	Polarity pin
31	LVGND	Low-voltage supply ground
32	DIR	Direction pin
33	CS	Chip select pin
34	$D_{OUT}B$	Data output pin
35	$D_{IN}B$	Data input pin
36	$D_{IN}A$	Data input pin

TABLE 2-1: 64-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
37	$D_{OUT}A$	Data output pin
38	CLK	Clock pin
39	$\overline{BLA}$	Blanking pins
40	$\overline{BLB}$	Blanking pins
41	VDD1	Logic power supply
42	LVGND	Low-voltage supply ground
43	N/C	No internal connection
44	HVGND	High-voltage supply ground
45	HVGND	High-voltage supply ground
46	VPP	High-voltage power supply
47	$HV_{OUT}D4$	High-voltage output
48	$HV_{OUT}C4$	High-voltage output
49	$HV_{OUT}B4$	High-voltage output
50	$HV_{OUT}A4$	High-voltage output
51	$HV_{OUT}D3$	High-voltage output
52	$HV_{OUT}C3$	High-voltage output
53	$HV_{OUT}B3$	High-voltage output
54	$HV_{OUT}A3$	High-voltage output
55	$HV_{OUT}D2$	High-voltage output
56	$HV_{OUT}C2$	High-voltage output
57	$HV_{OUT}B2$	High-voltage output
58	$HV_{OUT}A2$	High-voltage output
59	$HV_{OUT}D1$	High-voltage output
60	$HV_{OUT}C1$	High-voltage output
61	$HV_{OUT}B1$	High-voltage output
62	$HV_{OUT}A1$	High-voltage output
63	VPP	High-voltage power supply
64	HVGND	High-voltage supply ground

3.0 FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV7620.

TABLE 3-1: POWER-UP AND POWER-DOWN SEQUENCE

Power-Up		Power-Down	
Step	**Description**	**Step**	**Description**
1	GND (HV, LV)	1	Logic Input Signals
2	V_{DD1}	2	V_{PP}
3	V_{DD2}	3	V_{DD2}
4	V_{PP}	4	V_{DD1}
5	Logic Input Signals	5	GND (HV, LV)

TABLE 3-2: TRUTH FUNCTION TABLE [1]

Function	Inputs													HV_{OUT}			
	$D_{IN}A$	$D_{IN}B$	$D_{IN}C$	$D_{IN}D$	CLK	$\overline{LE}$	DIR	$\overline{BLA}$	$\overline{BLB}$	$\overline{BLC}$	$\overline{BLD}$	CS	$\overline{POL}$	A	B	C	D
All O/P High	X	X	X	X	X	X	X	X	X	X	X	L	L	H	H	H	H
All O/P Low	X	X	X	X	X	X	X	X	X	X	X	L	H	L	L	L	L
"A" (Note 3) Outputs Low	X	X	X	X	X	X	X	L	X	X	X	X	H	L	**Note 2**	**Note 2**	**Note 2**
Normal Polarity	X	X	X	X	X	X	X	H	H	H	H	H	H	No Inversion			
Outputs Inverted	X	X	X	X	X	X	X	H	H	H	H	H	L	Inversion			
Transparent Mode	H	L	L	L	↑	H	X	H	H	H	H	H	H	H	L	L	L
Data Stored	X	X	X	X	X	L	X	H	H	H	H	H	H	Stored data			
Shift CW[A]	X	X	X	X	↑	H	H	H	H	H	H	H	X	A_N → A_{N+1}	B_N → B_{N+1}	C_N → C_{N+1}	D_N → D_{N+1}
Shift CCW[B]	X	X	X	X	↑	H	L	H	H	H	H	H	X	A_N → A_{N-1}	B_N → B_{N-1}	C_N → C_{N-1}	D_N → D_{N-1}

Note 1: H = High logic level
L = Low logic level
X = Irrelevant
↑ = Low-to-high transition

2: Dependent on previous stage's state before the last CLK ↑ or last $\overline{LE}$ high

3: $\overline{BLB}$, $\overline{BLC}$ and $\overline{BLD}$ will have a similar effect on their respective output.

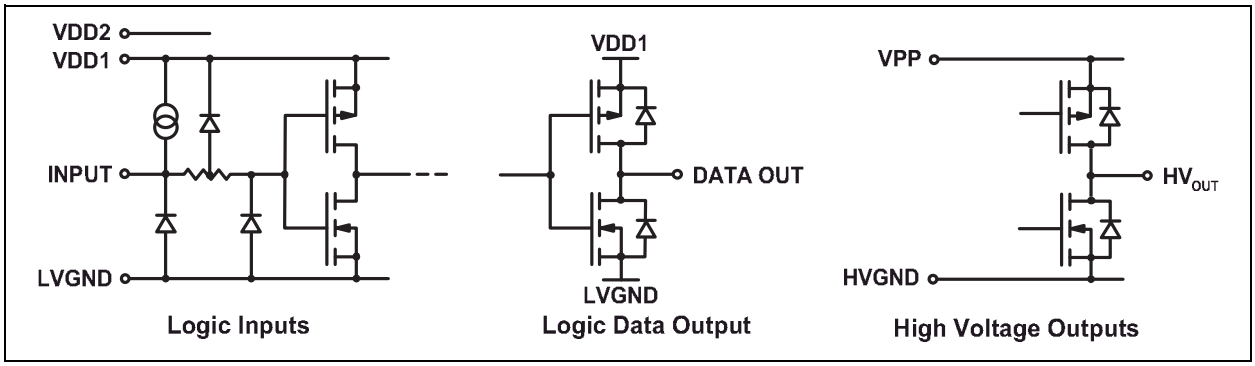


FIGURE 3-1: *Input and Output Equivalent Circuits.*

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

64-lead PQFP

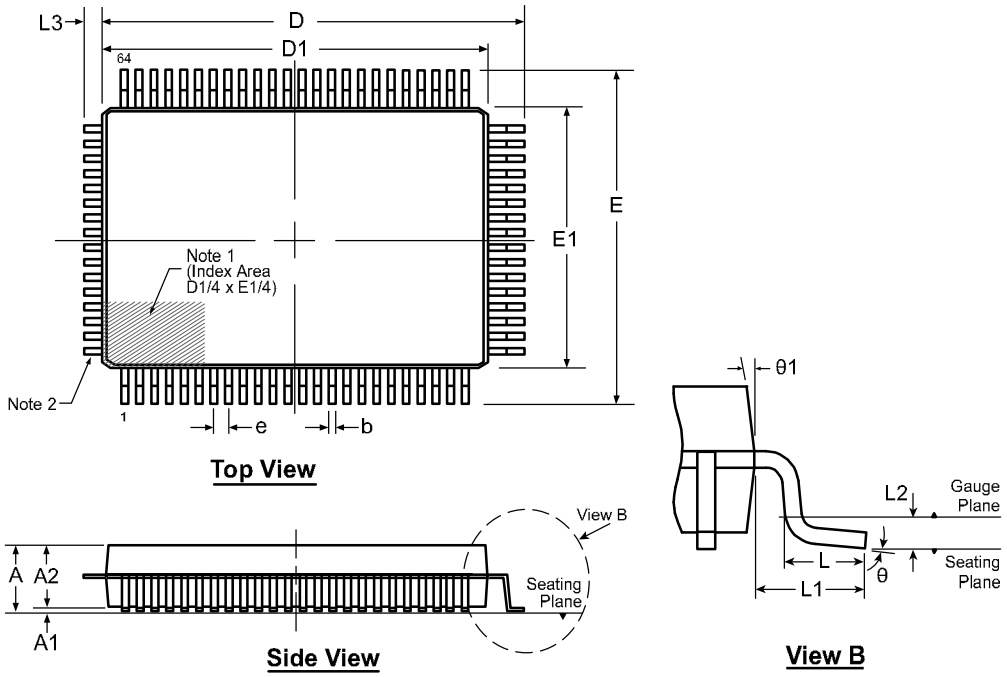
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *The leads on this side are trimmed.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	L3	θ	θ1
Dimension (mm)	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80	0.80 BSC	0.73	1.95 REF	0.25 BSC	0.55 REF	0°	5°
	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00		0.88				3.5°	-
	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7°	16°

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (January 2019)

- Converted Supertex Doc# DSFP-HV7620 to Microchip DS20005779A
- Removed “HVCMOS® Technology” from the Features section
- Changed the package marking format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV7620	=	40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs
Package:	PG	=	64-lead PQFP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	66/Tray for a PG Package

Example:

a) HV7620PG-G: 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs, 64-lead PQFP, 66/Tray

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SYST-31RUBG366 - Data Sheet - HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull

Affected Catalog Part Numbers(CPN)

HV7620ND
HV7620PG-G