

# Product Change Notification - SYST-31RUBG366

### Date:

01 Feb 2019

**Product Category:** 

Driver / Interface ICs

#### Affected CPNs:

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### Notification subject:

Data Sheet - HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs

### Notification text:

SYST-31RUBG366 Microchip has released a new DeviceDoc for the HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs of devices. If you are using one of these devices please read the document located at <u>HV7620 40 MHz 32-Channel Serial-to-Parallel</u> <u>Converter with Push-Pull Outputs</u>.

## Notification Status: Final

# **Description of Change:**

- 1. Converted Supertex Doc# DSFP-HV7620 to Microchip DS20005779A
- 2. Removed "HVCMOS® Technology" from the Features section
- 3. Changed the package marking format
- 4. Made minor text changes throughout the document

# Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

# Date Document Changes Effective: 01 Feb 2019

**NOTE:** Please be advised that this is a change to the document only the product has not been changed.

# Markings to Distinguish Revised from Unrevised Devices: N/A Attachment(s):

HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs

Please contact your local <u>Microchip sales office</u> with questions or concerns regarding this notification.

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# HV7620

# 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs

#### Features

- 5V Logic and 12V Supply Rail
- Up to +200V Output Voltage
- · Low-power Level Shifting
- 50 mA Minimum Source and Sink Currents
- 40 MHz Equivalent Data Rate
- Latched Data Outputs
- Forward and Reverse Shifting Options (DIR Pin)
- Chip Select
- Polarity Function

# Applications

- · Display Driver
- Print Head Driver
- MEMS Applications

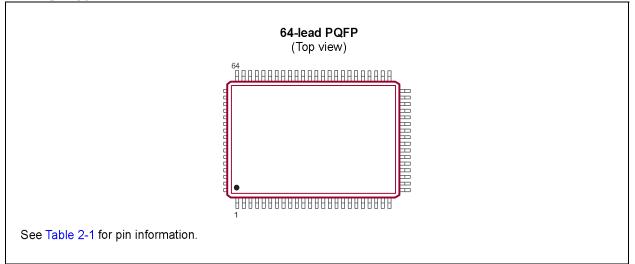
## **General Description**

The HV7620 is a low-voltage serial-to-high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

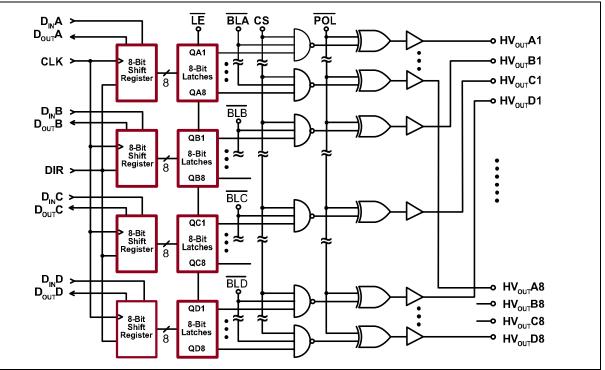
The device has four parallel 8-bit shift registers permitting data rates four times the speed of one. The data is clocked in simultaneously on all four data inputs with a single clock. Data is shifted in on a low-to-high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to  $V_{DD1}$  and counterclockwise (CCW) shifting when connected to LVGND. Operation of the shift register is not affected by the LE (latch enable) input. Transfer of data from the shift registers to the latches occurs when the LE input is high. Data is stored in the latches when LE is low. The current source on the logic inputs provides active pull up when the input pins are open.

#### Package Type



# **Functional Block Diagram**



# 1.0 ELECTRICAL CHARACTERISTICS

# Absolute Maximum Ratings†

$\begin{array}{l} Supply Voltage, V_{DD1} \\ Supply Voltage, V_{DD2} \\ Supply Voltage, V_{PP} \\ Logic Input Levels \\ Maximum Junction Temperature, T_{J(MAX)} \\ Storage Temperature, T_S \\ Continuous Total Power Dissipation: \\ \end{array}$	0.5V to +14V 0.5V to +225V 2V to V <sub>DD1</sub> +2V +125°C 65°C to +150°C
Continuous Total Power Dissipation: 64-lead PQFP (Note 1) ESD Rating (Note 2)	

**†** Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: For operations above 25°C ambient, derate linearly to maximum operating temperature at 20 mW/°C.

2: Device is ESD sensitive. Handling precautions are recommended.

# **RECOMMENDED OPERATING CONDITIONS**

Paramete	er	Sym.	Min.	Тур.	Max.	Unit	Conditions
Logic Supply Voltage		V <sub>DD1</sub>	4.5	_	V <sub>DD2</sub>	V	
12V Supply Voltage		V <sub>DD2</sub>	10.8	_	13.2	V	
High-Voltage Supply Vol	tage	V <sub>PP</sub>	50	_	200	V	
High-Level Input Voltage	)	V <sub>IH</sub>	V <sub>DD1</sub> -0.5V	_	V <sub>DD1</sub>	V	
Low-Level Input Voltage	Low-Level Input Voltage			_	0.5	V	
	V <sub>DD1</sub> = 5V	f	_		10	MHz	
Clock Frequency	V <sub>DD1</sub> = 12V	<sup>f</sup> CLK	_	_	5	MHz	
Operating Junction Tem	perature Range	T <sub>A</sub>	-40	_	+85	°C	
Allowable Pulsed Currer Output Diodes	nt through	lod	_		500	mA	Note 1
Allowable Pulsed V <sub>PP</sub> or HVGND Current		I <sub>GND(VPP)</sub>	—		16	А	Note 1
Slew Rate of V <sub>PP</sub>		V <sub>PP(SLEW)</sub>	_	—	340	V/µs	

**Note 1:** Current pulse width = 500 ns; duty cycle = 5%

# DC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** Over operating supply voltages and temperature, unless otherwise noted,  $V_{DD1} = 5V$ ,  $V_{DD2} = 12V$ ,  $V_{PP} = 200V$  and  $T_1 = 25^{\circ}C$ .

$v_{DD2} = 12v$ , $v_{PP} = 200v$ and $1$	<u>j - 20 0.</u>		1				1
Parameter		Sym.	Min.	Тур.	Max.	Unit	Conditions
V <sub>DD1</sub> Supply Current		I <sub>DD1</sub>	—	_	5	mA	f <sub>CLK</sub> = 10 MHz
V <sub>DD2</sub> Supply Current		I <sub>DD2</sub>	—		22	mA	V <sub>DD2</sub> = 13.2V, f <sub>CLK</sub> = 10 MHz
High Voltage Supply Current		I <sub>PP</sub>			2	mA	All outputs high or low
Quiescent V <sub>DD1</sub> Supply Curren	t	I <sub>DD1Q</sub>	—		100	μA	All input = V <sub>DD1</sub>
Quiescent V <sub>DD2</sub> Supply Curren	t	I <sub>DD2Q</sub>	—		100	μA	All input = V <sub>DD1</sub>
High-Level Output	HV <sub>OUT</sub>	V	185		_	V	I <sub>O</sub> = –50 mA
	Data OUT	V <sub>OH</sub>	V <sub>DD</sub> –1	_		V	<b>I<sub>O</sub> = −100 μA</b>
	HVOUT	V	—	-	20	V	l <sub>O</sub> = +50 mA
Low-Level Output	Data OUT	V <sub>OL</sub>		_	1	V	l <sub>O</sub> = +100 μA
High-Level Logic Input Current		Ι <sub>ΙΗ</sub>	—	-	1	μA	V <sub>IN</sub> = V <sub>DD1</sub>
Low-Level Logic Input Current		կլ	—	_	-10	μA	V <sub>IN</sub> = 0V
HVGND to LVGND Voltage Dif	erence	$V_{GG}$	-1		1	V	

# AC ELECTRICAL CHARACTERISTICS

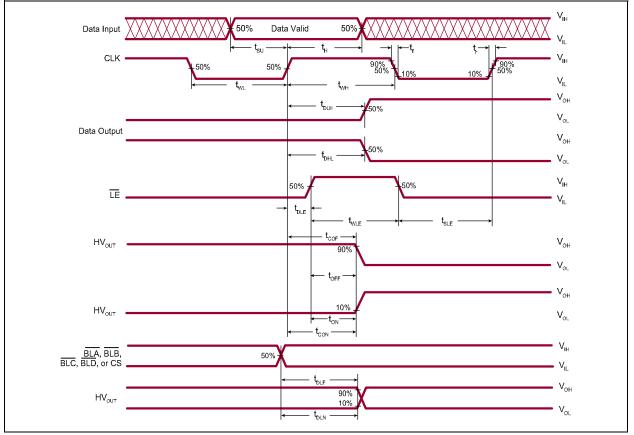
**Electrical Specifications:** Logic signal inputs and data inputs have  $t_r$ ,  $t_f \le 5$  ns.  $V_{DD1} = 5V$  or 12V,  $V_{DD2} = 12V$ ,  $V_{PP} = 200V$  and  $T_J = 25^{\circ}C$ .

vpp – 200 v and 1j – 23	0.						
Parame	ter	Sym.	Min.	Тур.	Max.	Unit	Conditions
Clock Frequency	V <sub>DD1</sub> = 5V	f	—	_	10	MHz	Per register, C <sub>L</sub> = 15 pF
Clock Frequency	V <sub>DD1</sub> = 12V	<sup>−</sup> <sup>f</sup> c∟ĸ	—	—	5	MHz	
Clock Width High or Lov	/	t <sub>wL</sub> , t <sub>wH</sub>	40			ns	
Data Set-Up Time Befor	e Clock Rises	t <sub>s∪</sub>	20			ns	
Data Hold Time after Clo	Data Hold Time after Clock Rises					ns	
Time from Latch Enable	t <sub>ON</sub> , t <sub>OFF</sub>			275	ns	C <sub>L</sub> = 15 pF	
LE Pulse Width		t <sub>WLE</sub>	25		_	ns	
Delay Time Clock to LE	Low to High	t <sub>DLE</sub>	50		_	ns	
LE Set-Up Time before (	Clock Rises	t <sub>SLE</sub>	20		_	ns	
BL or CS Low to High to	HV <sub>OUT</sub>	t <sub>DLF</sub> , t <sub>DLN</sub>		—	250	ns	
Clock to HV <sub>OUT</sub>		t <sub>COF</sub> , t <sub>CON</sub>		—	275	ns	
Delay Time Clock to	V <sub>DD1</sub> = 5V	t		—	250	ns	C <sub>I</sub> = 15 pF
Data Low to High	V <sub>DD1</sub> = 12V	- ФСН			100	ns	
Delay Time Clock to V <sub>DD1</sub> = 5V		<sub>tou</sub>			250	ns	C <sub>L</sub> = 15 pF
Data High to Low	V <sub>DD1</sub> = 12V	- <sup>t</sup> DHL	_	_	100	ns	

# **TEMPERATURE SPECIFICATIONS**

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Junction Temperature	Т <sub>Ј</sub>	-40		+85	°C	
Maximum Junction Temperature	T <sub>J(MAX)</sub>	—	—	+125	°C	
Storage Temperature	Т <sub>S</sub>	-65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
64-lead PQFP	$\theta_{JA}$		41		°C/W	

# Switching Waveforms



# 2.0 PIN DESCRIPTION

The details on the pins of HV7620 are listed on Table 2-1. Refer to **Package Type** for the location of pins.

Pin NumberPin NameDescription1HVGNDHigh-voltage supply ground2VPPHigh-voltage output3HVoUTOBHigh-voltage output4HVoUTCBHigh-voltage output5HVoUTBBHigh-voltage output6HVOUTBBHigh-voltage output7HVOUTD7High-voltage output8HVOUTC7High-voltage output9HVOUTB7High-voltage output10HVOUTB7High-voltage output11HVOUTB6High-voltage output12HVOUTB6High-voltage output13HVOUTC6High-voltage output14HVOUTC6High-voltage output15HVOUTC6High-voltage output16HVOUTC6High-voltage output17HVOUTC6High-voltage output18HVOUTC5High-voltage output19HVOUTC5High-voltage output11HVOUTC5High-voltage output12HVOUTC5High-voltage output13HVOUTC5High-voltage output14HVOUTC5High-voltage output15HVOUTC5High-voltage output16HVOUTC5High-voltage output17HVOUTC5High-voltage output18HVOUTC5High-voltage output19VpPHigh-voltage output21HVOUTC5High-voltage output22JUCDHigh-voltage output23BLCBlanking pins24 <th>IADLE 2-1:</th> <th colspan="11"></th>	IADLE 2-1:											
2       VPP       High-voltage power supply         3       HV <sub>QUT</sub> C8       High-voltage output         4       HV <sub>QUT</sub> C8       High-voltage output         5       HV <sub>QUT</sub> C8       High-voltage output         6       HV <sub>QUT</sub> C8       High-voltage output         7       HV <sub>QUT</sub> C7       High-voltage output         8       HV <sub>QUT</sub> C7       High-voltage output         9       HV <sub>QUT</sub> C7       High-voltage output         10       HV <sub>QUT</sub> A7       High-voltage output         11       HV <sub>QUT</sub> C6       High-voltage output         12       HV <sub>QUT</sub> C6       High-voltage output         13       HV <sub>QUT</sub> C6       High-voltage output         14       HV <sub>QUT</sub> C6       High-voltage output         15       HV <sub>QUT</sub> C6       High-voltage output         16       HV <sub>QUT</sub> C6       High-voltage output         17       HV <sub>QUT</sub> C6       High-voltage output         18       HV <sub>QUT</sub> C5       High-voltage output         19       VpP       High-voltage output         19       VpP       High-voltage supply ground         21       HVGND       High-voltage supply ground         22       VDD2       122       VDD2 <tr< th=""><th>Pin Number</th><th>Pin Name</th><th>Description</th></tr<>	Pin Number	Pin Name	Description									
3 $HV_{OuT}D8$ High-voltage output         4 $HV_{OuT}B8$ High-voltage output         5 $HV_{OuT}B8$ High-voltage output         6 $HV_{OuT}B4$ High-voltage output         7 $HV_{OuT}C7$ High-voltage output         8 $HV_{OuT}C7$ High-voltage output         9 $HV_{ouT}B7$ High-voltage output         10 $HV_{OuT}D7$ High-voltage output         11 $HV_{OuT}D6$ High-voltage output         12 $HV_{ouT}D6$ High-voltage output         13 $HV_{ouT}C6$ High-voltage output         14 $HV_{ouT}C6$ High-voltage output         15 $HV_{ouT}C6$ High-voltage output         16 $HV_{ouT}C5$ High-voltage output         17 $HV_{ouT}C5$ High-voltage output         18 $HV_{ouT}C5$ High-voltage output         19 $V_{PP}$ High-voltage output         20 $HVGND$ High-voltage supply ground         21 $HVGND$ High-voltage supply ground         22 $VDD2$ 12V power supply         23       BLC	1	HVGND	High-voltage supply ground									
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15 $VOUTDS$ High-voltage output16 $HV_{OUT}CS$ High-voltage output17 $HV_{OUT}S$ High-voltage output18 $HV_{OUT}AS$ High-voltage output19 $V_{PP}$ High-voltage output20 $HVGND$ High-voltage supply ground21 $HVGND$ High-voltage supply ground22 $VDD2$ 12V power supply23 $BLC$ Blanking pins24 $BLD$ Blanking pins25 $LE$ Latch enable pin26 $D_{OUT}D$ Data output pin27 $D_{IN}D$ Data input pin28 $D_{IN}C$ Data output pin30 $POL$ Polarity pin31 $LVGND$ Low-voltage supply ground32DIRDirection pin33CSChip select pin34 $D_{OUT}B$ Data input pin35 $D_{IN}B$ Data input pin	13	HV <sub>OUT</sub> B6	High-voltage output									
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17 $HV_{OUT}B5$ High-voltage output18 $HV_{OUT}A5$ High-voltage output19 $V_{PP}$ High-voltage power supply20 $HVGND$ High-voltage supply ground21 $HVGND$ High-voltage supply ground22 $VDD2$ $12V$ power supply23 $BLC$ Blanking pins24 $BLD$ Blanking pins25 $LE$ Latch enable pin26 $D_{OUT}D$ Data output pin27 $D_{IN}D$ Data input pin28 $D_{IN}C$ Data input pin30 $POL$ Polarity pin31 $LVGND$ Low-voltage supply ground32DIRDirection pin33CSChip select pin34 $D_{OUT}B$ Data output pin35 $D_{IN}B$ Data input pin	15	HV <sub>OUT</sub> D5	High-voltage output									
18       HV <sub>OUT</sub> A5       High-voltage output         19       V <sub>PP</sub> High-voltage power supply         20       HVGND       High-voltage supply ground         21       HVGND       High-voltage supply ground         22       VDD2       12V power supply         23       BLC       Blanking pins         24       BLD       Blanking pins         25       LE       Latch enable pin         26       D <sub>OUT</sub> D       Data output pin         27       D <sub>IN</sub> D       Data input pin         28       D <sub>IN</sub> C       Data input pin         29       D <sub>OUT</sub> C       Data output pin         30       POL       Polarity pin         31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin         35       D <sub>IN</sub> B       Data input pin	16	HV <sub>OUT</sub> C5	High-voltage output									
19 $V_{PP}$ High-voltage power supply20HVGNDHigh-voltage supply ground21HVGNDHigh-voltage supply ground22VDD212V power supply23BLCBlanking pins24BLDBlanking pins25LELatch enable pin26 $D_{OUT}D$ Data output pin27 $D_{IND}$ Data input pin28 $D_{INC}$ Data input pin29 $D_{OUT}C$ Data output pin30POLPolarity pin31LVGNDLow-voltage supply ground32DIRDirection pin33CSChip select pin34 $D_{OUT}B$ Data input pin	17	HV <sub>OUT</sub> B5	High-voltage output									
20HVGNDHigh-voltage supply ground21HVGNDHigh-voltage supply ground22VDD212V power supply23BLCBlanking pins24BLDBlanking pins25LELatch enable pin26D <sub>OUT</sub> DData output pin27D <sub>IN</sub> DData input pin28D <sub>IN</sub> CData output pin29D <sub>OUT</sub> CData output pin30POLPolarity pin31LVGNDLow-voltage supply ground32DIRDirection pin33CSChip select pin34D <sub>OUT</sub> BData output pin	18	HV <sub>OUT</sub> A5	High-voltage output									
21       HVGND       High-voltage supply ground         22       VDD2       12V power supply         23       BLC       Blanking pins         24       BLD       Blanking pins         25       LE       Latch enable pin         26       D <sub>OUT</sub> D       Data output pin         27       D <sub>IN</sub> D       Data input pin         28       D <sub>IN</sub> C       Data input pin         29       D <sub>OUT</sub> C       Data output pin         30       POL       Polarity pin         31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin         35       D <sub>IN</sub> B       Data input pin	19	V <sub>PP</sub>	High-voltage power supply									
22       VDD2       12V power supply         23       BLC       Blanking pins         24       BLD       Blanking pins         25       LE       Latch enable pin         26       D <sub>OUT</sub> D       Data output pin         27       D <sub>IN</sub> D       Data input pin         28       D <sub>IN</sub> C       Data output pin         29       D <sub>OUT</sub> C       Data output pin         30       POL       Polarity pin         31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin	20	HVGND	High-voltage supply ground									
23BLCBlanking pins24BLDBlanking pins25LELatch enable pin26D <sub>OUT</sub> DData output pin27D <sub>IN</sub> DData input pin28D <sub>IN</sub> CData output pin29D <sub>OUT</sub> CData output pin30POLPolarity pin31LVGNDLow-voltage supply ground32DIRDirection pin33CSChip select pin34D <sub>OUT</sub> BData output pin35D <sub>IN</sub> BData input pin	21	HVGND	High-voltage supply ground									
24BLDBlanking pins25LELatch enable pin26D <sub>OUT</sub> DData output pin27D <sub>IN</sub> DData input pin28D <sub>IN</sub> CData output pin29D <sub>OUT</sub> CData output pin30POLPolarity pin31LVGNDLow-voltage supply ground32DIRDirection pin33CSChip select pin34D <sub>OUT</sub> BData output pin35D <sub>IN</sub> BData input pin	22	VDD2	12V power supply									
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26D <sub>OUT</sub> DData output pin27D <sub>IN</sub> DData input pin28D <sub>IN</sub> CData input pin29D <sub>OUT</sub> CData output pin30POLPolarity pin31LVGNDLow-voltage supply ground32DIRDirection pin33CSChip select pin34D <sub>OUT</sub> BData output pin35D <sub>IN</sub> BData input pin	24	BLD	Blanking pins									
27DINDData input pin28DINCData input pin29DOUTCData output pin30POLPolarity pin31LVGNDLow-voltage supply ground32DIRDirection pin33CSChip select pin34DOUTBData output pin35DINBData input pin	25	LE	Latch enable pin									
28       D <sub>IN</sub> C       Data input pin         29       D <sub>OUT</sub> C       Data output pin         30       POL       Polarity pin         31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin         35       D <sub>IN</sub> B       Data input pin	26	D <sub>OUT</sub> D	Data output pin									
29       D <sub>OUT</sub> C       Data output pin         30       POL       Polarity pin         31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin         35       D <sub>IN</sub> B       Data input pin	27	D <sub>IN</sub> D	Data input pin									
30       POL       Polarity pin         31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin         35       D <sub>IN</sub> B       Data input pin	28	D <sub>IN</sub> C	Data input pin									
31       LVGND       Low-voltage supply ground         32       DIR       Direction pin         33       CS       Chip select pin         34       D <sub>OUT</sub> B       Data output pin         35       D <sub>IN</sub> B       Data input pin	29	D <sub>OUT</sub> C	Data output pin									
32     DIR     Direction pin       33     CS     Chip select pin       34     D <sub>OUT</sub> B     Data output pin       35     D <sub>IN</sub> B     Data input pin	30	POL	Polarity pin									
33     CS     Chip select pin       34     D <sub>OUT</sub> B     Data output pin       35     D <sub>IN</sub> B     Data input pin	31	LVGND	Low-voltage supply ground									
34     D <sub>OUT</sub> B     Data output pin       35     D <sub>IN</sub> B     Data input pin	32	DIR	Direction pin									
35 D <sub>IN</sub> B Data input pin	33	CS	Chip select pin									
	34	D <sub>OUT</sub> B	Data output pin									
36 D <sub>IN</sub> A Data input pin	35	D <sub>IN</sub> B	Data input pin									
	36	D <sub>IN</sub> A	Data input pin									

TABLE 2-1:	64-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)									
Pin Number	Pin Name	Description								
37	D <sub>OUT</sub> A	Data output pin								
38	CLK	Clock pin								
39	BLA	Blanking pins								
40	BLB	Blanking pins								
41	VDD1	Logic power supply								
42	LVGND	Low-voltage supply ground								
43	N/C	No internal connection								
44	HVGND	High-voltage supply ground								
45	HVGND	High-voltage supply ground								
46	VPP	High-voltage power supply								
47	HV <sub>OUT</sub> D4	High-voltage output								
48	HV <sub>OUT</sub> C4	High-voltage output								
49	HV <sub>OUT</sub> B4	High-voltage output								
50	HV <sub>OUT</sub> A4	High-voltage output								
51	HV <sub>OUT</sub> D3	High-voltage output								
52	HV <sub>OUT</sub> C3	High-voltage output								
53	HV <sub>OUT</sub> B3	High-voltage output								
54	HV <sub>OUT</sub> A3	High-voltage output								
55	HV <sub>OUT</sub> D2	High-voltage output								
56	HV <sub>OUT</sub> C2	High-voltage output								
57	HV <sub>OUT</sub> B2	High-voltage output								
58	HV <sub>OUT</sub> A2	High-voltage output								
59	HV <sub>OUT</sub> D1	High-voltage output								
60	HV <sub>OUT</sub> C1	High-voltage output								
61	HV <sub>OUT</sub> B1	High-voltage output								
62	HV <sub>OUT</sub> A1	High-voltage output								
63	VPP	High-voltage power supply								
64	HVGND	High-voltage supply ground								

TABLE 2-1: 64-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)

#### 3.0 **FUNCTIONAL DESCRIPTION**

Follow the steps in Table 3-1 to power up and power down the HV7620.

#### TABLE 3-1: **POWER-UP AND POWER-DOWN SEQUENCE**

	Power-Up	Power-Down						
Step	Description	Step	Description					
1	GND (HV, LV)	1	Logic Input Signals					
2	V <sub>DD1</sub>	2	V <sub>PP</sub>					
3	V <sub>DD2</sub>	3	V <sub>DD2</sub>					
4	V <sub>PP</sub>	4	V <sub>DD1</sub>					
5	Logic Input Signals	5	GND (HV, LV)					

#### TRUTH FUNCTION TABLE<sup>1</sup> TABLE 3-2:

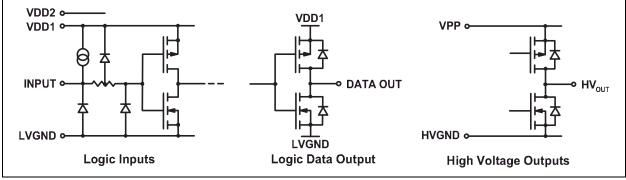
Function						I	nputs							HV <sub>OUT</sub>				
Function	D <sub>IN</sub> A	D <sub>IN</sub> B	DINC	D <sub>IN</sub> D	CLK	LE	DIR	BLA	BLB	BLC	BLD	CS	POL	Α	В	С	D	
All O/P High	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	L	Н	Н	Н	Н	
All O/P Low	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	Н	L	L	L	L	
"A" (Note 3) Outputs Low	х	х	х	х	х	х	х	L	х	х	х	х	н	L	Note 2	Note 2	Note 2	
Normal Polarity	х	х	х	х	х	х	х	н	Н	н	н	н	н	No Inversion				
Outputs Inverted	х	х	х	х	х	х	х	н	н	н	н	н	L		Inversion			
Transpar- ent Mode	Н	L	L	L	Ť	Н	х	н	Н	н	н	н	н	н	L	L	L	
Data Stored	Х	Х	Х	Х	Х	L	Х	Н	Н	Н	Н	Н	Н		Store	d data		
														A <sub>N</sub>	B <sub>N</sub>	C <sub>N</sub>	D <sub>N</sub>	
Shift CW <sup>A</sup>	Х	Х	х	х	1	Н	н	н	Н	н	н	н	х	$\rightarrow$	$\rightarrow$	$\rightarrow$	$\rightarrow$	
														A <sub>N+1</sub>	B <sub>N+1</sub>	C <sub>N+1</sub>	D <sub>N+1</sub>	
														$A_{N}$	B <sub>N</sub>	C <sub>N</sub>	$D_N$	
Shift CCW <sup>B</sup>	Х	Х	х	х	1	н	L	н	н	н	н	н	х	$\rightarrow$	$\rightarrow$	$\rightarrow$	$\rightarrow$	
														A <sub>N-1</sub>	B <sub>N-1</sub>	C <sub>N-1</sub>	D <sub>N-1</sub>	

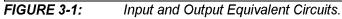
Note 1: H = High logic level L = Low logic level

X = Irrelevant

↑ = Low-to-high transition

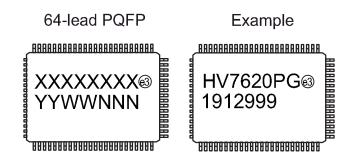
- 2: Dependent on previous stage's state before the last CLK ↑ or last LE high
- 3: BLB, BLC and BLD will have a similar effect on their respective output.





# HV7620

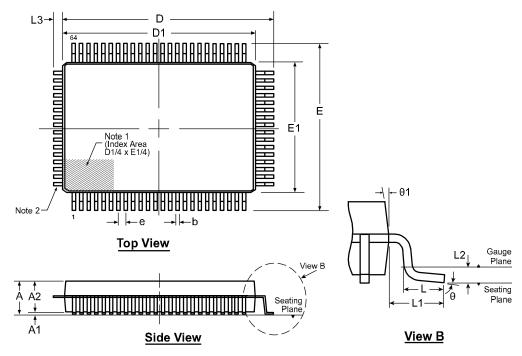
- 4.0 PACKAGE MARKING INFORMATION
- 4.1 Packaging Information



Legend	I: XXX Y YY WW NNN @3 *	Product Code or Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available s for product code or customer-specific information. Package may or e the corporate logo.

# 64-Lead PQFP (3-Sided) Package Outline (PG)

20.00x14.00mm body, 3.40mm height (max), 0.80mm pitch, 3.90mm footprint



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

- 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.2. The leads on this side are trimmed.

Sym	ool	Α	<b>A</b> 1	A2	b	D	D1	Е	E1	е	L	L1	L2	L3	θ	θ1
Dimen-	MIN	2.80	0.25	2.55	0.30	22.25	19.80	17.65	13.80		0.73				0 <sup>0</sup>	5 <sup>0</sup>
sion	NOM	-	-	2.80	-	22.50	20.00	17.90	14.00	0.80 BSC	0.88	1.95 REF	0.25 BSC	0.55 REF	3.5 <sup>0</sup>	-
(mm)	MAX	3.40	0.50	3.05	0.45	22.75	20.20	18.15	14.20		1.03				7 <sup>0</sup>	16 <sup>0</sup>

Drawings not to scale.

# APPENDIX A: REVISION HISTORY

## **Revision A (January 2019)**

- Converted Supertex Doc# DSFP-HV7620 to Microchip DS20005779A
- Removed "HVCMOS<sup>®</sup> Technology" from the Features section
- Changed the package marking format
- Made minor text changes throughout the document

# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	<u>xx</u>	-	¥ -	¥	Example:	
Device	Package Options		Environmental Med	dia Type	a) HV7620PG-G:	40 MHz 32-Channel Serial-to- Parallel Converter with Push- Pull Outputs, 64-lead PQFP, 66/Tray
Device:	HV7620	=	40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull Outputs			
Package:	PG	=	64-lead PQFP			
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package			
Media Type:	(blank)	=	66/Tray for a PG Package			

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SYST-31RUBG366 - Data Sheet - HV7620 40 MHz 32-Channel Serial-to-Parallel Converter with Push-Pull

Affected Catalog Part Numbers(CPN)

HV7620ND HV7620PG-G