Product Change Notification - SYST-01WULB292

Date:

03 Oct 2018

Product Category:

Motor Drivers

Affected CPNs:

Notification subject:

Data Sheet - MCP8025A/MCP8026 3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module

Notification text:

Notification Status: Final

Description of Change:

1) Updated “Features” section, removed “AEC-Q100 Grade 0 Qualified”.
2) Updated “Applications” section.
3) Updated Note 2 in “AC/DC Characteristics” table.
4) Updated “ESD, Susceptibility, Surge and Latch-up Testing” table.
5) Updated Section 4.5.1 “LIN Bus Transceiver (MCP8025A)”.
6) Updated Section 4.5.2 “Level Translator (MCP8026)”.
7) Updated Section 6.4 “External MOSFET DUVLO and OCP Detection”.
8) Added Section 6.10 “Buck Start-up Issue” in Section 6.0 “Errata”.

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 03 Oct 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

SYST-01WULB292

Microchip has released a new DeviceDoc for the MCP8025A/MCP8026 3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module of devices. If you are using one of these devices please read the document located at MCP8025A/MCP8026 3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module.

Attachment(s):

MCP8025A/MCP8026 3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module

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MCP8025A/6

3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode and LIN Transceiver

Features

- Quiescent Current:
  - Sleep mode: 5 µA Typical
  - Standby mode: < 200 µA
- LIN Transceiver Interface **(MCP8025A)**:
  - Compliant with LIN Bus Specifications 1.3, 2.2 and SAE J2602
  - Supports baud rates up to 20 Kbaud
  - Internal pull-up resistor and diode
  - Protected against ground shorts
  - Protected against loss of ground
  - Automatic thermal shutdown
  - LIN bus dominant time-out
- Three Half-Bridge Drivers Configured to Drive External High-Side NMOS and Low-Side NMOS MOSFETs:
  - Independent input control for high-side NMOS and low-side NMOS MOSFETs
  - Peak output current: 0.5A at 12V
  - Shoot-through protection
  - Overcurrent and short-circuit protection
- Adjustable Output Buck Regulator (750 mW)
- Fixed Output Linear Regulators:
  - 5V at 30 mA
  - 12V at 30 mA
- Operational Amplifiers:
  - One in MCP8025A
  - Three in MCP8026
- Overcurrent Comparator with DAC Reference
- Phase Comparator with Multiplexer **(MCP8025A)**
- Neutral Simulator **(MCP8025A)**
- Level Translators **(MCP8026)**
- Input Voltage Range: 6V to 40V
- Operational Voltage Range:
  - 6V to 19V **(MCP8025A)**
  - 6V to 28V **(MCP8026)**
- Buck Regulator Undervoltage Lockout: 4V
- Undervoltage Lockout (UVLO): 5.5V (Except Buck)
- Overvoltage Lockout (OVLO):
  - 20V **(MCP8025A)**
  - 32V **(MCP8026)**
- Transient (100 ms) Voltage Tolerance: 48V
- Extended Temperature Range (T_A): -40 to +150°C
- Thermal Shutdown

Applications

- Industrial Fuel, Water, Ventilation Motors
- Home Appliances
- Permanent Magnet Synchronous Motor (PMSM) Control
- Hobby Aircraft, Boats, Vehicles

Description

The MCP8025A/6 devices are 3-phase Brushless DC (BLDC) power modules, containing three integrated half-bridge drivers, capable of driving three external NMOS/NMOS transistor pairs. The three half-bridge drivers are capable of delivering a peak output current of 0.5A at 12V for driving high-side and low-side NMOS MOSFET transistors. The drivers have shoot-through, overcurrent and short-circuit protection. A Sleep mode has been added to achieve a typical “key-off” quiescent current of 5 µA.

The MCP8025A device integrates a comparator, a buck voltage regulator, two LDO regulators, power monitoring comparators, an overtemperature sensor, a LIN transceiver, a zero-crossing detector, a neutral simulator and an operational amplifier for motor current monitoring. The phase comparator and multiplexer allow for hardware commutation detection. The neutral simulator allows commutation detection without a neutral tap in the motor. The buck converter is capable of delivering 750 mW of power for powering a companion microcontroller. The buck regulator may be disabled if not used. The on-board 5V and 12V Low-Dropout (LDO) voltage regulators are capable of delivering 30 mA of current.

The MCP8026 device replaces the LIN transceiver, neutral simulator and zero-crossing detector in MCP8025A with two level shifters, and two additional op amps.

The MCP8025A/6 operation is specified over a temperature range of -40°C to +150°C.

Package options include 40-Lead 5x5 QFN and 48-Lead 7x7 TQFP with Exposed Pad (EP).

LOCAL INTERCONNECT NETWORK

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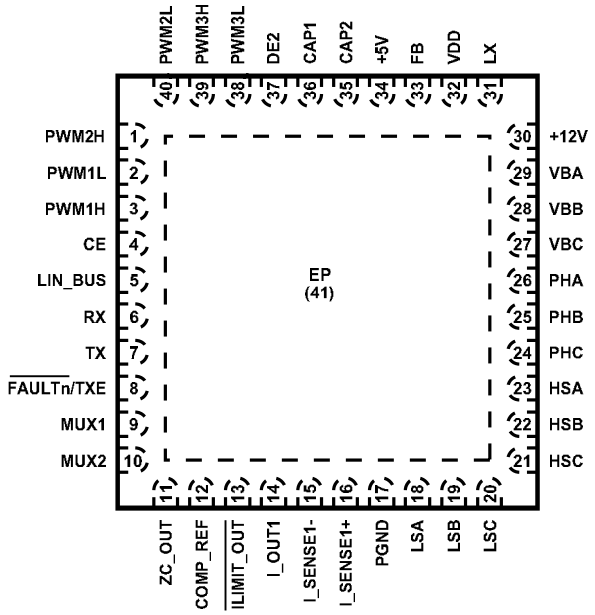
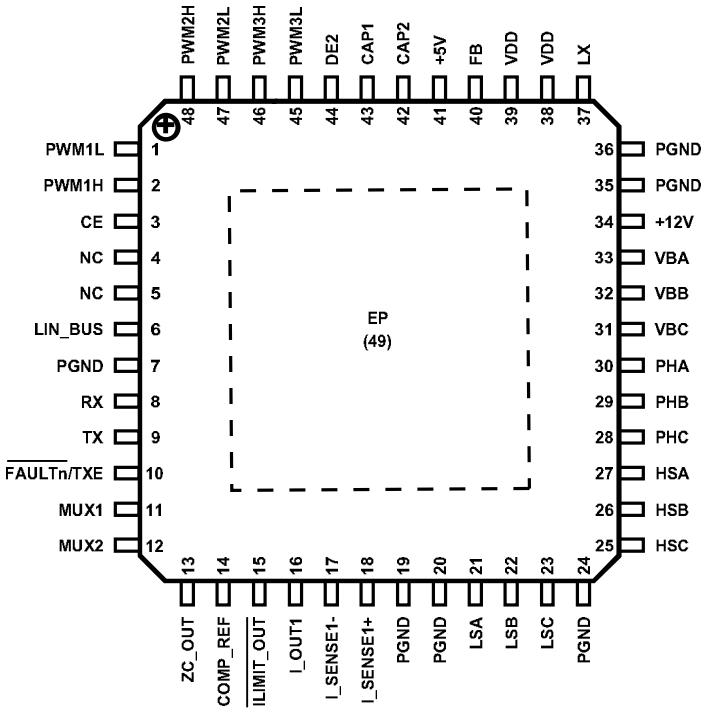
Package Types – MCP8025A

5 mm x 5 mm QFN-40*



7 mm x 7 mm TQFP-48*



* Includes Exposed Thermal Pad (EP), see Table 3-1.

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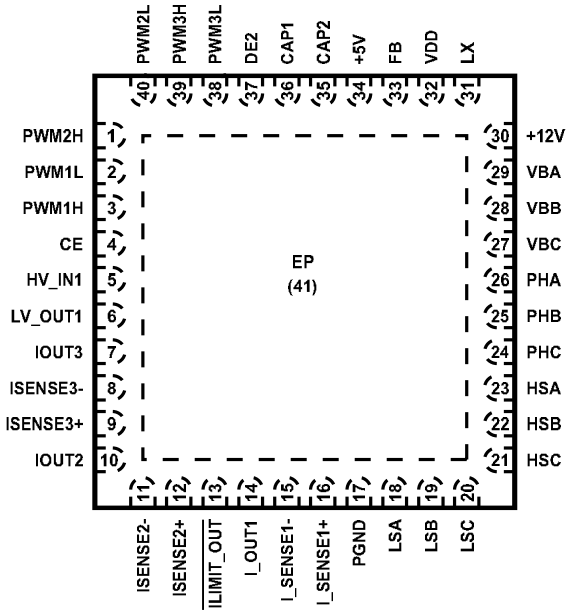
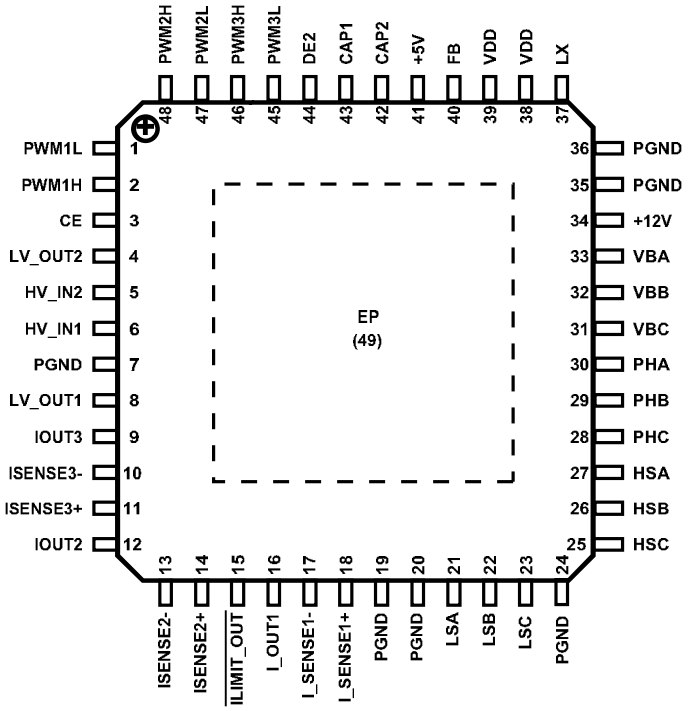
Package Types – MCP8026

5 mm x 5 mm QFN-40*

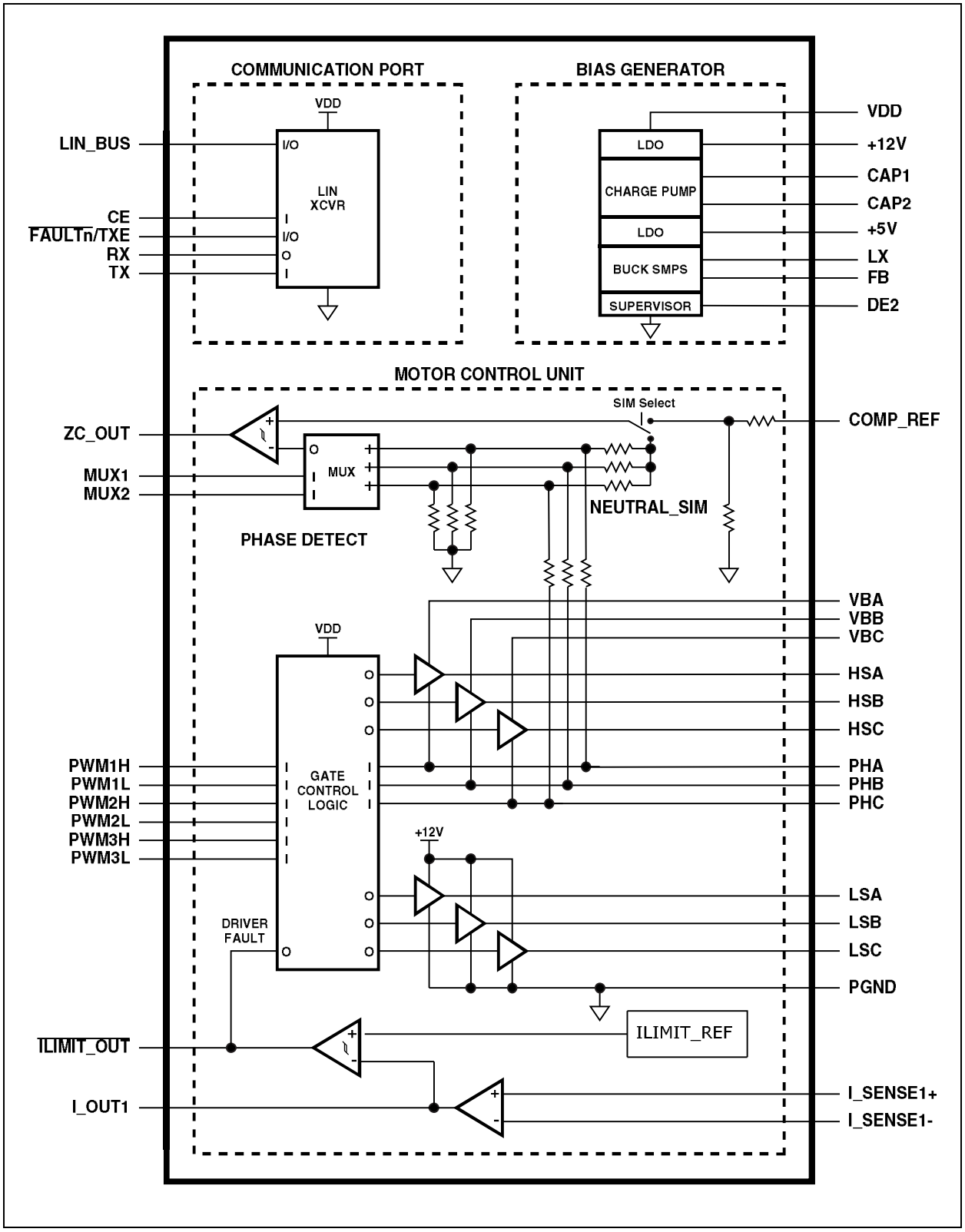


7 mm x 7 mm TQFP-48*



* Includes Exposed Thermal Pad (EP), see Table 3-2.

Functional Block Diagram – MCP8025A



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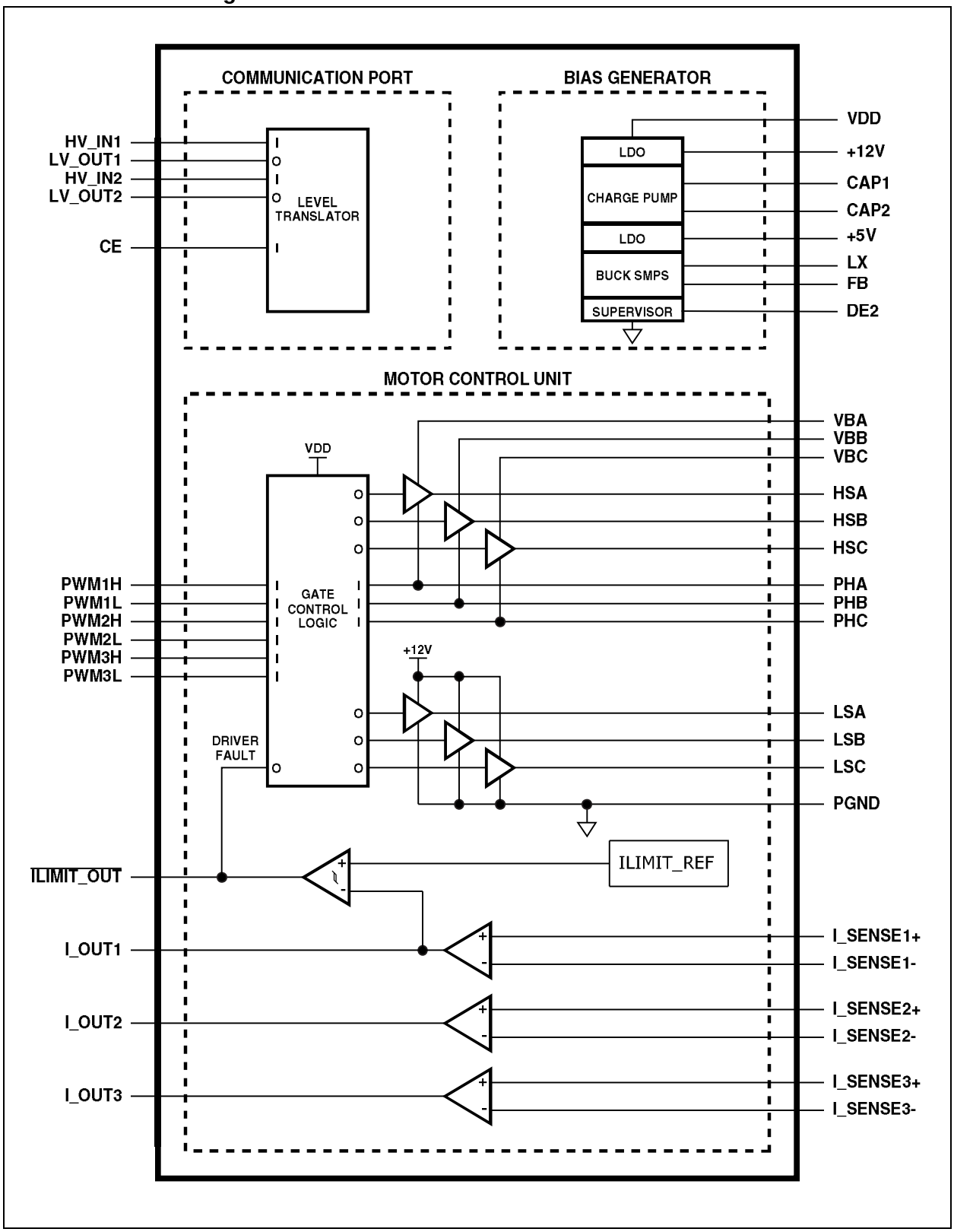
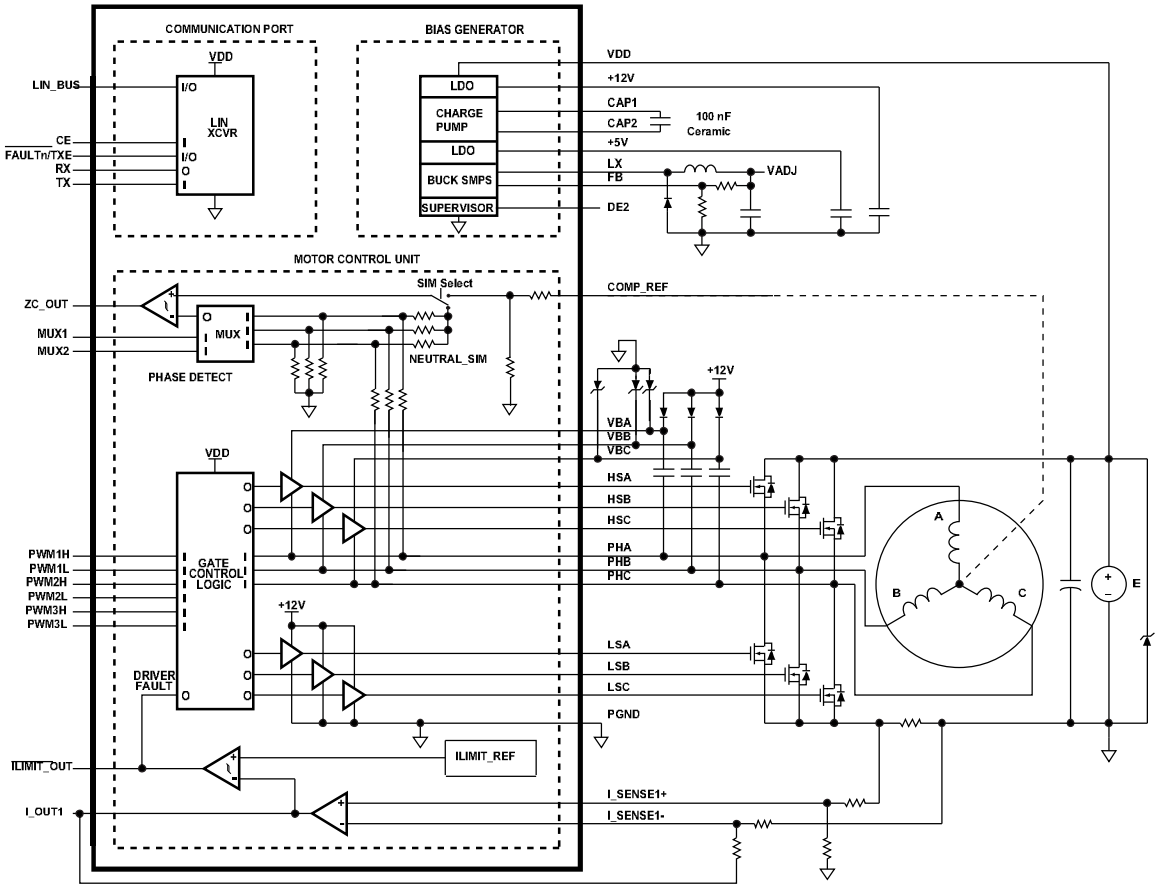
Functional Block Diagram – MCP8026



Typical Application Circuit – MCP8025A



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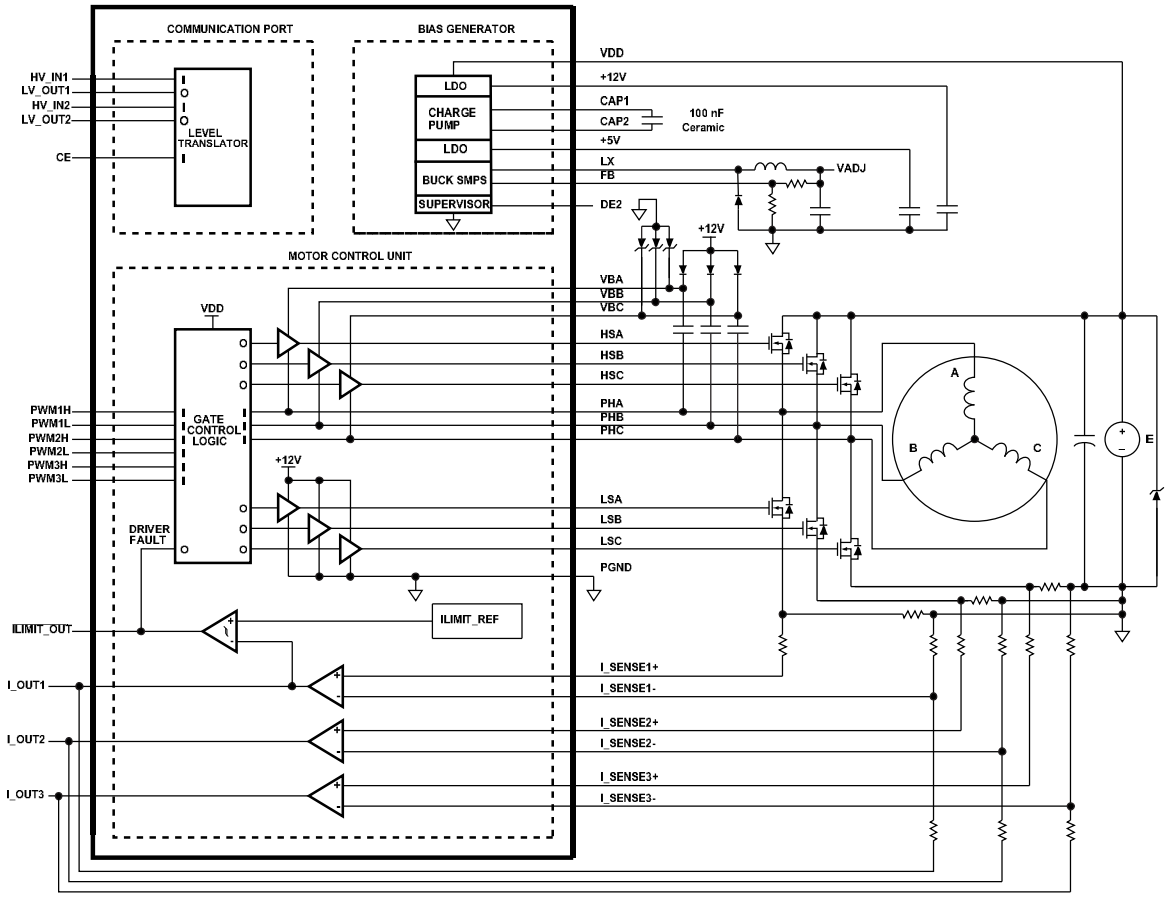
Typical Application Circuit – MCP8026



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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Digital Open-Drain Drive Strength	$DIGITAL_{IOL}$	—	1	—	mA	V_{DS} < 50 mV
Digital Input Rising Threshold	$V_{DIG_HI_TH}$	1.26	—	—	V	
Digital Input Falling Threshold	$V_{DIG_LO_TH}$	—	—	0.54	V	
Digital Input Hysteresis	V_{DIG_HYS}	—	500	—	mV	
Digital Input Current	I_{DIG}	—	30	100	µA	V_{DIG} = 3V
		—	0.2	—		V_{DIG} = 0V
Analog Low-Voltage Input	$ANALOG_{VIN}$	0	—	5.5	V	Excludes LIN and high-voltage pins
Analog Low-Voltage Output	$ANALOG_{VOUT}$	0	—	V_{OUT5}	V	Excludes LIN and high-voltage pins
BIAS GENERATOR						
+12V Regulated Charge Pump						
Charge Pump Current	I_{CP}	20	—	—	mA	V_{DD} = 9V
Charge Pump Start	CP_{START}	11	11.5	—	V	V_{DD} falling
Charge Pump Stop	CP_{STOP}	—	12	12.5	V	V_{DD} rising
Charge Pump Frequency (50% charging/ 50% discharging)	CP_{FSW}	—	76.8	—	kHz	V_{DD} = 9V
		—	0	—		V_{DD} = 13V (stopped)
Charge Pump Switch Resistance	CP_{RDSON}	—	14	—	Ω	RDS_{ON} sum of high side and low side
Output Voltage	V_{OUT12}	—	12	—	V	$V_{DD} \geq$ 7.5V, C_{PUMP} = 100 nF, I_{OUT} = 20 mA
		—	9	—		V_{DD} = 5.1V, C_{PUMP} = 260 nF, I_{OUT} = 15 mA
Output Voltage Tolerance	$\|TOLV_{OUT12}\|$	—	—	4	%	I_{OUT} = 1 mA
Output Current	I_{OUT}	30	—	—	mA	Average current
Output Current Limit	I_{LIMIT}	40	50	—	mA	Average current
Output Voltage Temperature Coefficient	TCV_{OUT12}	—	50	—	ppm/°C	**(Note 2)**
Line Regulation	$\|\Delta V_{OUT}/(V_{OUT} \times \Delta V_{DD})\|$	—	0.1	0.5	%/V	13V < V_{DD} < 19V, I_{OUT} = 20 mA
Load Regulation	$\|\Delta V_{OUT}/V_{OUT}\|$	—	0.2	0.5	%	I_{OUT} = 0.1 mA to 15 mA
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA **(Note 2)**
+5V Linear Regulator						
Output Voltage	V_{OUT5}	—	5	—	V	V_{DD} = V_{OUT5} + 1V, I_{OUT} = 1 mA
Output Voltage Tolerance	$\|TOLV_{OUT5}\|$	—	—	4	%	
Output Current	I_{OUT}	30	—	—	mA	Average current
Output Current Limit	I_{LIMIT}	40	50	—	mA	Average current
Output Voltage Temperature Coefficient	$\|TCV_{OUT5}\|$	—	50	—	ppm/°C	**(Note 2)**

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are ensured by design and characterization, not production tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Line Regulation	$\lvert\Delta V_{OUT}/(V_{OUT} \times \Delta V_{DD})\rvert$	—	0.1	0.5	%/V	6V < V_{DD} < 19V, I_{OUT} = 20 mA
Load Regulation	$\lvert\Delta V_{OUT}/V_{OUT}\rvert$	—	0.2	0.5	%	I_{OUT} = 0.1 mA to 15 mA
Dropout Voltage	$V_{DD} - V_{OUT5}$	—	180	350	mV	I_{OUT} = 20 mA, measurement taken when output voltage drops 2% from no load value
Power Supply Rejection Ratio	PSRR	—	60	—	dB	f = 1 kHz, I_{OUT} = 10 mA **(Note 2)**
Buck Regulator						
Feedback Voltage	V_{FB}	1.19	1.25	1.31	V	
Feedback Voltage Tolerance	$\lvert TOLV_{FB}\rvert$	—	—	5	%	I_{FB} = 1 µA
Feedback Voltage Line Regulation	$\lvert(\Delta V_{FB}/V_{FB})/\Delta V_{DD}\rvert$	—	0.1	0.5	%/V	V_{DD} = 6V to 28V
Feedback Voltage Load Regulation	$\lvert\Delta V_{FB}/V_{FB}\rvert$	—	0.1	0.5	%	I_{OUT} = 5 mA to 150 mA
Feedback Input Bias Current	I_{FB}	-100	—	+100	nA	Sink/Source **(Note 2)**
Feedback Voltage to Shut Down Buck Regulator	V_{BUCK_DIS}	2.5	—	5.5	V	V_{DD} > 6V
Switching Frequency	f_{SW}	—	461	—	kHz	
Duty Cycle Range	DC_{MAX}	3	—	96	%	**(Note 2)**
PMOS Switch-On Resistance	R_{DSON}	—	0.6	—	Ω	T_J = 25°C
PMOS Switch Current Limit	$I_{P(MAX)}$	—	2.5	—	A	
Ground Current – PWM Mode	I_{GND}	—	1.5	2.5	mA	Switching **(Note 2)**
Quiescent Current – PFM Mode	I_Q	—	150	200	µA	I_{OUT} = 0 mA **(Note 2)**
Output Voltage Adjust Range	V_{OUT}	2	—	5	V	**(Note 2)**
Output Current	I_{OUT}	150	—	—	mA	5V, $V_{DD} - V_{OUT}$ > 0.5V
		250	—	—		3V, $V_{DD} - V_{OUT}$ > 0.5V
Output Power	P_{OUT}	—	750	—	mW	P = $I_{OUT} \times V_{OUT}$ 2.5A peak current **(Note 2)**
Voltage Supervisor						
Buck Input Undervoltage Lockout – Start-up	$UVLO_{BK_STRT}$	—	4.3	4.5	V	V_{DD} rising
Buck Input Undervoltage Lockout – Shutdown	$UVLO_{BK_STOP}$	3.8	4	—	V	V_{DD} falling
Buck Input Undervoltage Lockout Hysteresis	$UVLO_{BK_HYS}$	—	0.3	—	V	
5V LDO Undervoltage Fault Inactive	$UVLO_{5VLDO_INACT}$	—	4.5	—	V	V_{OUT5} rising **(Note 2)**
5V LDO Undervoltage Fault Active	$UVLO_{5VLDO_ACT}$	—	4	—	V	V_{OUT5} falling **(Note 2)**
5V LDO Undervoltage Fault Hysteresis	$UVLO_{5VLDO_HYS}$	—	0.5	—	V	**(Note 2)**

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are ensured by design and characterization, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input Undervoltage Lockout – Start-up	$UVLO_{STRT}$	—	6	6.25	V	V_{DD} rising
Input Undervoltage Lockout – Shutdown	$UVLO_{STOP}$	5.1	5.5	—	V	V_{DD} falling
Input Undervoltage Lockout Hysteresis	$UVLO_{HYS}$	0.2	0.45	0.70	V	
Input Overvoltage Lockout – Driver Disabled **(MCP8025A)**	$DOVLO_{STOP}$	—	20	20.5	V	V_{DD} rising
Input Overvoltage Lockout – Driver Enabled **(MCP8025A)**	$DOVLO_{STRT}$	18.75	19.5	—	V	V_{DD} falling
Input Overvoltage Lockout Hysteresis **(MCP8025A)**	$DOVLO_{HYS}$	0.15	0.5	0.75	V	
Input Overvoltage Lockout – All Functions Disabled	$AOVLO_{STOP}$	—	32	33	V	V_{DD} rising
Input Overvoltage Lockout – All Functions Enabled	$AOVLO_{STRT}$	29	30	—	V	V_{DD} falling
Input Overvoltage Lockout Hysteresis	$AOVLO_{HYS}$	1	2	3	V	
Temperature Supervisor						
Thermal Warning Temperature	T_{WARN}	—	72	—	$\%T_{SD}$	Rising temperature (+115°C) **(Note 2)**
Thermal Warning Hysteresis	ΔT_{WARN}	—	15	—	°C	Falling temperature **(Note 2)**
Thermal Shutdown Temperature	T_{SD}	160	170	—	°C	Rising temperature **(Note 2)**
Thermal Shutdown Hysteresis	ΔT_{SD}	—	25	—	°C	Falling temperature **(Note 2)**
MOTOR CONTROL UNIT						
Output Drivers						
PWMH/L Input Pull-Down	R_{PULLDN}	—	47	—	kΩ	
Output Driver Source Current	I_{SOURCE}	0.3	—	—	A	V_{DD} = 12V, HS[A:C], LS[A:C]
Output Driver Sink Current	I_{SINK}	0.3	—	—	A	V_{DD} = 12V, HS[A:C], LS[A:C]
Output Driver Source Resistance	R_{DSON}	—	17	—	Ω	I_{OUT} = 10 mA, V_{DD} = 12V, HS[A:C], LS[A:C]
Output Driver Sink Resistance	R_{DSON}	—	17	—	Ω	I_{OUT} = 10 mA, V_{DD} = 12V, HS[A:C], LS[A:C]
Output Driver Blanking	t_{BLANK}	500	—	4000	ns	Configurable **(Note 2)**
Output Driver UVLO Threshold	D_{UVLO}	7.2	8	—	V	Configuration Register 0 bit 3 = 0
Output Driver UVLO Minimum Duration	t_{DUVLO}	t_{BLANK} + 700	—	t_{BLANK} + 1400	ns	Fault latched after t_{DUVLO} **(Note 2)**
Output Driver HS Drive Voltage	V_{HS}	8	12	13.5	V	With respect to the phase pin
		-5.5	—	—		With respect to ground
Output Driver LS Drive Voltage	V_{LS}	8	12	13.5	V	With respect to ground

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are ensured by design and characterization, not production tested.

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Driver Bootstrap Voltage	$V_{BOOTSTRAP}$	—	—	—	V	With respect to ground **(Note 2)**
		—	—	44		Continuous
		—	—	48		< 100 ms
Output Driver Phase Pin Voltage	V_{PHASE}	—	—	—	V	With respect to ground **(Note 2)**
		-5.5	—	44		Continuous
		-5.5	—	48		< 100 ms
Output Driver Short-Circuit Protection Threshold High Side (V_{DD} – V_{PHx}) Low Side (V_{PHx} – P_{GND})	D_{SC_THR}	—	—	—	V	Set in CFG0 register **(Note 2)**
		—	0.250	—		00 (default)
		—	0.500	—		01
		—	0.750	—		10
		—	1.000	—		11
Output Driver Short-Circuit Detected Propagation Delay	T_{SC_DLY}	—	—	—	ns	C_{LOAD} = 1000 pF, V_{DD} = 12V **(Note 2)**
		—	430	—		Detection after blanking
		—	10	—		Detection during blanking, value is delayed after blanking
Output Driver OVLO Turn-Off Delay	T_{OVLO_DLY}	3	5	—	µs	Detection synchronized with internal clock **(Note 2)**
Power-up or Sleep to Standby	t_{POWER}	—	—	—	ms	CE high-low-high transition < 100 µs (Fault clearing) **(Note 2)**
		—	10	—		**MCP8025A**
		—	5	—		**MCP8026**
Standby to Motor Operational	t_{MOTOR}	—	5	—	µs	CE high-low-high transition < 0.9 ms (Fault clearing)
		—	—	5	ms	Standby state to Operational state **(MCP8025A) (Note 2)**
		—	—	10	ms	Standby state to Operational state (**MCP8026) (Note 2)**
Fault to Driver Output Turn-Off	T_{FAULT_OFF}	—	—	—	µs	C_{LOAD} = 1000 pF, V_{DD} = 12V, time after Fault occurs **(Note 2)**
		—	1	—		UVLO, OCP Faults
		—	10	—		All other Faults
CE Low to Driver Output Turn-Off	T_{DEL_OFF}	—	100	250	ns	C_{LOAD} = 1000 pF, V_{DD} = 12V, time after CE = low **(Note 2)**
CE Low to Standby State	$t_{STANDBY}$	—	1	—	ms	Time after CE = low, SLEEP bit = 0 **(Note 2)**
CE Low to Sleep State	t_{SLEEP}	—	1	—	ms	Time after CE = low, SLEEP bit = 1 **(Note 2)**
CE Fault Clearing Pulse	t_{FAULT_CLR}	4	—	900	µs	CE high-low-high transition time **(Note 2)**

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Current Sense Amplifier						
Input Offset Voltage	V_{OS}	-3	—	+3	mV	V_{CM} = 0V, T_A = -40°C to +150°C
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±2	—	µV/°C	V_{CM} = 0V **(Note 2)**
Input Bias Current	I_B	-1	—	+1	µA	
Common-Mode Input Range	V_{CMR}	-0.3	—	3.5	V	**(Note 2)**
Common-Mode Rejection Ratio	CMRR	—	80	—	dB	Frequency = 1 kHz, I_{OUT} = 10 µA **(Note 2)**
Maximum Output Voltage Swing	V_{OL}, V_{OH}	0.05	—	4.5	V	I_{OUT} = 200 µA
Slew Rate	SR	—	±7	—	V/µs	Symmetrical **(Note 2)**
Gain Bandwidth Product	GBWP	—	10	—	MHz	**(Note 2)**
Current Comparator Hysteresis	CC_{HYS}	—	10	—	mV	**(Note 2)**
Current Comparator Common-Mode Input Range	V_{CC_CMR}	1	—	4.5	V	**(Note 2)**
Current Limit DAC						
Resolution		—	8	—	bits	
Output Voltage Range	V_{OL}, V_{OH}	0.991	—	4.503	V	I_{OUT} = 1 mA
Output Voltage	V_{DAC}	—	—	—	V	CFG1 code x 13.77 mV/bit + 0.991V **(Note 2)**
		—	0.991	—		Code 00H
		—	1.872	—		Code 40H
		—	4.503	—		Code FFH
Input to Output Delay	T_{DELAY}	—	50	—	µs	**(Note 2)**
Integral Nonlinearity	INL	-0.5	—	+0.5	%FSR	%Full Scale Range **(Note 2)**
Differential Nonlinearity	DNL	-50	—	+50	%LSB	%LSB **(Note 2)**
$\overline{ILIMIT_OUT}$ Sink Current (open-drain)	IL_{OUT}	—	1	—	mA	$V_{ILIMIT_OUT} \leq$ 50 mV
ZC Back EMF Sampler Comparator (MCP8025A)						
Maximum Output Voltage Swing	ZCV_{OL}, ZCV_{OH}	0.05	—	5	V	I_{OUT} = 1 mA
Reference Input Impedance	ZC_{ZREF}	—	83	—	kΩ	**(Note 2)**
Input to Output Delay	ZC_{DELAY}	—	—	500	ns	V_{IN_STEP} = 500 mV **(Note 2)**
Voltage Divider RC Time Constant	ZC_{TRC}	—	100	—	ns	**(Note 2)**
ZC Output Pull-up Range	$ZC_{RPULLUP}$	3.3	10	—	kΩ	**(Note 2)**
ZC Output Sink Current (open-drain)	ZC_{IOL}	—	1	—	mA	$V_{OUT} \leq$ 50 mV

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AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Back EMF Sampler Phase Multiplexer (MCP8025A)						
MUX[1:2] Input Pull-Down	R_{PULLDN}	—	47	—	kΩ	**(Note 2)**
Transition Time	t_{TRAN}	—	150	250	ns	**(Note 2)**
Delay from MUX Select to ZC Out	MUX_{DELAY}	—	210	—	ns	**(Note 2)**
Phase Filter Capacitors	C_{PHASE}	—	1.5	—	pF	MUX input to ground **(Note 2)**
COMMUNICATION PORTS						
Standard LIN (MCP8025A)						
Microcontroller Interface						
TX Input Pull-up Resistor	R_{PUTXD}	—	48	—	kΩ	Pull up to 5V
Bus Interface						
LIN Bus High-Level Input Voltage	V_{HI}	0.6 x V_{DD}	—	—	V	Recessive state
LIN Bus Low-Level Input Voltage	V_{LO}	—	—	0.4 x V_{DD}	V	Dominant state
LIN Bus Input Hysteresis	V_{HYS}	—	—	0.175 x V_{DD}	V	$V_{HI} - V_{LO}$
LIN Bus Low-Level Output Current	I_{OL}	7.3	—	—	mA	V_O = 0.2 x V_{DD}, V_{DD} = 8V
		16.5	—	—		V_O = 0.2 x V_{DD}, V_{DD} = 18V
		30.6	—	—		V_O = 0.251 x V_{DD}, V_{DD} = 18V
LIN Bus Input Pull-up Current	I_{PU}	5	—	180	µA	
LIN Bus Short-Circuit Current Limit	I_{SC}	50	—	200	mA	
LIN Bus Low-Level Output Voltage	V_{OL}	—	—	0.2 x V_{DD}	V	
LIN Bus Input Leakage Current (at receiver during dominant bus level)	$I_{BUS_PAS_DOM}$	-1	—	—	mA	Driver off, V_{BUS} = 0V, V_{DD} = 12V
LIN Bus Input Leakage Current (at receiver during recessive bus level)	$I_{BUS_PAS_REC}$	—	12	20	µA	Driver off, $V_{BUS} \geq V_{DD}$, 7V < V_{BUS} < 19V, 7V < V_{DD} < 19V
LIN Bus Input Leakage Current (disconnected from ground)	$I_{BUS_NO_GND}$	-1	—	1	mA	GND = V_{DD} = 12V, 0V < V_{BUS} < 19V
LIN Bus Input Leakage Current (disconnected from V_{DD})	$I_{BUS_NO_BAT}$	—	—	10	µA	V_{DD} = 0V, 0V < V_{BUS} < 19V
Receiver Center Voltage	V_{BUS_CNT}	0.475 x V_{DD}	0.5 x V_{DD}	0.525 x V_{DD}	V	$V_{BUS_CNT} = (V_{HI} - V_{LO})/2$
LIN Bus Slave Pull-up Resistance	R_{PULLUP}	20	30	47	kΩ	
LIN Dominant State Time-out	t_{DOM_TOUT}	—	25	—	ms	**(Note 2)**
Propagation Delay	T_{RX_PD}	—	3	6	µs	Propagation delay of receiver
Symmetry	T_{RX_SYM}	-2	—	+2	µs	Symmetry of receiver propagation delay rising edge w.r.t. falling edge

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are ensured by design and characterization, not production tested.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, T_J = -40°C to +150°C, typical values are for +25°C, V_{DD} = 13V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Voltage Level Translators (MCP8026)						
High-Voltage Input Range	V_{IN}	0	—	V_{DD}	V	
Low-Voltage Output Range	V_{OUT}	0	—	5	V	
Input Pull-up Resistor	RPU	—	30	—	kΩ	
High-Level Input Voltage	V_{IH}	0.6	—	—	V_{DD}	V_{DD} = 15V
Low-Level Input Voltage	V_{IL}	—	—	0.4	V_{DD}	V_{DD} = 15V
Input Hysteresis	V_{HYS}	—	0.24	—	V_{DD}	
Propagation Delay	T_{LV_OUT}	—	3	6	µs	**(Note 2)**
Maximum Communication Frequency	F_{MAX}	—	—	20	kHz	**(Note 2)**
Low-Voltage Output Sink Current (open-drain)	I_{OL}	—	1	—	mA	$V_{OUT} \leq$ 50 mV
DE2 Communications						
Baud Rate	BAUD	—	9600	—	bps	
Power-up Delay	PU_DELAY	—	1	—	ms	Time from rising $V_{DD} \geq$ 6V to DE2 active **(Note 2)**
DE2 Sink Current	$DE2_{iSINK}$	1	—	—	mA	$V_{DE2} \leq$ 50 mV **(Note 2)**
DE2 Message Response Time	$DE2_{RSP}$	0	—	—	µs	Time from last received Stop bit to response Start bit **(Note 2)**
DE2 Host Wait Time	$DE2_{WAIT}$	3.125	—	—	ms	Minimum time for host to wait for response; three packets based on 9600 baud **(Note 2)**
DE2 Message Receive Time-out	$DE2_{RCVTOUT}$	—	5	—	ms	Time between message bytes
INTERNAL ROM (READ-ONLY MEMORY) DATA RETENTION						
Cell High-Temperature Operating Life	HTOL	—	1000	—	Hours	T_J = +150°C **(Note 1)**
Cell Operating Life		—	10	—	Years	T_J = +85°C

Note 1: 1000 hour cumulative maximum for ROM data retention (typical).

2: Limits are ensured by design and characterization, not production tested.

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TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges (Note 1)						
Specified Temperature Range	T_A	-40	—	+150	°C	
Operating Temperature Range	T_A	-40	—	+150	°C	
	T_J	-40	—	+160	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	**(Note 2)**
Package Thermal Resistances						
Thermal Resistance, 5 mm x 5 mm 40-Lead QFN	θ_{JA}	—	37	—	°C/W	4-Layer JC51-5 standard board natural convection
	θ_{JC}	—	6.9	—		
Thermal Resistance, 7 mm x 7 mm 48-Lead TQFP with Exposed Pad	θ_{JA}	—	30	—	°C/W	
	θ_{JC}	—	15	—		

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +160°C rating. Sustained junction temperatures above +160°C can impact the device reliability.

2: 1000 hour cumulative maximum for ROM data retention (typical).

ESD, SUSCEPTIBILITY, SURGE AND LATCH-UP TESTING

Parameter	Standard and Test Condition	Value
Input Voltage Surges	ISO 16750-2	28V for 1 minute, 45V for 0.5 seconds
ESD according to IBEE LIN EMC – Pins LIN_BUS, V_{DD} (HMM)	Test Specification 1.0 following IEC 61000-4.2	±8 kV **(Note 1)**
ESD HBM with 1.5 kΩ/100 pF	CEI/IEC 60749-26: 2006, JEDEC JS-001-2012	±2 kV
ESD HBM with 1.5 kΩ/100 pF – Pins LIN_BUS, V_{DD}, HV_IN1 against PGND	CEI/IEC 60749-26: 2006, JEDEC JS-001-2012	±8 kV
ESD CDM (Charged Device Model) Field-Induced Method – Replaces Machine Model Method	ESD-STM5.3.1-1999	±750V all pins
Latch-up Susceptibility	JEDEC JESD78	

Note 1: With LIN ESD protection diode.

NOTES:

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2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

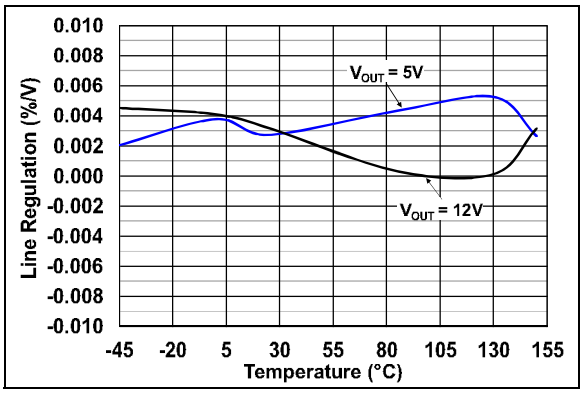

FIGURE 2-1: *LDO Line Regulation vs. Temperature.*

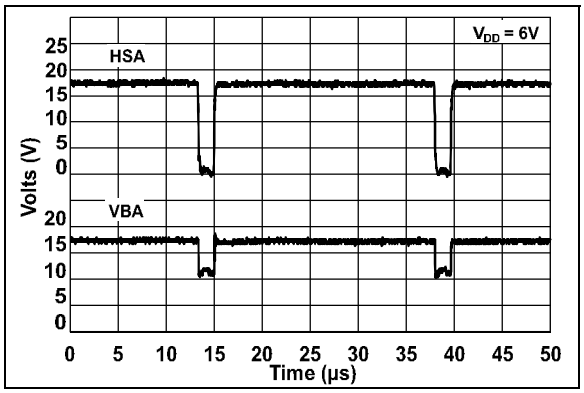

FIGURE 2-4: *Bootstrap Voltage at 92% Duty Cycle.*

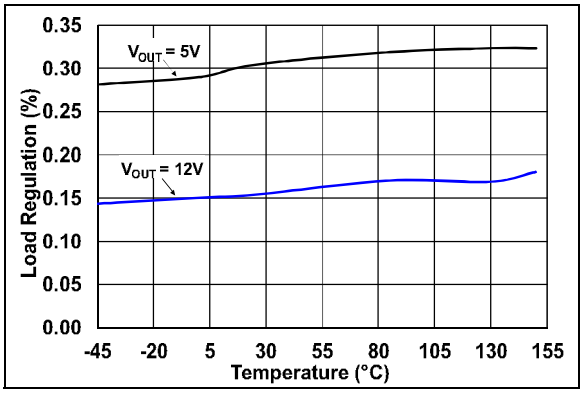

FIGURE 2-2: *LDO Load Regulation vs. Temperature.*

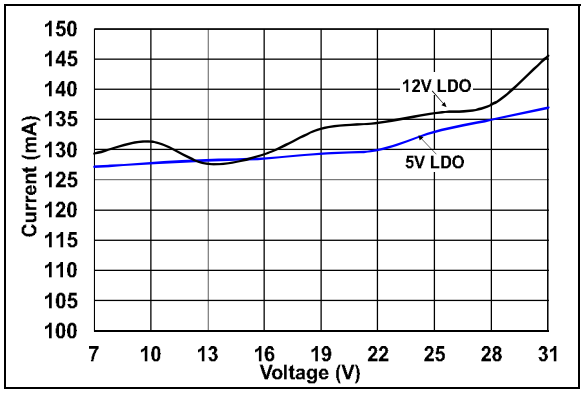

FIGURE 2-5: *LDO Short-Circuit Current vs. Input Voltage.*

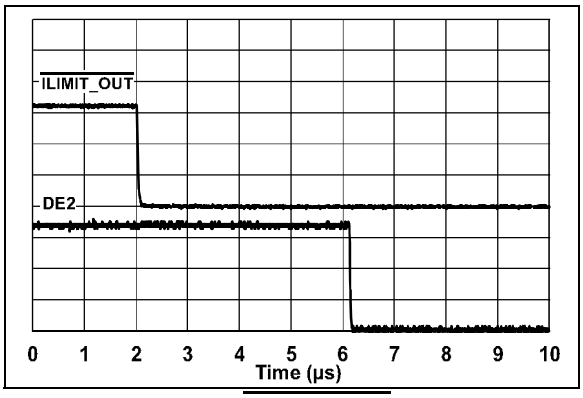

FIGURE 2-3: *$\overline{ILIMIT_OUT}$ Low to DE2 Message Delay.*

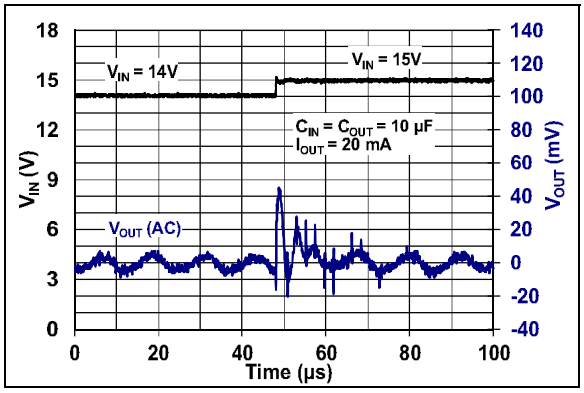

FIGURE 2-6: *5V LDO Dynamic Line Step – Rising V_{DD}.*

Note: Unless otherwise indicated, T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

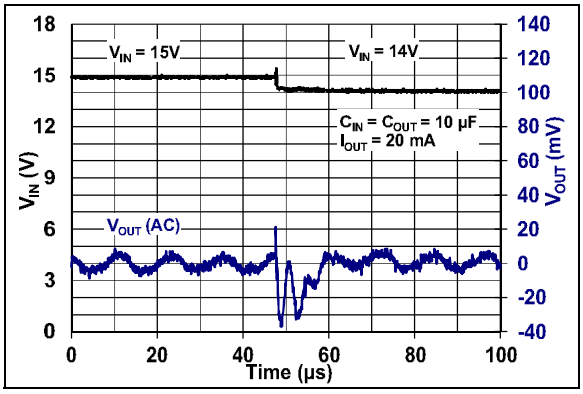

FIGURE 2-7: *5V LDO Dynamic Line Step – Falling V_{DD}.*

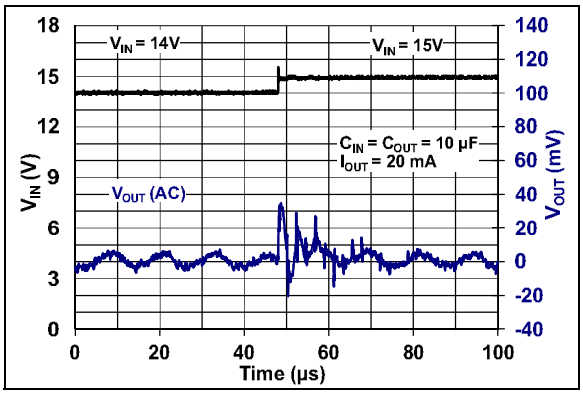

FIGURE 2-8: *12V LDO Dynamic Line Step – Rising V_{DD}.*

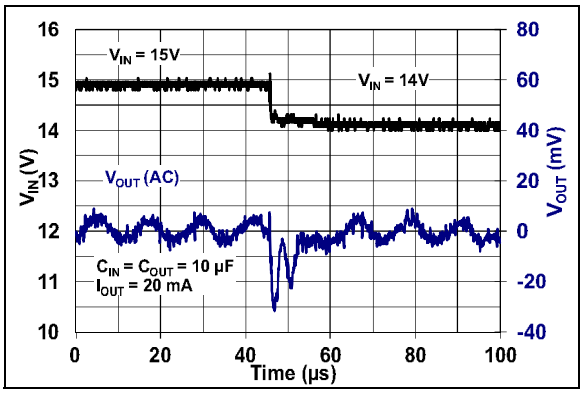

FIGURE 2-9: *12V LDO Dynamic Line Step – Falling V_{DD}.*

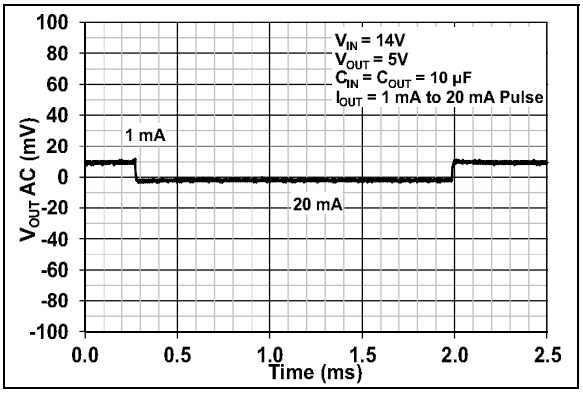

FIGURE 2-10: *5V LDO Dynamic Load Step.*

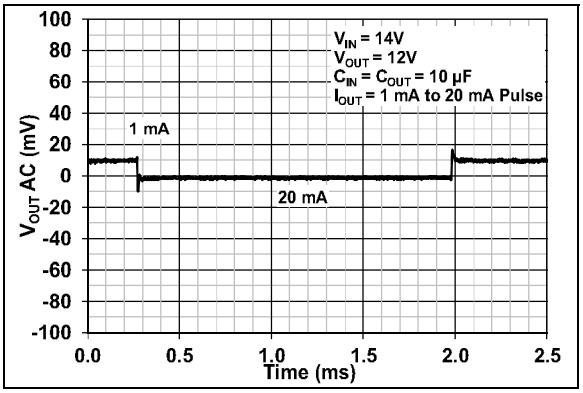

FIGURE 2-11: *12V LDO Dynamic Load Step.*

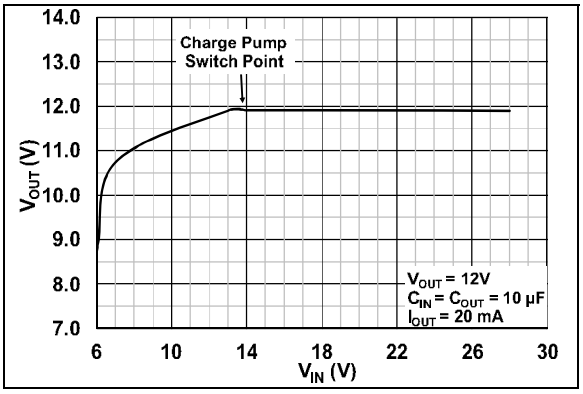

FIGURE 2-12: *12V LDO Output Voltage vs. Rising Input Voltage.*

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Note: Unless otherwise indicated, T_A = +25°C; Junction Temperature (T_J) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in junction temperature over the ambient temperature is not significant.

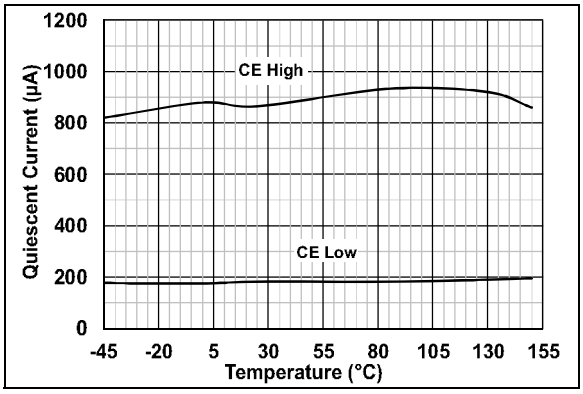

FIGURE 2-13: *Quiescent Current vs. Temperature* ***(MCP8025A)****.*

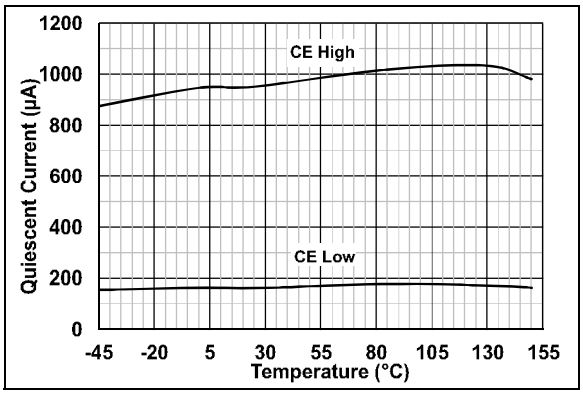

FIGURE 2-14: *Quiescent Current vs. Temperature* ***(MCP8026)****.*

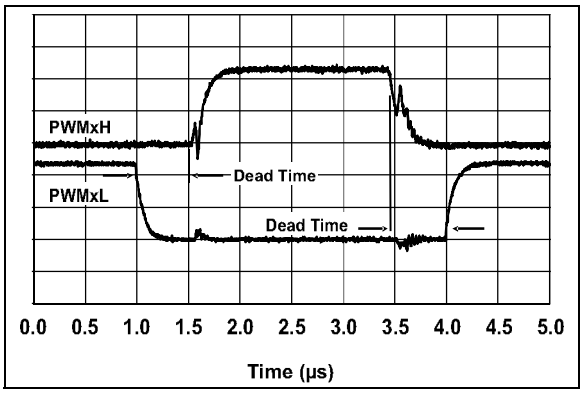

FIGURE 2-15: *500 ns PWM Dead-Time Injection.*

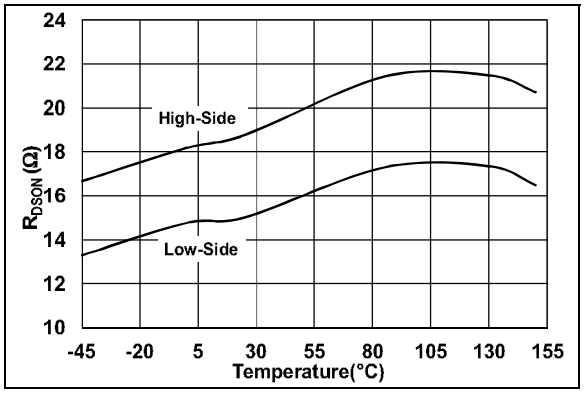

FIGURE 2-16: *Driver R_{DSON} vs. Temperature.*

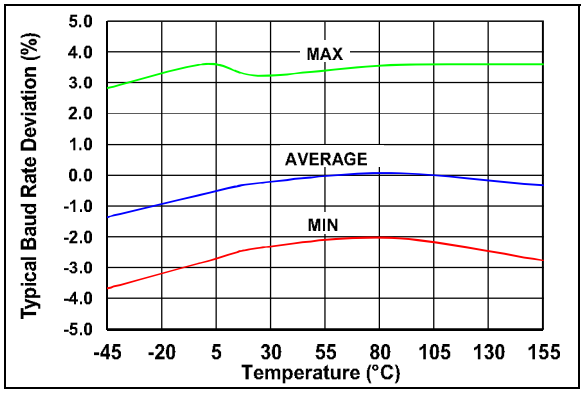

FIGURE 2-17: *Typical Baud Rate Deviation.*

NOTES:

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Tables 3-1 and 3-2.

TABLE 3-1: MCP8025A – PIN FUNCTION TABLE

QFN	TQFP	Symbol	I/O	Description
2	1	PWM1L	I	Digital input, Phase A low-side control, 47 kΩ pull-down
3	2	PWM1H	I	Digital input, Phase A high-side control, 47 kΩ pull-down
4	3	CE	I	Digital input, device enable, 47 kΩ pull-down
—	4	NC	—	No connection
—	5	NC	—	No connection
5	6	LIN_BUS	I/O	LIN bus physical layer
—	7	PGND	Power	Power 0V reference
6	8	RX	O	LIN bus receive data, open-drain
7	9	TX	I	LIN bus transmit data
8	10	$\overline{\text{FAULTn}}$/TXE	I/O	LIN transceiver Fault and transmit enable
9	11	MUX1	I	Digital input back EMF sampler phase multiplexer control, 47 kΩ pull-down
10	12	MUX2	I	Digital input back EMF sampler phase multiplexer control, 47 kΩ pull-down
11	13	ZC_OUT	O	Back EMF sampler comparator output, open-drain
12	14	COMP_REF	I	Back EMF sampler comparator reference
13	15	$\overline{\text{ILIMIT_OUT}}$	O	Current limit comparator, MOSFET driver Fault output, open-drain
14	16	I_OUT1	O	Motor current sense amplifier output
15	17	ISENSE1-	I	Motor current sense amplifier inverting input
16	18	ISENSE1+	I	Motor current sense amplifier noninverting input
17	19,20	PGND	Power	Power 0V reference
18	21	LSA	O	Phase A low-side N-channel MOSFET driver, active-high
19	22	LSB	O	Phase B low-side N-channel MOSFET driver, active-high
20	23	LSC	O	Phase C low-side N-channel MOSFET driver, active-high
—	24	PGND	Power	Power 0V reference
21	25	HSC	O	Phase C high-side N-channel MOSFET driver, active-high
22	26	HSB	O	Phase B high-side N-channel MOSFET driver, active-high
23	27	HSA	O	Phase A high-side N-channel MOSFET driver, active-high
24	28	PHC	I/O	Phase C high-side MOSFET driver reference, back EMF sense input
25	29	PHB	I/O	Phase B high-side MOSFET driver reference, back EMF sense input
26	30	PHA	I/O	Phase A high-side MOSFET driver reference, back EMF sense input
27	31	VBC	Power	Phase C high-side MOSFET driver bias
28	32	VBB	Power	Phase B high-side MOSFET driver bias
29	33	VBA	Power	Phase A high-side MOSFET driver bias
30	34	+12V	Power	Analog circuitry and low-side gate drive bias
—	35, 36	PGND	Power	Power 0V reference
31	37	LX	Power	Buck regulator switch node, external inductor connection
32	38, 39	V_{DD}	Power	Input supply
33	40	FB	I	Buck regulator feedback node
34	41	+5V	Power	Internal circuitry bias
35	42	CAP2	Power	Charge pump flying capacitor input
36	43	CAP1	Power	Charge pump flying capacitor input
37	44	DE2	O	Voltage and temperature supervisor output, open-drain
38	45	PWM3L	I	Digital input, Phase C low-side control, 47 kΩ pull-down
39	46	PWM3H	I	Digital input, Phase C high-side control, 47 kΩ pull-down
40	47	PWM2L	I	Digital input, Phase B low-side control, 47 kΩ pull-down
1	48	PWM2H	I	Digital input, Phase B high-side control, 47 kΩ pull-down
EP	EP	PGND	Power	Exposed Pad; connect to power 0V reference

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TABLE 3-2: MCP8026 – PIN FUNCTION TABLE

QFN	TQFP	Symbol	I/O	Description
2	1	PWM1L	I	Digital input, Phase A low-side control, 47 kΩ pull-down
3	2	PWM1H	I	Digital input, Phase A high-side control, 47 kΩ pull-down
4	3	CE	I	Digital input, device enable, 47 kΩ pull-down
—	4	LV_OUT2	O	Level Translator 2 logic level translated output, open-drain
—	5	HV_IN2	I	Level Translator 2 high-voltage input, 30 kΩ configurable pull-up
5	6	HV_IN1	I	Level Translator 1 high-voltage input, 30 kΩ configurable pull-up
—	7	PGND	Power	Power 0V reference
6	8	LV_OUT1	O	Level Translator 1 logic level translated output, open-drain
7	9	I_OUT3	O	Motor Phase Current Sense Amplifier 3 output
8	10	ISENSE3-	I	Motor Phase Current Sense Amplifier 3 inverting input
9	11	ISENSE3+	I	Motor Phase Current Sense Amplifier 3 noninverting input
10	12	I_OUT2	O	Motor Phase Current Sense Amplifier 2 output
11	13	ISENSE2-	I	Motor Phase Current Sense Amplifier 2 inverting input
12	14	ISENSE2+	I	Motor Phase Current Sense Amplifier 2 noninverting input
13	15	$\overline{\text{ILIMIT_OUT}}$	O	Current limit comparator, MOSFET driver Fault output, open-drain
14	16	I_OUT1	O	Motor Current Sense Amplifier 1 output
15	17	ISENSE1-	I	Motor Current Sense Amplifier 1 inverting input
16	18	ISENSE1+	I	Motor Current Sense Amplifier 1 noninverting input
17	19,20	PGND	Power	Power 0V reference
18	21	LSA	O	Phase A low-side N-channel MOSFET driver, active-high
19	22	LSB	O	Phase B low-side N-channel MOSFET driver, active-high
20	23	LSC	O	Phase C low-side N-channel MOSFET driver, active-high
—	24	PGND	Power	Power 0V reference
21	25	HSC	O	Phase C high-side N-channel MOSFET driver, active-high
22	26	HSB	O	Phase B high-side N-channel MOSFET driver, active-high
23	27	HSA	O	Phase A high-side N-channel MOSFET driver, active-high
24	28	PHC	I/O	Phase C high-side MOSFET driver reference, back EMF sense input
25	29	PHB	I/O	Phase B high-side MOSFET driver reference, back EMF sense input
26	30	PHA	I/O	Phase A high-side MOSFET driver reference, back EMF sense input
27	31	VBC	Power	Phase C high-side MOSFET driver bias
28	32	VBB	Power	Phase B high-side MOSFET driver bias
29	33	VBA	Power	Phase A high-side MOSFET driver bias
30	34	+12V	Power	Analog circuitry and low-side gate drive bias
—	35,36	PGND	Power	Power 0V reference
31	37	LX	Power	Buck regulator switch node, external inductor connection
32	38, 39	V_{DD}	Power	Input supply
33	40	FB	I	Buck regulator feedback node
34	41	+5V	Power	Internal circuitry bias
35	42	CAP2	Power	Charge pump flying capacitor input
36	43	CAP1	Power	Charge pump flying capacitor input
37	44	DE2	O	Voltage and temperature supervisor output, open-drain
38	45	PWM3L	I	Digital input, Phase C low-side control, 47 kΩ pull-down
39	46	PWM3H	I	Digital input, Phase C high-side control, 47 kΩ pull-down
40	47	PWM2L	I	Digital input, Phase B low-side control, 47 kΩ pull-down
1	48	PWM2H	I	Digital input, Phase B high-side control, 47 kΩ pull-down
EP	EP	PGND	Power	Exposed Pad; connect to power 0V reference

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3.1 Low-Side PWM Inputs (PWM1L, PWM2L, PWM3L)

Digital PWM inputs for low-side driver control. Each input has a 47 kΩ pull-down to ground. The PWM signals may contain dead-time timing or the system may use Configuration Register 2 (CFG2) to set the dead time.

3.2 High-Side PWM Inputs (PWM1H, PWM2H, PWM3H)

Digital PWM inputs for high-side driver control. Each input has a 47 kΩ pull-down to ground. The PWM signals may contain dead-time timing or the system may use Configuration Register 2 (CFG2) to set the dead time.

3.3 No Connect (NC)

Reserved. Do not connect.

3.4 Chip Enable Input (CE)

Chip Enable input is used to enable/disable the output driver and on-board functions. When CE is high, all device functions are enabled. When CE is low, the device operates in Standby or Sleep mode. When Standby mode is active, the current amplifiers and the 12V LDO are disabled. The buck regulator, the DE2 pin, and the voltage and temperature sensor functions are not affected. The 5V LDO is disabled on the MCP8026. The H-bridge driver outputs are all set to a low state within 100 ns of CE = 0. The device transitions to Standby or Sleep mode 1 ms after CE = 0.

The CE pin may be used to clear any hardware Faults. When a Fault occurs, the CE input may be used to clear the Fault by setting the pin low and then high again. The Fault is cleared by the rising edge of the CE signal if the hardware Fault is no longer active.

The CE pin is used to enable Sleep mode when the SLEEP bit in the CFG0 Configuration register is set to '1'. CE must be low for a minimum of 1 ms before the transition to Standby or Sleep mode occurs. This allows time for CE to be toggled to clear any Faults without going into Sleep mode.

The CE pin is used to awaken the device from the Sleep mode state. To awaken the device from a Sleep mode state, the CE pin must be set low for a minimum of 250 µs. The device will then wake-up with the next rising edge of the CE pin.

The CE pin has an internal 47 kΩ pull-down.

3.5 Level Translators (HV_IN1, HV_IN2, LV_OUT1, LV_OUT2)

Unidirectional digital level translators. These pins translate the digital input signal on the HV_INx pin to a low-level digital output signal on the LV_OUTx pin. The HV_INx pins have internal 30 kΩ pull-ups to V_{DD} that are controlled by bit PU30K in the CFG0 Configuration register. The PU30K bit is only sampled during CE = 0.

The HV_IN1 pin has higher ESD protection than the HV_IN2 pin. The higher ESD protection makes the HV_IN1 pin better suited for connection to external switches.

LV_OUT1 and LV_OUT2 are open-drain outputs. An external pull-up resistor to the low-voltage logic supply is required.

The HV_IN1 pin may be used to awaken the device from the Sleep mode state. The MCP8026 will awaken on the rising edge of the pin after detecting a low state lasting >250 µs on the pin.

3.6 LIN Transceiver Bus (LIN_BUS)

The bidirectional LIN_BUS interface pin connects to the LIN bus network. The LIN_BUS driver is controlled by the TX pin. The driver is an open-drain output. The MCP8025A device contains a LIN bus 30 kΩ pull-up resistor that may be enabled or disabled by setting the PU30K bit in the CFG0 Configuration register. The pull-up may only be changed while in Standby mode. During normal operation, the 30 kΩ pull-up is always enabled. In Sleep mode, the 30 kΩ pull-up is always disabled.

The LIN bus may be used to awaken the device from the Sleep mode state. When a LIN wake-up event is detected on the LIN_BUS pin, the device will wake-up. The MCP8025A will awaken on the rising edge of the bus after detecting a dominant state lasting >150 µs on the bus. The LIN bus master must provide the dominant state for >250 µs to meet the LIN 2.2A Specifications.

3.7 Power Ground (PGND), Exposed Pad (EP)

Device ground. The PCB ground traces should be short and wide, and should form a star pattern to the power source. The Exposed Pad (EP) must be soldered to the PCB. The PCB area below the EP should be a copper pour with thermal vias to help transfer heat away from the device.

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3.8 LIN Transceiver Received Data Output (RX)

The RX output pin follows the state of the LIN_BUS pin. The data received from the LIN bus is output on the RX pin for connection to a host MCU.

The RX pin is an open-drain output.

3.9 LIN Transceiver Transmit Data Input (TX)

The TX input pin is used to send data to the LIN bus. The LIN_BUS pin is low (dominant) when TXD is low and high (recessive) when TXD is high. Data to be transmitted from a host MCU is sent to the LIN bus via the TX pin.

3.10 LIN Transceiver Fault/ Transmit Enable (FAULTn/TXE)

Fault Detect output and Transmitter Enable input bidirectional pin. The FAULTn/TXE pin will be driven low whenever a LIN Fault occurs. There is a 47 kΩ resistor between the internal Fault signal and the FAULTn/TXE pin to allow the pin to be externally driven high after a Fault has occurred. The FAULTn/TXE pin must be pulsed high to start a transmit. If there is no Fault present when the pin is pulsed, the FAULTn/TXE pin will latch and be driven high by an internal 47 kΩ impedance. The FAULTn/TXE pin may then be monitored for Faults.

No external pull-up is needed. The microcontroller pin controlling the FAULTn/TXE pin must be able to switch between Output and Input modes.

3.11 Zero-Crossing Multiplexer Inputs (MUX1, MUX2)

The MUX1 and MUX2 multiplexer inputs select the desired phase winding to be used as the zero-crossing back EMF phase reference. The output of the multiplexer connects to one input of the zero-crossing comparator. The other zero-crossing comparator input connects to the neutral voltage. The MUX1 and MUX2 inputs must be driven by the host processor synchronously with the motor commutation.

3.12 Zero-Crossing Detector Output (ZC_OUT)

The ZC_OUT output pin is the output of the zero-crossing comparator. When the phase voltage selected by the multiplexer inputs crosses the neutral voltage, the zero-crossing detector will change the output state.

The ZC_OUT output is an open-drain output.

3.13 Neutral Voltage Reference Input (COMP_REF)

The COMP_REF input pin is used to connect to the neutral point of a motor if the neutral point is available. The COMP_REF input may be selected via a Configuration register as the neutral voltage reference used by the zero-crossing comparator.

3.14 Current Limit and Driver Fault Output (ILIMIT_OUT)

Dual purpose output pin. The open-drain output goes low when the current sensed by Current Sense Amplifier 1 exceeds the value set by the internal current reference DAC. The DAC has an offset of 0.991V (typical) that represents the zero current flow.

The open-drain output will also go low while a Fault is active. Table 4-1 shows the Faults that cause the ILIMIT_OUT pin to go low.

The ILIMIT_OUT pin is able to sink 1 mA of current while maintaining less than a 50 mV drop across the output.

3.15 Operational Amplifier Outputs (I_OUT1, I_OUT2, I_OUT3)

Current sense amplifier outputs. May be used with feedback resistors to set the current sense gain. The amplifiers are disabled when CE = 0.

3.16 Operational Amplifier Inputs (ISENSE1+/-, ISENSE2+/-, ISENSE3+/-)

Current sense amplifier inverting and noninverting inputs. Used in conjunction with the I_OUTx pin to set the current sense gain. The amplifiers are disabled when CE = 0.

3.17 Low-Side N-Channel MOSFET Driver Outputs (LSA, LSB, LSC)

Low-side N-channel MOSFET drive signals. Connect to the gate of the external MOSFETs. A low-impedance resistor may be used between these pins and the MOSFET gates to limit current and slew rate.

3.18 High-Side N-Channel MOSFET Driver Outputs (HSA, HSB, HSC)

High-side N-channel MOSFET drive signals. Connect to the gate of the external MOSFETs. A low-impedance resistor may be used between these pins and the MOSFET gates to limit current and slew rate.

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3.19 Driver Phase Inputs (PHA, PHB, PHC)

Phase signals from motor. These signals provide the high-side N-channel MOSFET driver reference and back EMF sense input. The phase signals are also used with the bootstrap capacitors to provide high-side gate drive via the VBx inputs.

3.20 Driver Bootstrap Inputs (VBA, VBB, VBC)

High-side MOSFET driver bias. Connect these pins between the bootstrap charge pump diode cathode and the bootstrap charge pump capacitor. The 12V LDO output is used to provide 12V at the diode anodes. The phase signals are connected to the other side of the bootstrap charge pump capacitors. The bootstrap capacitors charge to 12V when the phase signals are pulled low by the low-side drivers. When the low-side drivers turn off and the high-side drivers turn on, the phase signal is pulled to V_{DD}, causing the bootstrap voltage to rise to V_{DD} + 12V.

3.21 12V LDO (+12V)

+12-volt Low-Dropout (LDO) voltage regulator output. The +12V LDO may be used to power external devices, such as Hall effect sensors or amplifiers. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the +12V pin as is practical. For most applications, 4.7 µF of capacitance will ensure stable operation of the LDO circuit. The +12V LDO is supplied by the internal charge pump when the charge pump is active. When the charge pump is inactive, the +12V LDO is supplied by V_{DD}.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low-ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.22 Buck Regulator Switch Output (LX)

Buck regulator switch node external inductor connection. Connect this pin to the external inductor chosen for the buck regulator.

3.23 Power Supply Input (V_{DD})

Connect V_{DD} to the main supply voltage. This voltage should be the same as the motor voltage. The driver overcurrent and overvoltage shutdown features are relative to the V_{DD} pin. When the V_{DD} voltage is separate from the motor voltage, the overcurrent and overvoltage protection features may not be available.

The V_{DD} voltage must not exceed the maximum operating limits of the device. Connect a bulk capacitor close to this pin for good load step performance and transient protection.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low-ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.24 Buck Regulator Feedback Input (FB)

Buck regulator feedback node that is compared to an internal 1.25V reference voltage. Connect this pin to a resistor divider that sets the buck regulator output voltage. Connecting this pin to a separate +2.5V to +5.5V supply will disable the buck regulator. The FB pin should not be connected to the +5V LDO to disable the buck because the +5V LDO starts after the buck in the internal state machine. The lack of voltage at the FB pin would cause a buck UVLO Fault.

3.25 5V LDO (+5V)

+5-volt Low-Dropout (LDO) voltage regulator output. The +5V LDO may be used to power external devices, such as Hall effect sensors or amplifiers. The +5V LDO is disabled on the MCP8026 when CE = 0. The internal state machine starts the buck regulator before the +5V LDO, so the +5V LDO should not be connected to the buck FB pin to disable the buck regulator. A buck UVLO Fault will occur if the +5V LDO is used to disable the buck regulator. The LDO requires an output capacitor for stability. The positive side of the output capacitor should be physically located as close to the +5V pin as is practical. For most applications, 4.7 µF of capacitance will ensure stable operation of the LDO circuit.

The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low-ESR characteristics of the ceramic will yield better noise and PSRR performance at high frequency.

3.26 Charge Pump Flying Capacitor (CAP1, CAP2)

Charge pump flying capacitor connections. Connect the charge pump capacitor across these two pins. The charge pump flying capacitor supplies the power for the 12V LDO when the charge pump is active.

3.27 Communications Port (DE2)

Open-drain communication node. The DE2 communication is a half-duplex, 9600 baud, 8-bit, no parity communication link. The open-drain DE2 pin must be pulled high by an external pull-up resistor. The pin has a minimum drive capability of 1 mA, resulting in a V_{DE2} of ≤50 mV when driven low.

NOTES:

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4.0 DETAILED DESCRIPTION

4.1 State Diagrams

4.1.1 MCP8025A/6 STATE DIAGRAM

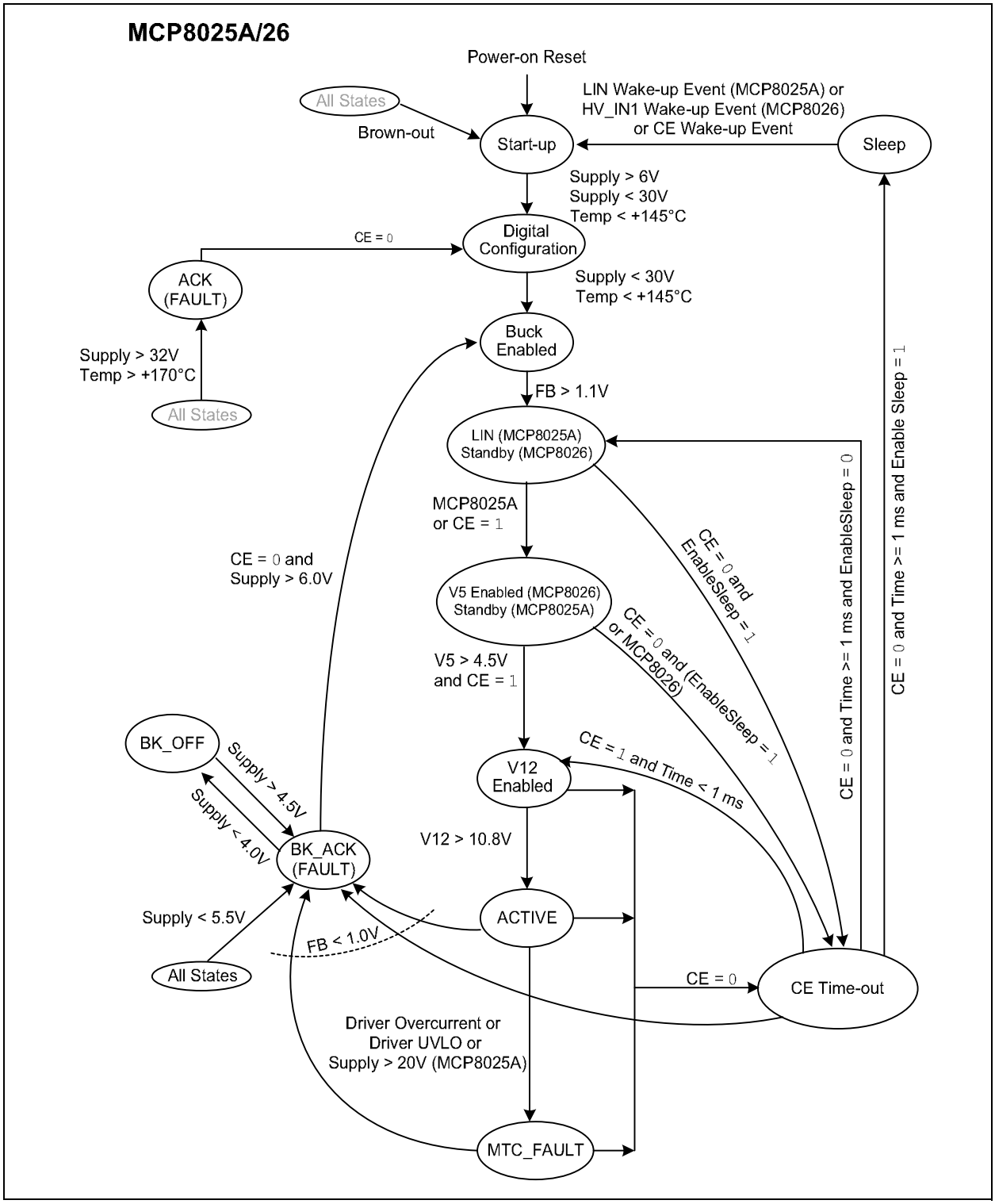

FIGURE 4-1: *MCP8025A/6 State Diagram.*

4.2 Bias Generator

The internal bias generator controls three voltage rails. Two fixed output Low-Dropout linear regulators, an adjustable Buck Switch mode power converter and an unregulated charge pump are controlled through the bias generator. In addition, the bias generator performs supervisory functions.

4.2.1 +12V LOW-DROPOUT LINEAR REGULATOR (LDO)

The +12V rail is used for bias of the 3-phase power MOSFET bridge.

The regulator is capable of supplying 30 mA of external load current. The regulator has a minimum overcurrent limit of 40 mA.

When operating at a supply voltage (V_{DD}) that is in the range of +12V to +12.7V, the +12V charge pump will be off and the +12V source will be the V_{DD} supply voltage. The +12V output may be lower than +12V while operating in the V_{DD} range of +12V to +12.7V, due to the dropout voltage of the regulator.

The Low-Dropout regulators require an output capacitor connected from V_{OUT} to GND to stabilize the internal control loop. A minimum of 4.7 µF ceramic output capacitance is required for the 12V LDO.

The +12V LDO is disabled when the Chip Enable (CE) pin is not active.

Table 4-1 shows the Faults that will also disable the +12V LDO.

4.2.2 +5V LOW-DROPOUT LINEAR REGULATOR (LDO)

The +5V LDO is used for bias of an external micro-controller, the internal current sense amplifier and the gate control logic.

The +5V LDO is capable of supplying 30 mA of external load current. The regulator has a minimum overcurrent limit of 40 mA. If additional external current is required, the Buck Switch mode power converter should be utilized.

A minimum of 4.7 µF ceramic output capacitance is required for the +5V LDO.

The +5V LDO is disabled when the system is in Sleep mode. The +5V LDO is enabled in the MCP8025A and disabled in the MCP8026 when in Standby mode.

Table 4-1 shows the Faults that will also disable the +5V LDO.

4.2.3 BUCK SWITCH MODE POWER SUPPLY (SMPS)

The SMPS is a high-efficiency, fixed frequency, step-down DC-DC converter. The SMPS provides all the active functions for local DC-DC conversion with fast transient response and accurate regulation.

During normal operation of the buck power stage, Q1 is repeatedly switched on and off with the on and off times governed by the control circuit. This switching action causes a train of pulses at the LX node, which are filtered by the L/C output filter to produce a DC output voltage, V_O. Figure 4-2 depicts the functional block diagram of the SMPS.

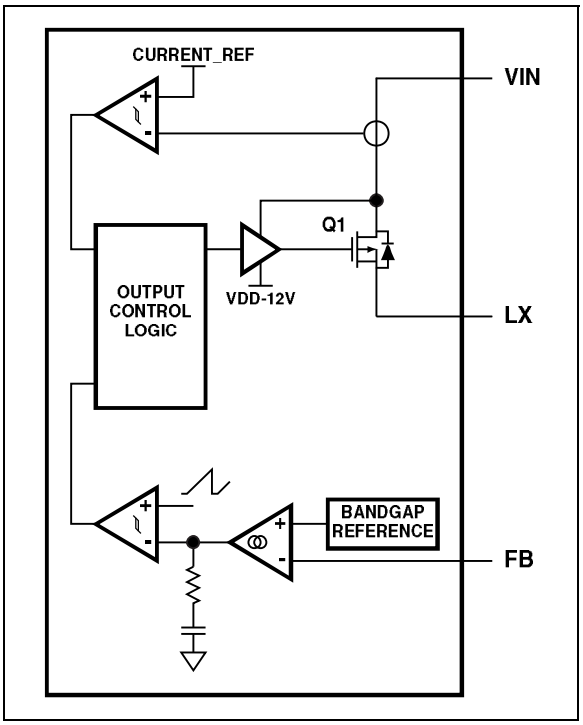

FIGURE 4-2: *SMPS Functional Block Diagram.*

The SMPS is designed to operate in Discontinuous Conduction Mode (DCM) with Voltage mode control and current-limited protection. The SMPS is capable of supplying 750 mW of power to an external load, at a fixed switching frequency of 460 kHz, with an input voltage of 6V. The output of the SMPS is power-limited. For a programmed output voltage of 3V, the SMPS will be capable of supplying 250 mA to an external load. An external diode is required between the LX pin and ground. The diode will be required to handle the inductor current when the switch is off. The diode is external to the device to reduce substrate currents and power dissipation caused by the switcher. The external diode carries the current during the switch-off time, eliminating the current path back through the device.

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The SMPS enters Pulse Frequency Modulation (PFM) mode at light loads, improving efficiency at the expense of higher output voltage ripple. The PFM circuitry provides a means to disable the SMPS as well. If the SMPS is not utilized in the application, connecting the Feedback pin (FB) to an external supply (2.5V to 5.5V) will force the SMPS to a shutdown state.

The maximum inductor value for operation in Discontinuous Conduction mode can be determined by using Equation 4-1.

EQUATION 4-1: L_{MAX} SIMPLIFIED

$$L_{MAX} \leq \frac{V_O \times \left(1 - \frac{V_O}{V_{IN}}\right) \times T}{2 \times I_{O(CRIT)}}$$

Using the L_{MAX} inductor value, calculated using Equation 4-1, will ensure Discontinuous Conduction mode operation for output load currents below the critical current level, $I_{O(CRIT)}$. For example, with an output voltage of +5V, a standard inductor value of 4.7 µH will ensure Discontinuous Conduction mode operation with an input voltage of 6V, a switching frequency of 468 kHz and a critical load current of 150 mA.

The output voltage is set by using a resistor divider network. The resistor divider is connected between the inductor output and ground. The divider common point is connected to the FB pin, which is then compared to an internal 1.25V reference voltage.

The buck regulator will set the BIOCPW bit in the STAT0 register and send a `STATUS_0` message to the host whenever the input switching current exceeds 2.5A peak (typical). The bit will be cleared when the peak input switching current drops back below the 2.5A (typical) limit. This is a warning bit only, no action is taken to shut down the buck operation. The overcurrent limit will shorten the buck duty cycle, and therefore, limit the maximum power out of the buck regulator.

The buck regulator will set the BUVLOW bit in the STAT0 register and send a `STATUS_0` message to the host whenever the output voltage drops below 90% of the rated output voltage. The bit will be cleared when the output voltage returns to 94% of the rated value.

If the buck regulator output voltage falls below 80% of the rated output voltage, the device will shut down with a buck Undervoltage Lockout Fault. The BUVLOF bit in the STAT0 register will be set and a `STATUS_0` message will be sent to the host. The $\overline{\text{ILIMIT_OUT}}$ signal will transition low to indicate the Fault.

The voltage supervisor is designed to shut down the buck regulator when V_{DD} rises above $AOVLO_{STOP}$. When shutting down the buck regulator is not desirable, the user should add a voltage suppression device to the V_{DD} input in order to prevent V_{DD} from rising above $AOVLO_{STOP}$.

The voltage supervisor is also designed to shut down the buck regulator when V_{DD} falls below $UVLO_{BK_STOP}$.

The device will set the BUVLOF bit in the STAT0 register and send a `STATUS_0` message to the host when the buck input voltage drops below $UVLO_{BK_STOP}$.

Table 4-1 shows the Faults that will disable the buck regulator.

4.2.4 CHARGE PUMP

An unregulated charge pump is utilized to boost the input to the +12V LDO during low input conditions. When the input bias to the device (V_{DD}) drops below CP_{START}, the charge pump is activated. When activated, 2 x V_{DD} is presented to the input of the +12V LDO, which maintains a minimum of +10V at its output.

The typical charge pump flying capacitor is a 0.1 µF to 1 µF ceramic capacitor.

4.2.5 SUPERVISOR

The bias generator incorporates a voltage supervisor and a temperature supervisor.

4.2.5.1 Brown-out – Configuration Lost

When the device first powers up or when V_{DD} drops below 3.8V, the Brown-out Reset warning flag bit (BORW) in the STAT1 register will be set. The bit is only a warning indicating that the contents of the Configuration registers may have been compromised by a low supply voltage condition. The host processor should send new configuration information to the device.

4.2.5.2 Voltage Supervisor

The voltage supervisor protects the device, the external power MOSFETs and the external microcontroller from damage caused by overvoltage or undervoltage of the input supply, V_{DD}.

In the event of an undervoltage condition (V_{DD} < +5.5V) or an overvoltage condition of the MCP8025A device (V_{DD} > +20V), the motor drivers are switched off. The bias generator, the communication port and the remainder of the motor control unit remain active. The failure state is flagged on the DE2 pin with a status message. In extreme overvoltage conditions (V_{DD} > +32V), all functions are turned off.

In the event of a severe undervoltage condition (V_{DD} < +4.0V), the buck regulator will be disabled. If the set point of the buck regulator output voltage is above the buck Undervoltage Lockout value, the buck output voltage will decrease as V_{DD} decreases.

4.2.5.3 Temperature Supervisor

An integrated temperature sensor self-protects the device circuitry. If the temperature rises above the overtemperature shutdown threshold, all functions are turned off. Active operation resumes when the temperature has cooled down below a set hysteresis value and the Fault has been cleared by toggling CE.

It is desirable to signal the microcontroller with a warning message before the overtemperature threshold is reached. When the thermal warning temperature set point is exceeded, a warning message will be sent to the host microcontroller. The microcontroller should take appropriate actions to reduce the temperature rise. The method to signal the microcontroller is through the DE2 pin.

4.2.5.4 Internal Function Block Status

Table 4-1 shows the effects of the CE pin, the Faults and the SLEEP bit upon the functional status of the internal blocks of the MCP8025A/6.

TABLE 4-1: INTERNAL FUNCTION BLOCK STATUS

System State	Faults	Conditions	5V LDO	Buck	LIN, HV_IN1, HV_IN2	12V LDO	Motor Drivers	DE2	Internal UVLO, OVLO, OTP
Sleep		CE = 0, SLEEP = 1	—	—	W	—	—	—	—
Standby **(MCP8025A)**		CE = 0, SLEEP = 0	A	A	R	—	—	A	A
Standby **(MCP8026)**		CE = 0, SLEEP = 0	—	A	A	—	—	A	A
Operating		CE = 1, $\overline{\text{ILIMIT_OUT}}$ = 1	A	A	A	A	A	A	A
Faults CE = 1 $\overline{\text{ILIMIT_OUT}}$ = 0	Driver OTP	T_J > +160°C	—	—	—	—	—	A	A
	V_{DD} UVLO	$V_{IN} \leq 5.5V$	—	A	—	—	—	A	A
	Buck Input UVLO	$V_{IN} \leq 4V$	—	—	—	—	—	A	A
	Buck Output Brown-out	V_{BUCK} < 80% (Brown-out)	—	A	—	—	—	A	A
	5V LDO UVLO	$V_{OUT5} \leq 4V$	A	A	R	A	—	A	A
	Driver OVLO **(MCP8025A)**	$V_{IN} \geq 20V$	A	A	A	A	—	A	A
	System OVLO	$V_{IN} \geq 32V$	—	—	—	—	—	A	A
	MOSFET UVLO	$V_{HS[A:C]}$ < 8V, $V_{LS[A:C]}$ < 8V	A	A	A	A	—	A	A
	MOSFET OCP	$V_{Drain\text{-}Source}$ > EXTOC<1:0> Setting	A	A	A	A	—	A	A
Warnings CE = 1 $\overline{\text{ILIMIT_OUT}}$ = 1	Buck OCP	I_{BUCK} Input > 2.5A Peak	A	A	A	A	A	A	A
	Buck Output Undervoltage	V_{BUCK} < 90%	A	A	A	A	A	A	A
	Driver Temperature	T_J > 72% T_{SD_MIN} (+115°C for +160°C Driver OTP)	A	A	A	A	A	A	A
	Configuration Lost (BORW)	Set at Initial Power-up or when V_{DD} < $UVLO_{BK_STOP}$	A	A	A	A	A	A	A

Legend: "A" = Active (On), "—" = Inactive (Off), "W" = Wake-up (from Sleep), "R" = Receiver Only
OCP = Overcurrent Protection
OTP = Overtemperature Protection
UVLO = Undervoltage Lockout
OVLO = Overvoltage Lockout

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4.3 Motor Control Unit

The motor control unit is composed of the following:

- External drive for a 3-phase bridge with NMOS/NMOS MOSFET pairs
- Back EMF sampler with phase multiplexer and neutral simulator **(MCP8025A)**
- Motor current sense amplifier and comparator
- Two additional current sense amplifiers **(MCP8026)**

4.3.1 MOTOR CURRENT SENSE CIRCUITRY

The internal motor current sense circuitry consists of an operational amplifier and a comparator. The amplifier output is presented to the inverting comparator input and as an output to the microcontroller. The noninverting comparator input is connected to an internally programmable 8-bit DAC. A selectable motor current limit threshold may be set with a `SET_ILIMIT` message from the host to the MCP8025A/6 via the DE2 communication link. The DACREF<7:0> bits in the CFG1 register contain the DAC current reference value. The dual purpose $\overline{\text{ILIMIT_OUT}}$ pin handles the current limit output as well as system Fault outputs. The 8-bit DAC is powered by the 5V supply. The DAC output voltage ranges from 0.991V to 4.503V. The DAC has a bit value of $(4.503V - 0.991V)/(2^8 - 1) = 13.77$ mV/bit. A DAC input of 00H yields a DAC output voltage of 0.991V. The default power-up DAC value is 40H (1.872V). The DAC uses a 100 kHz filter. Input code to output voltage delay is approximately five time constants ≈ 50 µs. The desired current sense gain is established with an external resistor network.

> **Note:** The motor current limit comparator output is internally OR'd with the driver Fault output of the driver logic block. The microcontroller should monitor the comparator output and take appropriate actions. The motor current limit comparator circuitry does not disable the motor drivers when an overcurrent situation occurs. Only one current limit comparator is provided. The MCP8026 provides three current sense amplifiers, which can be used for implementation of advanced control algorithms, such as Field-Oriented Control (FOC).

The comparator output may be employed as a current limit. Alternatively, the current sense output can be employed in a chop-chop PWM speed loop for any situation where the motor is being accelerated, either positively or negatively. An analog chop-chop speed loop can be implemented by hysteretic control or fixed off-time of the motor current. This makes for a very robust controller, as the motor current is always in instantaneous control.

A sense resistor in series with the bridge ground return provides a current signal for both feedback and current limiting. This resistor should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impractical to eliminate, careful layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low-ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values and serve double duty as the half-bridge bypass capacitors.

> **Note:** With a chop-chop control, motor current always flows through the sense resistor. When the PWM is off, however, the flyback diodes or synchronous rectifiers conduct, causing the current to reverse polarity through the sense resistor.

The current sense resistor is chosen to establish the peak current limit threshold, which is typically set 20% higher than the maximum current command level to provide Overcurrent Protection during abnormal conditions. Under normal circumstances with a properly compensated current loop, peak current limit will not be exercised.

The current sense operational amplifier is disabled when CE = `0`.

4.3.2 BACK EMF SAMPLER WITH PHASE MULTIPLEXER AND NEUTRAL SIMULATOR **(MCP8025A)**

The commutation loop of a BLDC motor control is a Phase-Locked Loop (PLL) that locks to the rotor's position. Note that this inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity and the commutation loop locks to the rotor's position to commutate the phases at the correct times.

The back EMF sensor consists of the motor, a back EMF sampler, a phase multiplexer and a neutral simulator.

The Back EMF sampler takes the motor phase voltages and calculates the neutral point of the motor by using Equation 4-2.

EQUATION 4-2: NEUTRAL POINT

$$NEUTRAL = \frac{\Phi A + \Phi B + \Phi C}{3}$$

This allows the microcontroller to compare the back EMF signal to the motor's neutral point without the need to bring out an extra wire on a WYE wound motor. For Delta wound motors, there is no physical neutral to bring out, so this reference point must be calculated in any case.

The back EMF sampler measures the motor phase that is not driven (i.e., if LSA and HSB are on, then Phase A is driven low, Phase B is driven high and Phase C is sampled). The sampled phase provides a back EMF signal that is compared against the neutral of the motor. The sampler is controlled by the microcontroller via the MUX1 and MUX2 input signals.

When the BEMF signal crosses the neutral point, the zero-crossing detector will switch the ZC_OUT signal. The host controller may use this signal as a '30 degrees before commutation' reference point. The host controller must commutate the system after 30 degrees of electrical rotation have occurred. Different motor control scenarios may increase or decrease the commutation point by a few degrees.

Internal filtering capacitors are connected after the phase voltage dividers to help eliminate transients during the zero-crossing detection.

TABLE 4-2: PHASE SAMPLER

MUX		Phase Sampled
MUX2	MUX1	
0	0	Phase A
0	1	Phase B
1	0	Phase C
1	1	Phase C

The neutral simulator may be disabled when access to the motor winding neutral point is available. When disabling the neutral simulator, the motor neutral is connected directly to the COMP_REF pin. The actual motor neutral is then used for zero-crossing detection. The neutral simulator may be disabled via DE2 communications.

4.3.3 MOTOR CONTROL

The commutation loop of a BLDC motor control is a Phase-Locked Loop (PLL) that locks to the rotor's position. Note that this inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. An outer speed loop changes the rotor velocity and the commutation loop locks to the rotor's position to commutate the phases at the correct times.

4.3.3.1 Sensorless Motor Control

Many control algorithms can be implemented with the MCP8025A/6 in conjunction with a microcontroller. The following discussion provides a starting point for implementing the MCP8025A or MCP8026 in a sensorless control application of a 3-phase motor. The motor is driven by energizing two windings at a time and sequencing the windings in a 'six-step per electrical revolution' method. This method leaves one winding unenergized at all times and the voltage (back EMF or BEMF) on that unenergized winding can be monitored to determine the rotor position.

4.3.3.2 Start-up Sequence

When the motor being driven is at rest, the BEMF voltage is equal to zero. The motor needs to be rotating for the BEMF sensor to lock onto the rotor position and commutate the motor. The recommended start-up sequence is to bring the rotor from rest up to a speed fast enough to allow BEMF sensing. Motor operation is comprised of five modes: Disabled mode, Bootstrap mode, Lock or Align mode, Ramp mode and Run mode. Refer to the commutation state machine in Table 4-3. The order in which the microcontroller steps through the commutation state machine determines the direction the motor rotates.

4.3.3.2.3 Disabled Mode (CE = 0)

When the driver is disabled (CE = 0), all of the MOSFET driver outputs are set low.

4.3.3.2.4 Bootstrap Mode

The high-side driver obtains the high-side biasing voltage from the +12V LDO, the bootstrap diode and the bootstrap capacitor. The bootstrap capacitors must first be charged before the high-side drives may be used. The bootstrap capacitors are all charged by activating all three low-side drivers. The active low-side drivers pull their respective phase nodes low, charging the bootstrap capacitors to the +12V LDO voltage. The three low-side drivers should be active for at least 1.2 ms per 1 µF of bootstrap capacitance. This assumes a +12V voltage change and 30 mA (10 mA per phase) of current coming from the +12V LDO.

4.3.3.2.5 Lock Mode

Before the motor can be started, the rotor should be in a known position. In Lock mode, the microcontroller drives Phase B low and Phases A and C high. This aligns the rotor 30 electrical degrees before the center of the first commutation state. Lock mode must last long enough to allow the motor and its load to settle into this position.

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4.3.3.2.6 Ramp Mode

At the end of the Lock mode, Ramp mode is entered. In Ramp mode, the microcontroller steps through the commutation state machine, increasing linearly, until a minimum speed is reached. Ramp mode is an open-loop commutation. No knowledge of the rotor position is used.

4.3.3.2.7 Run Mode

At the end of Ramp mode, Run mode is entered. In Run mode, the back EMF sensor is enabled and commutation is now under the control of the Phase-Locked Loop. Motor speed can be regulated by an outer speed control loop.

TABLE 4-3: COMMUTATION STATE MACHINE

State	Outputs						BEMF Phase
	HSA	HSB	HSC	LSA	LSB	LSC	
CE = 0	OFF	OFF	OFF	OFF	OFF	OFF	N/A
BOOTSTRAP	OFF	OFF	OFF	ON	ON	ON	N/A
LOCK	ON	OFF	ON	OFF	ON	OFF	N/A
1	ON	OFF	OFF	OFF	OFF	ON	Phase B
2	OFF	ON	OFF	OFF	OFF	ON	Phase A
3	OFF	ON	OFF	ON	OFF	OFF	Phase C
4	OFF	OFF	ON	ON	OFF	OFF	Phase B
5	OFF	OFF	ON	OFF	ON	OFF	Phase A
6	ON	OFF	OFF	OFF	ON	OFF	Phase C

4.3.3.3 PWM Speed Control

The inner commutation loop is a Phase-Locked Loop, which locks to the rotor's position. This inner loop does not attempt to modify the position of the rotor, but modifies the commutation times to match whatever position the rotor has. The outer speed loop changes the rotor velocity and the inner commutation loop locks to the rotor's position to commutate the phase at the correct times.

The outer speed loop pulse width modulates the motor drive inverter to produce the desired wave shape and voltage at the motor. The inductance of the motor then integrates this Pulse-Width Modulation (PWM) pattern to produce the desired average current, thus controlling the desired torque and speed of the motor. For a trapezoidal BLDC motor drive with six-step commutation, the PWM is used to generate the average voltage to produce the desired motor current and motor speed.

There are two basic methods to Pulse-Width Modulate the inverter switches. The first method returns the reactive energy in the motor inductance to the source by reversing the voltage on the motor winding during the current decay period. This method is referred to as fast decay or chop-chop. The second method circulates the reactive current in the motor with minimal voltage applied to the inductance. This method is referred to as slow decay or chop-coast.

The preferred control method employs a chop-chop PWM for any situation where the motor is being accelerated, either positively or negatively. For improved efficiency, chop-coast PWM is employed during steady-state conditions. The chop-chop speed loop is implemented by hysteretic control, fixed off-time control or average Current-mode control of the motor current. This makes for a very robust controller, as the motor current is always in instantaneous control.

The motor speed presented to the chop-chop loop is reduced by approximately 9%. A fixed frequency PWM that only modulates the high-side switches implements the chop-coast loop. The chop-coast loop is presented with the full motor speed, so if it is able to control the speed, the chop-chop loop will never be satisfied and will remain saturated. The chop-chop remains able to assume full control if the motor torque is exceeded, either through a load change or a change in speed that produces acceleration torque. The chop-coast loop will remain saturated, with the chop-chop loop in full control, during start-up and acceleration to full speed. The bandwidth of the chop-coast loop is set to be slower than the chop-chop loop, so that any transients will be handled by the chop-chop loop and the chop-coast loop will only be active in steady-state operation.

4.3.4 EXTERNAL DRIVE FOR A 3-PHASE BRIDGE WITH NMOS/NMOS MOSFET PAIRS

Each motor phase is driven with external NMOS/NMOS MOSFET pairs. These are controlled by a low-side and a high-side gate driver. The gate drivers are controlled directly by the digital input pins PWM[1:3]H/L. A logic high turns the associated gate driver on and a logic low turns the associated gate driver off. The PWM[1:3]H/L digital inputs are equipped with internal pull-down resistors.

The low-side gate drivers are biased by the +12V LDO output, referenced to ground. The high-side gate drivers are a floating drive biased by a bootstrap capacitor circuit. The bootstrap capacitor is charged by the +12V LDO whenever the accompanying low-side MOSFET is turned on.

The high-side and low-side driver outputs all go to a low state whenever there is a Fault or when CE = `0`, regardless of the PWM[1:3]H/L inputs.

4.3.4.1 MOSFET Driver External Protection Features

Each driver is equipped with Undervoltage Lockout (UVLO) and short-circuit protection features.

4.3.4.1.1 MOSFET Driver Undervoltage Lockout (UVLO)

The MOSFET UVLO Fault detection monitors the available voltage used to drive the external MOSFET gates. The Fault detection is only active while the driver is actively driving the external MOSFET gate. Any time the driver bias voltage is below the Driver Undervoltage Lockout (D_{UVLO}) threshold for a period longer than the one specified by the t_{DUVLO} parameter, the driver will not turn on when commanded, on. A driver Fault will be indicated to the host microcontroller on the $\overline{\text{ILIMIT_OUT}}$ open-drain output pin and also via a DE2 communication `STATUS_1` message. This is a latched Fault. Clearing the Fault requires either removal of device power or disabling and re-enabling the device via the device enable input (CE). The EXTUVLO bit in the CFG0 register is used to enable or disable the Driver Undervoltage Lockout feature. This protection feature prevents the external MOSFETs from being controlled with a gate voltage not suitable to fully enhance the device.

4.3.4.1.2 External MOSFET Short-Circuit Current

Short-circuit protection monitors the voltage across the external MOSFETs during an On condition. The high-side driver voltage is measured from V_{DD} to PH[1:3]. The low-side driver voltage is measured from PH[1:3] to PGND. If the voltage rises above a user-configurable threshold, after the external MOSFET gate voltage has been driven high, all drivers will be turned off. A driver Fault will be indicated to the host microcontroller on the open-drain $\overline{\text{ILIMIT_OUT}}$ output pin and also via a DE2 communication `STATUS_1` message. This is a latched Fault. Clearing the Fault requires either removal of device power or disabling and re-enabling the device via the device enable input (CE). This protection feature helps detect internal motor failures, such as winding to case shorts.

Note:	The driver short-circuit protection is dependent on application parameters. A configuration message is provided for a set number of threshold levels. The MOSFET driver UVLO and short-circuit protection features have the option to be disabled.

The short-circuit voltage may be set via a DE2 `SET_CFG_0` message. The EXTOC<1:0> bits in the CFG0 register are used to select the voltage level for the short-circuit comparison. If the voltage across the MOSFET drain source terminals exceeds the selected voltage level when the MOSFET is active, a Fault will be triggered. The selectable voltage levels are 250 mV, 500 mV, 750 mV and 1000 mV. The EXTSC bit in the CFG0 register is used to enable or disable the MOSFET driver short-circuit detection.

4.3.4.1.3 Fault Pin Output ($\overline{\text{ILIMIT_OUT}}$)

The dual purpose $\overline{\text{ILIMIT_OUT}}$ pin is used as a Fault indicator and as an overcurrent indicator when used with the internal DAC. The pin is capable of sinking a minimum of 1 mA of current while maintaining less than 50 mV of voltage across the output. An external pull-up resistor to the logic supply is required.

The open-drain $\overline{\text{ILIMIT_OUT}}$ pin transitions low when a Fault occurs. Table 4-4 lists the faults that activate the $\overline{\text{ILIMIT_OUT}}$ signal. Warnings do not activate the $\overline{\text{ILIMIT_OUT}}$ signal. Table 4-5 lists the warnings.

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TABLE 4-4: $\overline{\text{ILIMIT_OUT}}$ FAULTS

Fault	DE2 Register
Overtemperature	0x85 0x02
Device Input Undervoltage	0x85 0x04
Driver Input Overvoltage	0x85 0x08
Device Input Overvoltage	0x85 0x10
Buck Regulator Output Undervoltage	0x85 0x80
External MOSFET Undervoltage Lockout	0x86 0x04
External MOSFET Overcurrent Detection	0x86 0x08
5V LDO Undervoltage Lockout	0x86 0x20

TABLE 4-5: WARNINGS

Fault	DE2 Register
Temperature Warning	0x85 0x01
Buck Regulator Overcurrent	0x85 0x20
Buck Regulator Undervoltage	0x85 0x40
Brown-out – Configuration Lost	0x86 0x10

4.3.4.2 Gate Control Logic

The gate control logic provides level shifting of the digital inputs, polarity control and cross-conduction protection.

4.3.4.2.1 Cross-Conduction Protection

Logic prevents switching on one power MOSFET while the opposite one in the same half-bridge is already switched on. If both MOSFETs in the same half-bridge are commanded on simultaneously by the digital inputs, both will be turned off.

4.3.4.2.2 Programmable Dead Time

The gate control logic employs a ‘break-before-make’ dead-time delay that is programmable. A configuration message is provided to configure the driver dead time. The programmable dead times range from 250 ns to 2000 ns (default) in 250 ns increments. The dead time allows the PWM inputs to be direct inversions of each other and still allow proper motor operation. The dead time internally modifies the PWMH/L gate drive timing to prevent cross-conduction. The DRVDT<2:0> bits in the CFG2 register are used to set the dead-time value.

4.3.4.2.3 Programmable Blanking Time

A configuration message is provided to configure the driver current limit blanking time. The blanking time allows the system to ignore any current spikes that may occur when switching the driver outputs. The allowable blanking times are 500 ns, 1 µs, 2 µs and 4 µs (default). The blanking time will start after the dead-time circuitry has timed out. The DRVBT<1:0> bits in the CFG2 register are used to set the blanking time value.

The blanking time affects the driver Undervoltage Lockout. The driver Undervoltage Lockout latches the external MOSFET Undervoltage Lockout Fault if the undervoltage condition lasts longer than the time specified by the t_{DUVLO} parameter. The t_{DUVLO} parameter takes into account the blanking time if blanking is in progress.

4.4 Chip Enable (CE)

The Chip Enable (CE) pin allows the device to be disabled by external control. The Chip Enable pin has four modes of operation.

4.4.1 FAULT CLEARING STATE

The CE pin is used to clear any Faults and re-enable the driver. After toggling the CE pin low-to-high, the system requires a minimum time period to re-enable and start up all the driver blocks. The start-up time is approximately 35 µs. The maximum pulse time for the high-low-high transition to clear Faults should be less than 1 ms. If the high-low-high transition is longer than 1 ms, the device will start up from the Standby state.

Any Fault status bits that are set will be cleared by the low-to-high transition of the CE pin if, and only if, the Fault condition has ceased to exist. If the Fault condition still exists, the active Fault status bit will remain active. No additional Fault messages will be sent for a Fault that remains active.

4.4.2 WAKE FROM SLEEP MODE

The CE pin is also used to awaken the device from the Sleep mode state. To wake the device from a Sleep mode state, the CE pin must be set low for a minimum of 250 µs. The device will then wake-up with the next rising edge of the CE pin.

The LIN bus may be used to wake the device from the Sleep mode state. When a LIN wake-up event is detected on the LIN_BUS pin, the device will wake-up. The MCP8025A will wake-up on the rising edge of the bus after detecting a dominate state lasting >150 µs on the bus. The LIN bus master must provide the dominate state for >250 µs to meet the LIN 2.2A Specifications.

The HV_IN1 pin may be used to wake the device from the Sleep mode state. The MCP8026 will wake-up on the rising edge of the pin after detecting a low state, lasting >250 µs on the pin.

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4.4.3 STANDBY STATE

Standby state is entered when the CE pin goes low for longer than 1 ms and the Sleep Configuration bit is inactive. When Standby mode is entered, the following subsystems are disabled:

- High-side gate drives (HSA, HSB, HSC), forced low
- Low-side gate drives (LSA, LSB, LSC), forced low
- +12V LDO
- +5V LDO **(MCP8026)**
- The 30 kΩ pull-up resistor connected to the level translator is switched out of the circuit to minimize current consumption (configurable) **(MCP8026)**
- The 30 kΩ pull-up resistor connected to the LIN bus is switched out of the circuit to minimize current consumption (configurable) **(MCP8025A)**

The buck regulator stays enabled. The DE2 communication port remains active but the port may only respond to commands. When CE is inactive, the DE2 port is prevented from initiating communications in order to conserve power.

The total current consumption of the device, when CE is inactive (device disabled), stays within the Standby mode input quiescent current limits specified in the **"AC/DC Characteristics"** table.

4.4.4 SLEEP MODE

Sleep mode is entered when both a `SLEEP` command is sent to the device via DE2 communication and the CE pin is low. The two conditions may occur in any order. The transition to Sleep mode occurs after the last of the two conditions occurs and the t_{SLEEP} delay time has elapsed. The SLEEP bit in the CFG0 Configuration register indicates when the device should transition to a low-power mode. The device will operate normally until the CE pin is transitioned low by an external device. At that point in time, the SLEEP bit value determines whether the device transitions to Standby mode or low-power Sleep mode. The quiescent current during Sleep mode will typically be 5 µA. When Sleep mode is activated, most functions will be shut off, including the buck regulator. Only the Power-on Reset (POR) monitor, the voltage translators and the minimal state machine will remain active to detect a wake-up event. This indicates that the host processor will be shut down if the host is using the buck regulator for power. The device will stay in the low-power Sleep mode until either of the following conditions is met:

- The CE pin is toggled low for a minimum of 250 µs and then transitioned high
- The LIN_BUS pin receives a LIN wake-up event; the wake-up event must last at least 250 µs, per LIN Standard 2.2A **(MCP8025A)**
- The HV_IN1 pin transitions high after being in a low state lasting longer than 250 µs **(MCP8026)**

The MCP8025A/6 devices are not required to retain configuration data while in Sleep mode. Sleep mode will set the BORW bit. When exiting Sleep mode, the host should send a new configuration message to configure the device if the default configuration values are not desired. The same configuration sequence used during power-up may be used when exiting Sleep mode. Sleep mode will not be entered if there is a Fault active that will affect the buck regulator output voltage. This prevents a transition to Sleep mode when the host is powered by the buck regulator and the regulator is in an unreliable state.

4.5 Communication Ports

The communication ports provide a means of communicating to the host system.

4.5.1 LIN BUS TRANSCEIVER (MCP8025A)

The MCP8025A provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for industrial applications with serial bus speeds up to 20 kilobaud. The MCP8025A provides a half-duplex, bidirectional communication interface between a microcontroller and the serial network bus. This device will translate the CMOS/TTL logic levels to LIN-level logic and vice versa.

The LIN bus transceiver circuit provides a LIN bus-compliant interface between the LIN bus and a LIN-capable UART on an external microcontroller. The LIN bus transceiver is load dump protected and conforms to LIN 2.1.

4.5.1.1 LIN Wake-up

A LIN wake-up event may be used to wake-up the MCP8025A from Sleep mode. The MCP8025A will wake-up on the rising edge of the LIN bus after detecting a dominate state lasting >150 µs on the LIN_BUS pin. The LIN bus master must provide the dominate state for >250 µs to meet the LIN 2.2A and SAE J2602.

4.5.1.2 $\overline{\text{FAULT}}$/TXE (MCP8025A)

The $\overline{\text{FAULT}}$/TXE pin is a bidirectional open-drain output pin. The state of the pin is defined in Table 4-6. Whenever the $\overline{\text{FAULT}}$/TXE signal is low, the LIN transmitter is off. The transmitter may be re-enabled whenever the $\overline{\text{FAULT}}$/TXE signal returns high, either by removing the internal Fault condition or by the host returning the $\overline{\text{FAULT}}$/TXE high. The $\overline{\text{FAULT}}$/TXE will go low when there is a mismatch between the TX input and the LIN_BUS level. This may be used to detect a bus contention.

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The $\overline{\text{FAULT}}$/TXE pin will go low whenever the internal circuits have detected a short circuit and have disabled the LIN_BUS output driver. The MCP8025A limits the transmitter current to less than 200 mA when a short circuit is detected. If the host MCU is driving the $\overline{\text{FAULT}}$/TXE pin high, then the transmitter will remain enabled and the Fault condition will be overruled. If the host MCU is driving the pin low or is in high-Z mode, the MCP8025A will drive the pin low and will disable the LIN transmitter.

4.5.1.3 LIN Dominant State Time-out

The MCP8025A has an additional LIN feature, LIN Dominant State Time-out, that is not in the current LIN 2.0 Specification. If the LIN TX pin is externally held low for more than the time specified by t_{DOM_TOUT}, the MCP8025A will disable the LIN transmitter. The $\overline{\text{FAULT}}$/TXE pin will go low, indicating a LIN Dominant State Time-out Fault. Forcing the $\overline{\text{FAULT}}$/TXE pin high will not re-enable the transmitter. The transmitter will stay disabled until the TX pin is set high again. This prevents the LIN transceiver from inadvertently locking up the bus.

TABLE 4-6: $\overline{\text{FAULT}}$/TXE TRUTH TABLE

TX In	RX Out	LIN_BUS I/O	$\overline{\text{FAULT}}$/TXE		Definition
			External Input	Driven Output	
L	H	V_{DD}	high-Z	L	**FAULT**, TX driven low, LIN_BUS shorted to V_{DD} (**Note 1**)
L	H	V_{DD}	H	L	**FAULT**, overridden by CPU driving $\overline{\text{FAULT}}$/TXE high
H	H	V_{DD}	high-Z, H	H	**OK**
H	L	GND	high-Z, H	H	**OK**, data is being received from the LIN_BUS
L	L	GND	high-Z, H	H	**OK**
L	L	GND → V_{DD}	high-Z, H	L	**FAULT**, if TX is low longer than t_{DOM_TOUT}
x	x	V_{DD}	L	x	**NO FAULT**, the CPU is commanding the transceiver to turn off the transmitter driver

Legend: x = Irrelevant

Note 1: The $\overline{\text{FAULT}}$/TXE is valid approximately 25 µs after the TXD falling edge. This helps eliminate false Fault reporting during bus propagation delays.

4.5.2 LEVEL TRANSLATOR (MCP8026)

The level translators are an interface between the companion microcontroller's logic levels and the input voltage levels from the system. The level translators are unidirectional translators. Signals on the high-voltage input are translated to low-voltage signals on the low-voltage outputs. The high-voltage HV_IN[1:2] inputs have a configurable 30 kΩ pull-up. The pull-up is configured via a `SET_CFG_0` message. The PU30K bit in the CFG0 register controls the state of the pull-up. The bit may only be changed when the CE pin is low. The low-voltage LV_OUT[1:2] outputs are open-drain outputs. The outputs are capable of sinking a minimum of 1 mA of current while maintaining less than 50 mV at the output.

The HV_IN1 translator is also used to wake-up the device from Sleep mode whenever the HV_IN1 input is transitioned to a low level, for a minimum of 250 µs, followed by a transition to the high-voltage level.

Note:	The TQFP package has two level translators. The second level translator typically interfaces to an ignition key on/off signal.

4.5.3 DE2 COMMUNICATIONS PORT

A half-duplex 9600 baud UART interface is available to communicate with an external host. The port is used to configure the MCP8025A/6 and also for status and Fault messages. The DE2 communication port is described in detail in **Section 4.5.3.1 "Communication Interface"**.

4.5.3.1 Communication Interface

A single-wire, half-duplex, 9600 baud, 8-bit bidirectional communication interface is implemented using the open-drain DE2 pin. The interface consists of eight data bits, one Stop bit and one Start bit. The implementation of the interface is described in the following sections.

The DE2 interface is an open-drain interface. The open-drain output is capable of sinking a minimum of 1 mA of current while maintaining less than 50 mV at the output.

A 5 kΩ resistor should typically be used between the host transmit pin and the MCP8025A/6 DE2 pin to allow the MCP8025A/6 to drive the DE2 line when the host TX pin is at an Idle high level.

The DE2 communication is active when CE = 0 with the constraint that the MCP8025A/6 devices will not initiate any messages. The host processor may initiate messages, regardless of the state of the CE pin, when the device is not in Sleep mode. The MCP8025A/6 devices will respond to host commands when the CE pin is low. The time from receiving the last bit of a command message to sending the first bit of the response message ranges from $DE2_{RSP}$ to $DE2_{WAIT}$, corresponding to 0 µs to 3.125 ms.

4.5.3.2 Packet Format

Every internal status change will provide a communication to the microcontroller. The interface uses a standard UART baud rate of 9600 bits per second.

In the DE2 protocol, the transmitter and the receiver do not share a clock signal. A clock signal does not emanate from one transmitter to the other receiver. Due to this reason, the protocol is asynchronous. The protocol uses only one line to communicate, so the transmit/receive packet must be done in Half-Duplex mode. A new transmit message is allowed only when a complete packet has been transmitted.

The host must listen to the DE2 line in order to check for contentions. In case of contention, the host must release the line and wait for at least three packet length times before initiating a new transfer.

Figure 4-3 illustrates a basic DE2 data packet.

4.5.3.3 Packet Timing

While no data is being transmitted, a logic '1' must be placed on the open-drain DE2 line by an external pull-up resistor. A data packet is composed of one Start bit, which is always a logic '0', followed by eight data bits and a Stop bit. The Stop bit must always be a logic '1'. It takes ten bits to transmit a byte of data.

The device detects the Start bit by detecting the transition from logic '1' to logic '0' (note that while the data line is Idle, the logic level is high). Once the Start bit is detected, the next data bit's "center" can be assured to be 24 ticks minus 2 (worst-case synchronizer uncertainty) later. From then on, every next data bit center is 16 clock ticks later. Figure 4-4 illustrates this point.

4.5.3.4 Message Handling

The driver will not transition to Standby mode or Sleep mode while a message is being received. If a DE2 message is being received or transmitted while the driver is transitioning from Operational mode to either Sleep mode (t_{SLEEP}) or Standby mode ($t_{STANDBY}$), the driver will wait until the ongoing message is completed before changing modes.

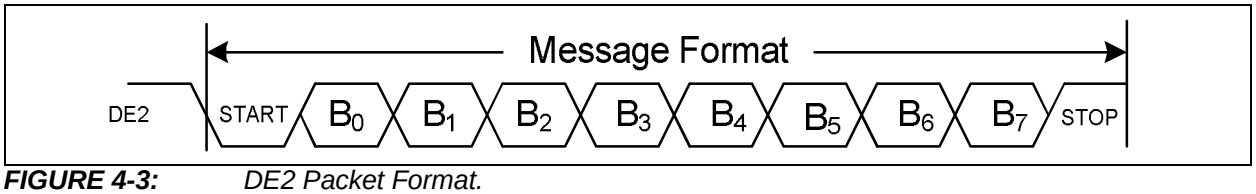

FIGURE 4-3: *DE2 Packet Format.*

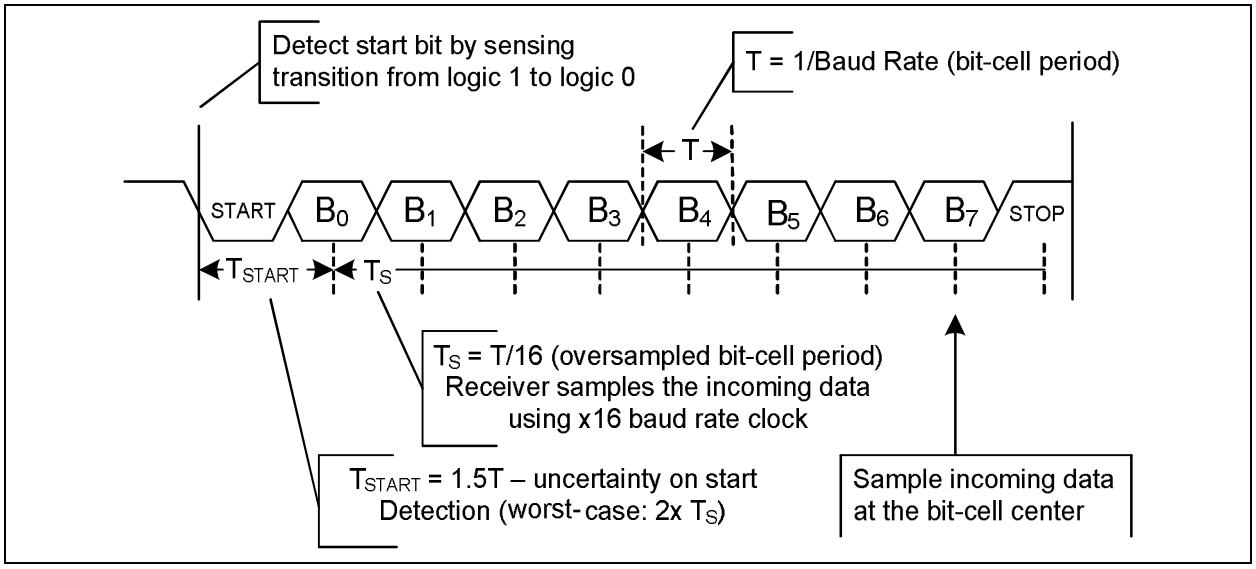

FIGURE 4-4: *DE2 Packet Timing.*

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4.5.4 MESSAGING INTERFACE

A command byte will always have the Most Significant bit 7 (MSb) set to '1'. Bits 6 and 5 are reserved for future use and should be set to '0'. Bits [4:0] are used for commands; that allows for 32 possible commands.

4.5.4.1 Host to MCP8025A/6

Messages sent from the host to the MCP8025A/6 devices consist of either one or two 8-bit bytes. The first byte transmitted is the command byte. The second byte transmitted, if required, is the data for the command.

If a multibyte command is sent to the MCP8025A/6 devices and no second byte is received by the MCP8025A/6 devices, then a 'Not Acknowledged' (NACK) message will be sent back to the host after a 5 ms time-out period.

4.5.4.2 MCP8025A/6 to Host

A solicited response byte from the MCP8025A/6 devices will always echo the command byte with bit 7 set to '0' (Response) and with bit 6 set to '1' for 'Acknowledged' (ACK) or '0' for 'Not Acknowledged' (NACK). The second byte, if required, will be the data for the host command. Any command that causes an error or is not supported will receive a NACK response.

The MCP8025A/6 devices may send unsolicited command messages to the host controller. No message to the host controller requires a response from the host controller.

4.5.5 MESSAGES

4.5.5.1 SET_CFG_0

The SET_CFG_0 message is sent by the host to the MCP8025A/6 devices to configure the devices. The SET_CFG_0 message may be sent to the device at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_0 message. The SET_CFG_0 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

4.5.5.2 GET_CFG_0

The GET_CFG_0 message is sent by the host to the MCP8025A/6 devices to retrieve the device Configuration register. The GET_CFG_0 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

4.5.5.3 STATUS_0 and STATUS_1

STATUS_0 and STATUS_1 messages are sent by the host to the MCP8025A/6 devices to retrieve the device STAT0 or STAT1 register. Unsolicited STATUS_0 and STATUS_1 messages may also be sent to the host by the MCP8025A/6 devices to inform the host of status changes. The unsolicited STATUS_0 and STATUS_1 messages will only be sent when a status bit changes to an active state. The STATUS_0 and STATUS_1 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

When a STATUS_0 and STATUS_1 message is sent to the host in response to a new Fault becoming active, the Fault bit will be cleared, either by the host issuing a STATUS_0 and STATUS_1 request message or by the host toggling the CE pin low, then high. The Fault bit will stay active and not be cleared if the Fault condition still exists at the time the host attempted to clear the Fault.

The BORW bit in the STAT1 register will be set every time the device restarts due to a brown-out event, a Sleep mode wake-up or a normal power-up. When the bit is set, a single unsolicited message will be sent to the host indicating a voltage brown-out or power-up has taken place and that the configuration data may have been lost. The flag is reset by a 'STATUS_1 ACK' (01000110 (46H)) from the device in response to a host status request command.

4.5.5.4 SET_CFG_1

The SET_CFG_1 message is sent by the host to the MCP8025A/6 devices to configure the motor current limit reference DAC. The SET_CFG_1 message may be sent to the device at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_1 message. The SET_CFG_1 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

4.5.5.5 GET_CFG_1

The GET_CFG_1 message is sent by the host to the MCP8025A/6 devices to retrieve the motor current limit reference DAC Configuration register. The GET_CFG_1 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

4.5.5.6 SET_CFG_2

The SET_CFG_2 message is sent by the host to the MCP8025A/6 devices to configure the driver current limit blanking time. The SET_CFG_2 message may be sent to the device at any time. The host is responsible for making sure the system is in a state that will not be compromised by sending the SET_CFG_2 message. The SET_CFG_2 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

4.5.5.7 GET_CFG_2

The GET_CFG_2 message is sent by the host to the MCP8025A/6 devices to retrieve the device Configuration Register 2. The GET_CFG_2 message format is indicated in Table 4-7. The response is indicated in Table 4-8.

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TABLE 4-7: DE2 COMMUNICATION COMMANDS TO MCP8025A/6 FROM HOST

Command	Byte	Bit	Value	Description
SET_CFG_0	1		10000001 (81H)	Set Configuration Register 0
	2	7	0	Reserved
		6	–	Always '0' in Sleep mode
			0	Enable Disconnect of 30 kΩ LIN Bus/Level Translator Pull-up when CE = 0 (default)
			1	Disable Disconnect of 30 kΩ LIN Bus/Level Translator Pull-up when CE = 0
		5	0	System Enters Standby mode when CE = 0
			1	System Enters Sleep mode when CE = 0, 30 kΩ LIN Bus/Level Translator Pull-up Disconnect Always Enabled
		4	0	Disable Internal Neutral Simulator (start-up default)
			1	Enable Internal Neutral Simulator
		3	0	Enable MOSFET Undervoltage Lockout (start-up default)
			1	Disable MOSFET Undervoltage Lockout
		2	0	Enable External MOSFET Short-Circuit Detection (start-up default)
			1	Disable External MOSFET Short-Circuit Detection
		1:0	00	Set External MOSFET Overcurrent Limit to 0.250V (Start-up default)
			01	Set External MOSFET Overcurrent Limit to 0.500V
			10	Set External MOSFET Overcurrent Limit to 0.750V
			11	Set External MOSFET Overcurrent Limit to 1.000V
GET_CFG_0	1		10000010 (82H)	Get Configuration Register 0
SET_CFG_1	1		10000011 (83H)	Set Configuration Register 1 DAC Motor Current Limit Reference Voltage
	2	7:0	00H-FFH	Select DAC Current Reference Value (4.503V – 0.991V)/255 = 13.77 mV/bit 00H = 0.991V 40H = 1.872V (40H x 0.1377 mV/bit + 0.991V) (start-up default) FFH = 4.503V (FFH x 0.1377 mV/bit + 0.991V)
GET_CFG_1	1		10000100 (84H)	Get Configuration Register 1 Get DAC Motor Current Limit Reference Voltage
STATUS_0	1		10000101 (85H)	Get STATUS Register 0
STATUS_1	1		10000110 (86H)	Get STATUS Register 1
SET_CFG_2	1		10000111 (87H)	Set Configuration Register 2
	2	7:5	00H	Reserved
		4:2	–	Driver Dead Time (for PWMH/PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	–	Driver Blanking Time (ignore switching current spikes)
			00	4 µs (default)
			01	2 µs
			10	1 µs
			11	500 ns
GET_CFG_2	1		10001000 (88H)	Get Configuration Register 2

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TABLE 4-8: DE2 COMMUNICATION MESSAGES FROM MCP8025A/6 TO HOST

Message	Byte	Bit	Value	Description
SET_CFG_0	1	7:0	00000001 (01H)	Set Configuration Register 0 'Not Acknowledged' (response)
			01000001 (41H)	Set Configuration Register 0 'Acknowledged' (response)
	2	7	0	Reserved
		6	–	Ignored in Sleep mode
			0	Enable Disconnect of 30K LIN Bus/Level Translator Pull-up when CE = 0 (default)
			1	Disable Disconnect of 30K LIN Bus/Level Translator Pull-up when CE = 0
		5	0	System Enters Standby mode when CE = 0
			1	System Enters Sleep mode when CE = 0, 30K LIN Bus/Level Translator Pull-up Disconnect Always Enabled
		4	0	Internal Neutral Simulator Disabled (start-up default)
			1	Internal Neutral Simulator Enabled
		3	0	Undervoltage Lockout Enabled (default)
			1	Undervoltage Lockout Disabled
		2	0	External MOSFET Overcurrent Detection Enabled (default)
			1	External MOSFET Overcurrent Detection Disabled
		1:0	00	0.250V External MOSFET Overcurrent Limit (default)
			01	0.500V External MOSFET Overcurrent Limit
			10	0.750V External MOSFET Overcurrent Limit
			11	1.000V External MOSFET Overcurrent Limit
GET_CFG_0	1	7:0	00000010 (02H)	Get Configuration Register 0 'Not Acknowledged' (response)
			01000010 (42H)	Get Configuration Register 0 'Acknowledged' (response)
	2	7	0	Reserved
		6	–	Ignored in Sleep mode
			0	Enable Disconnect of 30K LIN Bus/Level Translator Pull-up when CE = 0 (default)
			1	Disable Disconnect of 30K LIN Bus/Level Translator Pull-up when CE = 0
		5	0	System Enters Standby mode when CE = 0
			1	System Enters Sleep mode when CE = 0, 30K LIN Bus/Level Translator Pull-up Disconnect Always Enabled
		4	0	Internal Neutral Simulator Disabled (start-up default)
			1	Internal Neutral Simulator Enabled
		3	0	Undervoltage Lockout Enabled
			1	Undervoltage Lockout Disabled
		2	0	External MOSFET Overcurrent Detection Enabled
			1	External MOSFET Overcurrent Detection Disabled
		1:0	00	0.250V External MOSFET Overcurrent Limit
			01	0.500V External MOSFET Overcurrent Limit
			10	0.750V External MOSFET Overcurrent Limit
			11	1.000V External MOSFET Overcurrent Limit
SET_CFG_1	1		00000011 (03H)	Set DAC Motor Current Limit Reference Voltage 'Not Acknowledged' (response)
			01000011 (43H)	Set DAC Motor Current Limit Reference Voltage 'Acknowledged' (response)
	2	7:0	00H-FFH	Current DAC Current Reference Value: 13.77 mV/bit + 0.991V
GET_CFG_1	1		00000100 (04H)	Get DAC Motor Current Limit Reference Voltage 'Not Acknowledged' (Response)
			01000100 (44H)	Get DAC Motor Current Limit Reference Voltage 'Acknowledged' (Response)
	2	7:0	00H-FFH	Current DAC Current Reference Value: 13.77 mV/bit + 0.991V

TABLE 4-8: DE2 COMMUNICATION MESSAGES FROM MCP8025A/6 TO HOST (CONTINUED)

Message	Byte	Bit	Value	Description
STATUS_0	1	7:0	00000101 (05H)	STATUS Register 0 'Not Acknowledged' (response)
			01000101 (45H)	STATUS Register 0 'Acknowledged' (response)
			10000101 (85H)	STATUS Register 0 Command to Host (unsolicited)
	2	7:0	00000000	Normal Operation
			00000001	Temperature Warning (T_J > 72% T_{SD_MIN} = +115°C) (default)
			00000010	Overtemperature (T_J > +160°C)
			00000100	Input Undervoltage (V_{DD} < 5.5V)
			00001000	Driver Input Overvoltage (20V < V_{DDH} < 32V)
			00010000	Input Overvoltage (V_{DD} > 32V)
			00100000	Buck Regulator Overcurrent
			01000000	Buck Regulator Output Undervoltage Warning
			10000000	Buck Regulator Output Undervoltage (<80%, brown-out error)
STATUS_1	1	7:0	00000110 (06H)	STATUS Register 1 'Not Acknowledged' (response)
			01000110 (46H)	STATUS Register 1 'Acknowledged' (response)
			10000110 (86H)	STATUS Register 1 Command to Host (unsolicited)
	2	7:0	00000000	Normal Operation
			00000001	Reserved
			00000010	Reserved
			00000100	External MOSFET Undervoltage Lockout (UVLO)
			00001000	External MOSFET Overcurrent Detection
			00010000	Brown-out Reset – Configuration Lost (start-up default = 1)
			00100000	+5V LDO Undervoltage Lockout (UVLO)
			01000000	Reserved
			10000000	Reserved
SET_CFG_2	1		00000111 (07H)	Set Configuration Register 2 'Not Acknowledged' (response)
			01000111 (47H)	Set Configuration Register 2 'Acknowledged' (response)
	2	7:5	00H	Reserved
		4:2	–	Driver Dead Time (for PWMH/PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	–	Driver Blanking Time (ignore switching current spikes)
			00	4 µs (default)
			01	2 µs
			10	1 µs
			11	500 ns

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TABLE 4-8: DE2 COMMUNICATION MESSAGES FROM MCP8025A/6 TO HOST (CONTINUED)

Message	Byte	Bit	Value	Description
GET_CFG_2	1		00001000 (08H)	Get Configuration Register 2 'Not Acknowledged' (response)
			01001000 (48H)	Get Configuration Register 2 'Acknowledged' (response)
	2	7:5	00H	Reserved
		4:2	–	Driver Dead Time (for PWMH/PWML inputs)
			000	2000 ns (default)
			001	1750 ns
			010	1500 ns
			011	1250 ns
			100	1000 ns
			101	750 ns
			110	500 ns
			111	250 ns
		1:0	–	Driver Blanking Time (ignore switching current spikes)
			00	4 µs (default)
			01	2 µs
			10	1 µs
			11	500 ns

4.6 Register Definitions

REGISTER 4-1: CFG0: CONFIGURATION REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PU30K(1)	SLEEP	NEUSIM	EXTUVLO	EXTSC	EXTOC1	EXTOC0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **PU30K:** 30K LIN/Level Translator Pull-up bit(1)
- 1 = Disable disconnect of 30K pull-up when CE = 0
- 0 = Enable disconnect of 30K pull-up when CE = 0

bit 5 **SLEEP:** Sleep Mode bit
- 1 = System enters Sleep mode when CE = 0; disconnect of 30K LIN/level translator pull-up always enabled
- 0 = System enters Standby mode when CE = 0

bit 4 **NEUSIM:** Neutral Simulator bit **(MCP8025A)**
- 1 = Enable internal neutral simulator
- 0 = Disable internal neutral simulator

bit 3 **EXTUVLO:** External MOSFET Undervoltage Lockout bit
- 1 = Disable
- 0 = Enable

bit 2 **EXTSC:** External MOSFET Short-Circuit Detection bit
- 1 = Disable
- 0 = Enable

bit 1-0 **EXTOC<1:0>:** External MOSFET Overcurrent Limit Value bits
- 00 = Overcurrent limit set to 0.250V
- 01 = Overcurrent limit set to 0.500V
- 10 = Overcurrent limit set to 0.750V
- 11 = Overcurrent limit set to 1.000V

Note 1: Bit may only be changed while in Standby mode.

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REGISTER 4-2: CFG1: CONFIGURATION REGISTER 1

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DACREF7	DACREF6	DACREF5	DACREF4	DACREF3	DACREF2	DACREF1	DACREF0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **DACREF<7:0>:** DAC Current Reference Value bits
(4.503V – 0.991V)/255 = 13.77 mV/bit
00H = 0.991V
40H = 1.872V (40H x 0.1377 mV/bit + 0.991V)
FFH = 4.503V (FFH x 0.1377 mV/bit + 0.991V)

REGISTER 4-3: CFG2: CONFIGURATION REGISTER 2

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	DRVDT2	DRVDT1	DRVDT0	DRVBL1	DRVBL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-2 **DRVDT<2:0>:** Driver Dead-Time Selection bits
000 = 2000 ns
001 = 1750 ns
010 = 1500 ns
011 = 1250 ns
100 = 1000 ns
101 = 750 ns
110 = 500 ns
111 = 250 ns

bit 1-0 **DRVB<1:0>:** Driver Blanking Time Selection bits
00 = 4000 ns
01 = 2000 ns
10 = 1000 ns
11 = 500 ns

REGISTER 4-4: STAT0: STATUS REGISTER 0

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
BUVLOF	BUVLOW	BIOCPW	OVLOF	DOVLOF	UVLOF	OTPF	OTPW
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **BUVLOF:** Buck Undervoltage Lockout Fault bit
1 = Buck output voltage is below 80% of expected value
0 = Buck output voltage is above 80% of expected value

bit 6 **BUVLOW:** Buck Undervoltage Lockout Warning bit
1 = Buck output voltage is below 90% of expected value
0 = Buck output voltage is above 90% of expected value

bit 5 **BIOCPW:** Buck Input Overcurrent Protection Warning bit
1 = Buck input current is above 2A peak
0 = Buck input current is below 2A peak

bit 4 **OVLOF:** Input Overvoltage Lockout Fault bit
1 = V_{DD} input voltage > 32V
0 = V_{DD} input voltage < 32V

bit 3 **DOVLOF:** Driver Input Overvoltage Lockout Fault bit (**MCP8025A** only, **MCP8026** = 0)
1 = 20V < V_{DDH}
0 = V_{DD} < 20V

bit 2 **UVLOF:** Input Undervoltage Fault bit
1 = V_{DD} input voltage < 5.5V
0 = V_{DD} input voltage > 5.5V

bit 1 **OTPF:** Overtemperature Protection Fault bit
1 = Device junction temperature is > +160°C
0 = Device junction temperature is < +160°C

bit 0 **OTPW:** Overtemperature Protection Warning bit
1 = Device junction temperature is > +115°C
0 = Device junction temperature is < +115°C

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REGISTER 4-5: STAT1: STATUS REGISTER 1

U-0	U-0	R-0	R-1	R-0	R-0	U-0	U-0
—	—	UVLOF5V	BORW	XOCPF[1]	XUVLOF	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **UVLOF5V:** +5V LDO Undervoltage Lockout bit
1 = +5V LDO output voltage < 4.0V
0 = +5V LDO output voltage > 4.0V

bit 4 **BORW:** Brown-out Reset Warning, Configuration Lost bit
1 = Internal device Reset has occurred since last configuration message
0 = No internal device Reset has occurred since last configuration message

bit 3 **XOCPF:** External MOSFET Overcurrent Protection Fault bit[1]
1 = External MOSFET V_{DS} > CFG0<EXTOC> value
0 = External MOSFET V_{DS} < CFG0<EXTOC> value

bit 2 **XUVLOF:** External MOSFET Gate Drive Undervoltage Fault bit
1 = HS_X output voltage < 8V
0 = HS_X output voltage > 8V

bit 1-0 **Unimplemented:** Read as ‘0’

Note 1: Only valid when CFG0<EXTSC> = 1.

NOTES:

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5.0 APPLICATION INFORMATION

5.1 Component Calculations

5.1.1 CHARGE PUMP CAPACITORS

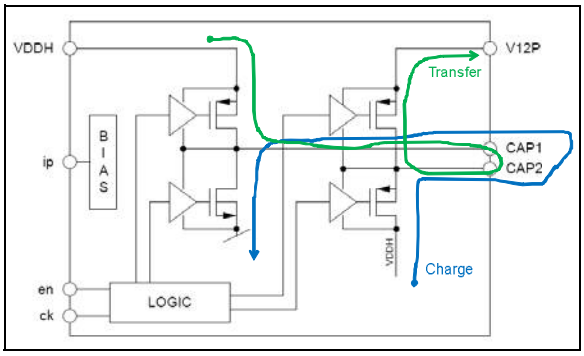

FIGURE 5-1: *Charge Pump.*

Let:

I_{OUT} = 20 mA
f_{CP} = 75 kHz (charge/discharge in one cycle)
50% duty cycle
V_{DDH} = 6V (worst-case)
R_{DSON} = 7.5Ω (R_{PMOS}), 3.5Ω (R_{NMOS})
V12P = 2 x V_{DDH} (ideal)
C_{ESR} = 20 mΩ (ceramic capacitors)
V_{DROP} = 100 mV (V_{OUT} ripple)
T_{CHG} = T_{DCHG} = 0.5 x 1/75 kHz = 6.67 µs

5.1.1.1 Flying Capacitor

The flying capacitor should be chosen to charge to a minimum of 95% (3τ) of V_{DDH}, within one half of a switching cycle.

$3 \times \tau = T_{CHG}$
$\tau = T_{CHG}/3$
$RC = T_{CHG}/3$
$C = T_{CHG}/(R \times 3)$
$C = 6.67\ \mu s/([7.5\Omega + 3.5\Omega + 0.02\Omega] \times 3)$
$C = 202$ nF

Choose a 180 nF capacitor.

5.1.1.2 Charge Pump Output Capacitor

Solve for the charge pump output capacitance, connected between V12P and ground, that will supply the 20 mA load for one switch cycle. The +12V LDO pin on the MCP8025A/6 is the "V12P" pin referenced in the calculations.

$C = I_{OUT} \times dt/dV$
$C = I_{OUT} \times 13.3\ \mu s/(V_{DROP} + I_{OUT} \times C_{ESR})$
$C = 20\ mA \times 13.3\ \mu s/(0.1V + 20\ mA \times 20\ m\Omega)$
$C \geq 2.65\ \mu F$

For stability reasons, the +12V LDO and +5V LDO capacitors must be greater than 4.7 µF, so choose C ≥ 4.7 µF.

5.1.1.3 Charging Path (Flying Capacitor Across CAP1 and CAP2)

$V_{CAP} = V_{DDH}(1 - e^{-T/\tau})$
$V_{CAP} = 6V(1 - e^{-[6.67\ \mu s/([7.5\Omega + 3.5\Omega + 20\ m\Omega] \times 180\ nF)]})$
V_{CAP} = 5.79V available for transfer

5.1.1.4 Transfer Path (Flying and Output Capacitors)

$V12P = V_{DDH} + V_{CAP} - I_{OUT} \times dt/C$
$V12P = 6V + 5.79V - (20\ mA \times 6.67\ \mu s/180\ nF)$
$V12P = 11.049V$

5.1.1.5 Calculate the Flying Capacitor Voltage Drop in One Cycle while Supplying 20 mA

$dV = I_{OUT} \times dt/C$
$dV = 20\ mA \times 6.67\ \mu s/180\ nF$
$dV = 0.741V$ @ 20 mA

The second and subsequent transfer cycles will have a higher voltage available for transfer, since the capacitor is not completely depleted with each cycle. V_{CAP} will then be, $V_{CAP} - dV$, after the first transfer, plus $V_{DDH} - (V_{CAP} - dV)$ times the RC constant. This repeats for each subsequent cycle, allowing a larger charge pump capacitor to be used if the system tolerates several charge transfers before requiring full-output voltage and current.

Repeating the steps in **Section 5.1.1.3 "Charging Path (Flying Capacitor Across CAP1 and CAP2)"** for the second cycle (and subsequent by re-calculating for each new value of V_{CAP} after each transfer):

$V_{CAP} = (V_{CAP} - dV) + (V_{DDH} - (V_{CAP} - dV))(1 - e^{-T/\tau})$
$V_{CAP} = (5.79V - 0.741V) + (6V - (5.79V - 0.741V)) \times (1 - e^{-[6.67\ \mu s/([7.5\Omega + 3.5\Omega + 20\ m\Omega] \times 180\ nF)]})$
$V_{CAP} = 5.049V + 0.951V \times 0.96535$
V_{CAP} = 5.967V available for transfer on second cycle

5.1.1.6 Charge Pump Results

The maximum charge pump flying capacitor value is 202 nF to maintain a 95% voltage transfer ratio on the first charge pump cycle. Larger capacitor values may be used, but they will require more cycles to charge to maximum voltage. The minimum required output capacitor value is 2.65 µF to supply 20 mA for 13.3 µs with a 100 mV drop. A larger output capacitor may be used to cover losses due to capacitor tolerance over temperature, capacitor dielectric and PCB losses.

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These are approximate calculations. The actual voltages may vary due to incomplete charging or discharging of capacitors per cycle due to load changes. The charge pump calculations assume the charge pump is able to charge up the external boot cap within a few cycles.

5.1.2 BOOTSTRAP CAPACITOR

The high-side driver bootstrap capacitor needs to power the high-side driver and gate, for 1/3 of the motor electrical period, for a 3-phase BLDC motor.

Let:

MOSFET Driver Current = 300 mA
PWM Period = 50 µs (20 kHz)
Minimum Duty Cycle = 1% (500 ns)
Maximum Duty Cycle = 99% (49.5 µs)
V_{IN} = 12V
Minimum Gate Drive Voltage = 8V (V_{GS})
Total Gate Charge = 130 nC (80A MOSFET)
Allowable V_{GS} Drop (V_{DROP}) = 3V
Switch R_{DSON} = 100 mΩ
Driver Internal Bias Current = 20 µA (I_{BIAS})

Solve for the smallest capacitance that can supply:

- 130 nC of charge to the MOSFET gate
- 1 MΩ gate source resistor current
- Driver bias current and switching losses

Q_{MOSFET} = 130 nC
$Q_{RESISTOR}$ = [(V_{GS}/R) x T_{ON}]
Q_{DRIVER} = (I_{BIAS} x T_{ON})
T_{ON} = 49.5 µs (99% DC) for worst-case
$Q_{RESISTOR}$ = (12V/1 MΩ) x 49.5 µs
$Q_{RESISTOR}$ = 0.594 nC
Q_{DRIVER} = 20 µA x 49.5 µs
Q_{DRIVER} = 0.99 nC

Sum all of the energy requirements:

C = (Q_{MOSFET} + $Q_{RESISTOR}$ + Q_{DRIVER})/V_{DROP}
C = (130 nC + 0.594 nC + 0.99 nC)/3V
C = 43.86 nF

Choose a bootstrap capacitor value that is larger than 43.86 nF.

5.1.3 BUCK SWITCHER

5.1.3.1 Calculate the Buck Inductor for Discontinuous Mode Operation

Let:

V_{IN} = 4.3V (worst-case is BUVLO)
V_{OUT} = 3.3V
I_{OUT} = 225 mA
f_{SW} = 468 kHz (T_{SW} = 2.137 µs)

Solve for maximum inductance value.

L_{MAX} = V_{OUT} x (1 – V_{OUT}/V_{IN}) x T_{SW}/(2 x I_{OUT})
L_{MAX} = 3.3V x (1 – 3.3V/4.3V) x 2.137 µs/(2 x 225 mA)
L_{MAX} = 3.64 µH

Choose an inductor ≤ 3.64 µH to ensure Discontinuous Conduction mode.

Table 5-1 shows the various maximum inductance values for a worst-case input voltage of 6V and various output voltages.

TABLE 5-1: MAXIMUM INDUCTANCE FOR BUCK DISCONTINUOUS MODE OPERATION

V_{IN} (worst-case)	V_{OUT}	I_{OUT}	Maximum Inductance
4.3V (BUVLO)	3V	250 mA	4.3 µH
4.3V (BUVLO)	3.3V	225 mA	3.6 µH
6V	5V	150 mA	5.9 µH

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5.1.3.2 Determine the Peak Switch Current for the Calculated Inductor

I_{PEAK} = (V_S – V_O) x D x T/L

I_{PEAK} = (4.3V – 3.3V) x (3.3V/4.3V) x 2.137 µs/3.64 µH

I_{PEAK} = 450 mA

5.1.3.3 Setting the Buck Output Voltage

The buck output voltage is set by a resistor voltage divider from the inductor output to ground. The divider center tap is fed back to the MCP8025A FB pin. The FB pin is compared to an internal 1.25V reference voltage. When the FB pin voltage drops below the reference voltage, the buck duty cycle increases. When the FB pin rises above the reference voltage, the buck duty cycle decreases.

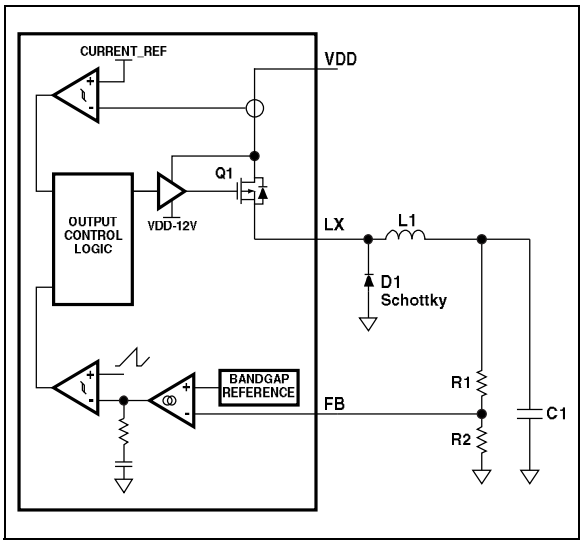

FIGURE 5-2: *Typical Buck Application.*

See **Section 6.7 "Buck Overvoltage"** for resistor value requirements.

V_{BUCK} = 1.25V x (R1 + R2)/R2

5.1.3.4 Start-up Delay for Bootstrap Charging

A start-up delay is required whenever the device has been disabled (CE = `0`) and the bootstrap capacitors have discharged. When the device is re-enabled (CE = `1`), there is a voltage divider between the +12V LDO capacitor and the bootstrap capacitors. To prevent a gate drive Undervoltage Lockout, the +12V LDO capacitor must be sized to prevent the bootstrap capacitors from pulling the 12V supply below the UVLO threshold when the 12V supply is enabled.

Assuming the V12 capacitor is 4.7 µF, V12 LDO is 12V, $C_{BOOTSTRAP}$ = 1 µF, the bootstrap voltage when the 12V supply is first turned on will be:

12V x (4.7 µF/(4.7 µF + 3 bootstrap caps charging x 1 µF)) = 7.32V, which will trip the gate driver UVLO if the low side is turned on at this time.

By sizing the 12V LDO capacitor to prevent the bootstrap voltage from dropping below 8V, the UVLO may be averted.

$V_{BOOTCAP}$ = 12V (Cap12V/(Cap12V + n x $Cap_{BOOTSTRAP}$))

Where 'n' is the number of simultaneous bootstrap caps being charged at the same time.

$V_{BOOTCAP}$/12V = Cap12V/(Cap12V + n x $Cap_{BOOTSTRAP}$)

12V/$V_{BOOTCAP}$ = (Cap12V + n x $Cap_{BOOTSTRAP}$)/ Cap12V

Cap12V x 12V/$V_{BOOTCAP}$ = Cap12V + n x $Cap_{BOOTSTRAP}$

12V/$V_{BOOTCAP}$ x Cap12V – Cap12V = n x $Cap_{BOOTSTRAP}$

Cap12V = (n x $Cap_{BOOTSTRAP}$)/(12V/$V_{BOOTCAP}$ – 1)

Letting V_{BOOT} = 9V, $Cap_{BOOTSTRAP}$ = 470 nF and charging three caps simultaneously:

Cap12V = (3 x 470 nF)/(12V/9V – 1) = 4.23 µF

Use a 4.7 µF capacitor for the +12V LDO.

Letting V_{BOOT} = 9V, $Cap_{BOOTSTRAP}$ = 1 µF and charging three caps simultaneously:

Cap12V = (3 x 1 µF)/(12V/9V – 1) = 9.0 µF

Use a 10 µF capacitor for the +12V LDO.

Letting V_{BOOT}= 9V, $Cap_{BOOTSTRAP}$ = 1 µF and charging one cap at a time:

Cap12V = (1 x 1 µF)/(12V/9V – 1) = 3.0 µF

Use a 3.3 µF capacitor for the +12V LDO.

5.2 Device Protection

5.2.1 MOSFET VOLTAGE SUPPRESSION

When a motor shaft is rotating and power is removed, the magnetism of the motor components will cause the motor to act like a generator. The current that was flowing into the motor will now flow out of the motor. As the motor magnetic field decays, the generator output will also decay. The voltage across the generator terminals will be proportional to the generator current and the circuit impedance of the generator circuit. If the power supply is part of the return path for the current and the power supply is disconnected, then the voltage at the generator terminals will increase until the current flows. This voltage increase must be handled external to the driver. A voltage suppression device must be used to clamp the motor terminal voltage to a level that will not exceed the maximum motor operating voltage. A voltage suppressor should be connected from ground to each motor terminal. The PCB traces must be capable of carrying the motor current with minimum voltage and temperature rise.

An additional method is to inactivate the high-side drivers and to activate the low-side drivers. This allows current to flow through the low-side external MOSFETs and prevents the voltage increases at the power supply terminals. A pure hardware implementation may be done by connecting a bidirectional Transient Voltage Suppressor (TVS) from the gate of each external low-side driver MOSFET to the drain of the same MOSFET. When the phase voltage rises above the TVS standoff voltage, the TVS will start to conduct, pulling up the gate of the low-side MOSFET. This turns on the MOSFET and creates a low-voltage current path for the motor windings to dissipate stored energy. The implementation is a fail-safe mechanism in cases where the supply becomes disconnected or the controller shuts down due to a Fault or command. The MCP8025A/6 Overvoltage Lockout (OVLO) is 32V, so a 33V TVS would be used. This allows the MCP8025A/6 to shut down before the TVS forces the low-side gates high, preventing the MCP8025A/6 low-side drivers from sinking current if they are being driven low. The MCP8025A may use a lower voltage transzorb due to the fact that the MCP8025A driver Overvoltage Lockout (DOVLO) occurs at a lower voltage.

5.2.2 BOOTSTRAP VOLTAGE SUPPRESSION

The pins which handle the highest voltage during motor operation are the bootstrap pins (VBx). The bootstrap pin voltage is typically 12V higher than the associated phase voltage. When the high-side MOSFET is conducting, the phase pin voltage is typically at V_{DD} and the bootstrap pin voltage is typically at V_{DD} + 12V. When the phase MOSFETs switch, current-induced voltage transients occur on the phase pins. Those induced voltages cause the bootstrap pin voltages to also increase. Depending on the magnitude of the phase pin voltage, the bootstrap pin voltage may exceed the safe operating voltage of the device. The current-induced transients may be reduced by slowing down the turn-on and turn-off times of the MOSFETs. The external MOSFETs may be slowed down by adding a 10 to 75Ω resistor in series with the gate drive. The high-side MOSFETs may also be slowed down by inserting a 4Ω resistor between each bootstrap pin and the associated bootstrap diode-capacitor junction. Another 25Ω to 50Ω resistor is then added between the gate drive and the MOSFET gate. This results in a high-side turn-on resistance of 4Ω plus the resistance of the series gate resistor. The high-side turn-off resistance only consists of the series gate resistance and will allow for a faster shutoff time.

36V TVS devices (40V breakdown voltage) should also be connected from each bootstrap pin (VBx) to ground. This will ensure that the bootstrap voltage does not exceed the 46V absolute maximum voltage allowed on the pins. The resistors connected between the bootstrap pins and the bootstrap diode-capacitor junctions, mentioned in the previous paragraph, should also be used in order to limit the TVS current and reduce the TVS package size.

5.2.3 FLOATING GATE SUPPRESSION

The gate drive pins may float when the supply voltage is lost or an overvoltage situation shuts down the driver. When an overvoltage condition exists, the driver high-side and low-side outputs are high-Z. Each external MOSFET that is connected to the gate driver should have a gate-to-source resistor to bleed off any charge that may accumulate due to the high-Z state. This will help prevent inadvertent turn-on of the MOSFET.

5.2.4 MOSFET BODY DIODE REVERSE RECOVERY SNUBBER

When motor current is flowing through the external MOSFET body diodes and the complimentary MOSFET of the phase pair turns on, the body diode reverse recovery creates a momentary short circuit until the reverse recovery time is complete. When the body diode reverse recovery is complete, the current path is opened, causing the phase node voltage to slew rapidly towards ground or V_{DD} levels. The rapid slew rate may cause an inversion of the gate-to-source voltage on the MOSFET that is turning on and result in that MOSFET turning off.

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Adding a drain-to-source snubber slows down the slew rate of the phase node and results in a more controlled excursion of the phase node voltage. The snubber consists of a resistor and a capacitor connected in series between the drain and source of the MOSFET. The resistor is chosen to keep the initial snubber voltage below a few volts when peak motor current is flowing through the body diode. The capacitor is then chosen to provide an RC time constant longer than the MOSFET body diode reverse recovery time. A 0.1Ω resistor is typically used along with a 0.1 µF capacitor to provide an RC of 10 ns.

The power dissipated by the capacitor is calculated by applying Equation 5-1.

EQUATION 5-1: SNUBBER CAPACITOR POWER DISSIPATION

$$P_{DISS} = 2 \times \pi \times f \times C \times V^2 \times \text{Dissipation Factor}$$

Where:

f = PWM Frequency

C = Capacitance

V = Motor Voltage

Dissipation Factor = $2 \times \pi \times f \times C \times ESR = ESR / X_C$

The capacitor and resistor form factors are chosen to handle the dissipated power.

5.3 Related Literature

- AN885, *"Brushless DC (BLDC) Motor Fundamentals"* (DS00885) Microchip Technology Inc., 2003
- AN1160, *"Sensorless BLDC Control with Back-EMF Filtering Using a Majority Function"* (DS01160) Microchip Technology Inc., 2008
- AN1078, *"Sensorless Field Oriented Control of a PMSM"* (DS01078) Microchip Technology Inc., 2010

Figure 5-3 shows the location of the overvoltage TVS devices, gate resistors, bootstrap resistors and gate-to-source resistors.

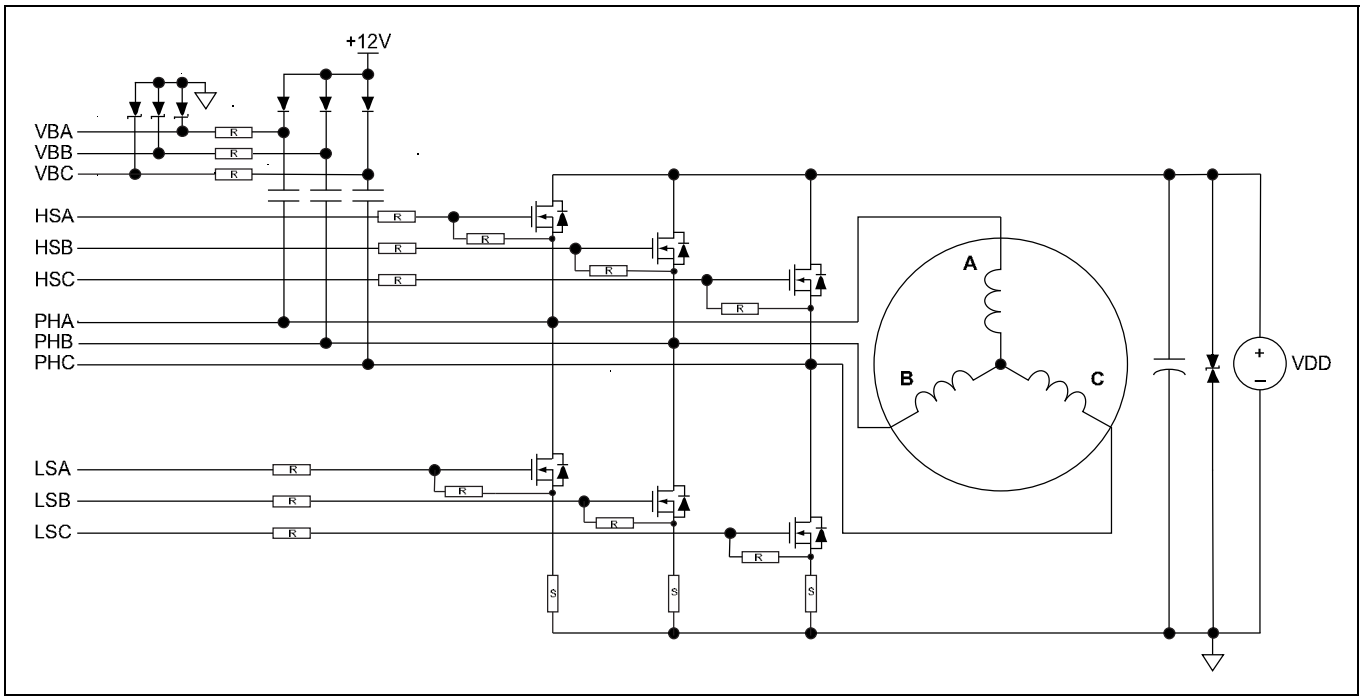

FIGURE 5-3: *Overvoltage Protection.*

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6.0 ERRATA

6.1 V_{BOOT} Not Ready

When CE toggles from a logic '0' to a logic '1', V_{BOOT} must attain 10.8V before the driver outputs will be enabled. If the PWM inputs change state before V_{BOOT} attains 10.8V, the driver outputs will not change and no driver Fault will be issued.

Work Around: When setting CE = 1 from Standby mode, allow time for the V_{BOOT} capacitor to charge up to 10.8V. Typical time is 250 µs.

Device: All

6.2 PWM Pulse Width = Driver Dead-Time Pulse Width

When the PWM input pulse width is the same as the driver programmed dead time, a dead-time race condition may occur that forces both driver outputs to go low until both PWM inputs go low again. Normally, the PWM pulse width is longer than the dead time in order to generate an output pulse equal to PWM_PULSEWIDTH - DEAD TIME. However, some systems allow the PWM pulse width to be smaller than the driver dead time, knowing that there will be no driver output.

Work Around: Set up host minimum PWM pulse width to be at least 50 ns larger or smaller than driver dead-time setting.

Device: All

6.3 Motor Driver Lock

It has been detected that the motor driver can be locked after a momentary drop of V_{DD} below the minimum operating voltage or after enabling the driver output when using low V_{GS} threshold MOSFETs (V_{GS} < 1.1V). The issue was traced back to the high-side driver operation at voltages below the minimum operating voltage.

Work Around: None.

Device: MCP8026 – Date codes prior to YYWW = 1635

6.4 External MOSFET DUVLO and OCP Detection

These detection functions could flag an inexistent motor driver undervoltage or power MOSFET overcurrent Fault when a DE2 message was sent to enable the functions while the motor was running.

Work Around: Stop the motor before enabling the external MOSFET UVLO and OCP protection, and try to keep the blanking time as long as motor application allows.

Device: MCP8025A – All date codes;
MCP8026 – Date codes prior to YYWW = 1635

6.5 External MOSFET DUVLO and OCP Fault

When a resistor is used in series with the VBx bootstrap pins, an external MOSFET undervoltage Fault and/or Overcurrent Protection Fault may occur. This is caused by the voltage drop across the resistor when the complementary driver transistors switch state. The switching overlap may draw enough current to lower the voltage long enough to trigger the Fault. Increasing the bootstrap capacitance and charge time will provide more energy storage.

Work Around: When a series VBx bootstrap resistor is used with short duration off time duty cycles (<8%), the value should be kept below 4 ohms.

Device: All

6.6 Supply Start-up Sequence

It has been detected that in cases where V_{DD} momentarily dropped below the minimum operating voltage and then recovered, the driver buck regulator could restart before the supply voltage reached 6V.

Work Around: Keep V_{DD} within the operational voltage limits set forth in the data sheet.

Device: MCP8026 – Date codes prior to YYWW = 1635

6.7 Buck Overvoltage

It has been observed that the buck output voltage may exceed the target voltage for <1.5 ms, after power-up, under certain power-up scenarios. The issue is caused by an unintended current that may flow into the FB pin, causing an additional voltage drop across the resistor R1 (high-side of resistor divider), from the buck output to the FB pin. The overvoltage has only been observed on an application with no resistive load on the +5V LDO output to discharge the 5V LDO capacitor to 0V before the system is powered up again, but it cannot be excluded that other applications may also be affected.

Work Around: The overvoltage will be minimized if the resistor selection for R2 (low-side of resistor divider) in **Section 5.1.3.3 "Setting the Buck Output Voltage"** is 620 ohms or less.

Device: All

6.8 Minimum Fault Clearing Pulse Width

It has been detected that the minimum Fault clearing pulse-width parameter is too narrow for the CE pin input filter. The correct minimum Fault clearing pulse width is 4 µs.

Work Around: The host should generate a minimum Fault clearing pulse width of 4 µs.

Device: All

6.9 Start-up DE2 Message

A STAT1 message with the BORW bit set is sent one time by the MCP802X device upon start-up. The message is immediately sent when either the CE pin goes high or when the DE2 pin goes low. This may cause a collision with a host message.

Work Around: Pulse the CE pin low-high-low at start-up before sending any messages to the MCP802X device. This triggers the MCP802X to send the BORW message and prevent any collision.

Device: All

6.10 Buck Start-up Issue

It has been detected that when V_{DD} rises faster than 0.083 [V/µs], the driver could enter into Sleep mode.

Work Around: Keep V_{DD} slew rate slower than 0.083 [V/µs]. If this is not possible, the device could leave Sleep mode via the CE or LIN signals.

Device: All

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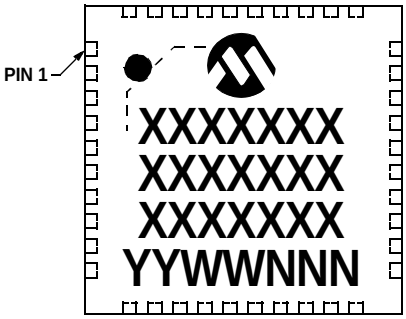
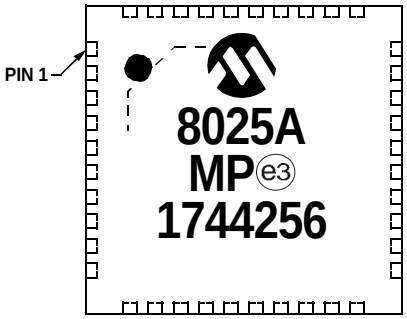
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

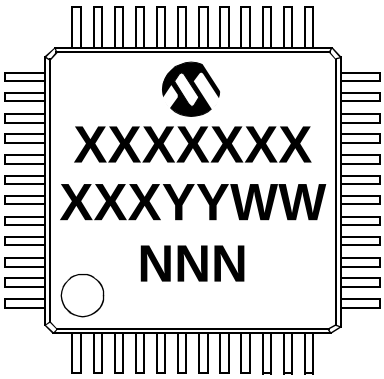
40-Lead QFN (5x5x0.85 mm)



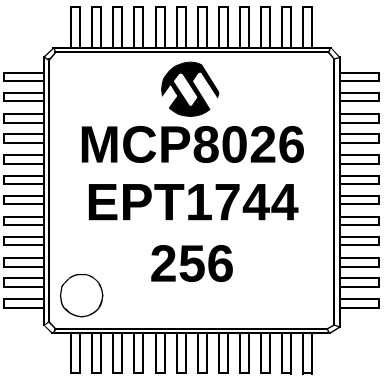
Example



48-Lead TQFP (7x7x1 mm)



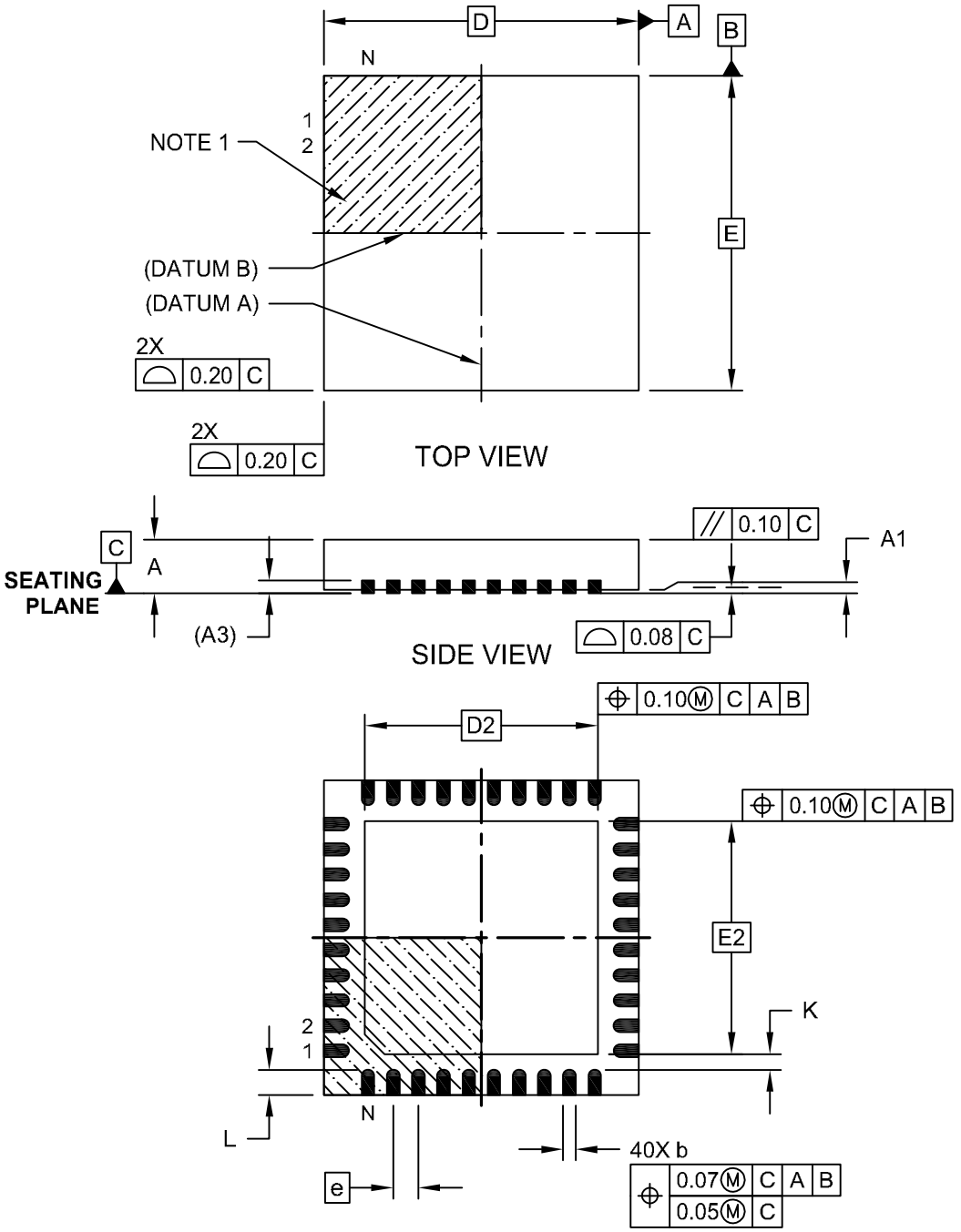
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.	

40-Lead Plastic Quad Flat, No Lead Package (MP) - 5x5 mm Body [QFN]
With 3.7x3.7 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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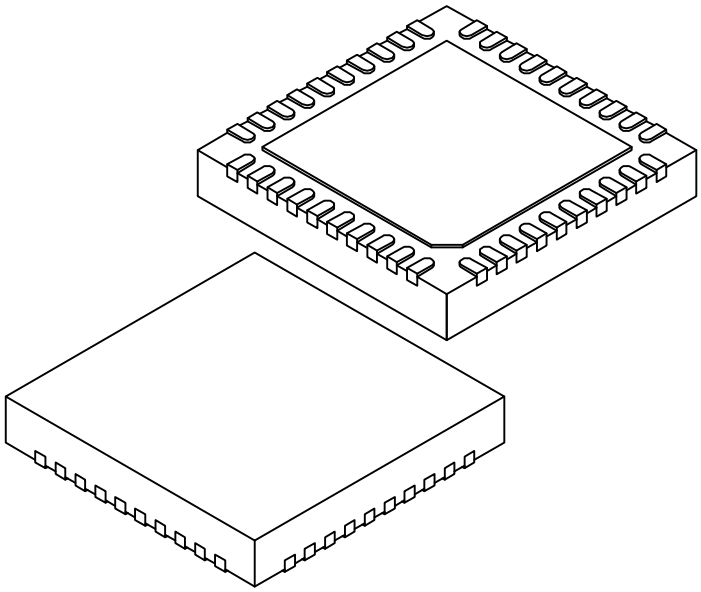
40-Lead Plastic Quad Flat, No Lead Package (MP) - 5x5 mm Body [QFN] With 3.7x3.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	40		
Pitch	e	0.40 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	5.00 BSC		
Exposed Pad Width	E2	3.70 BSC		
Overall Length	D	5.00 BSC		
Exposed Pad Length	D2	3.70 BSC		
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

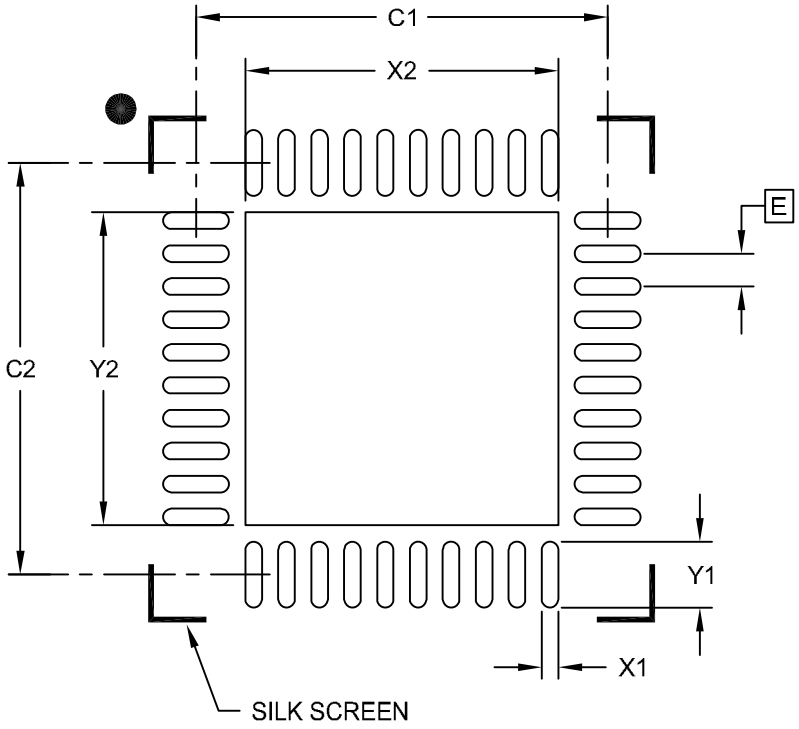
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-047-002A Sheet 2 of 2

40-Lead Plastic Quad Flat, No Lead Package (MP) - 5x5 mm Body [QFN] With 3.7x3.7 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			3.80
Optional Center Pad Length	Y2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.80

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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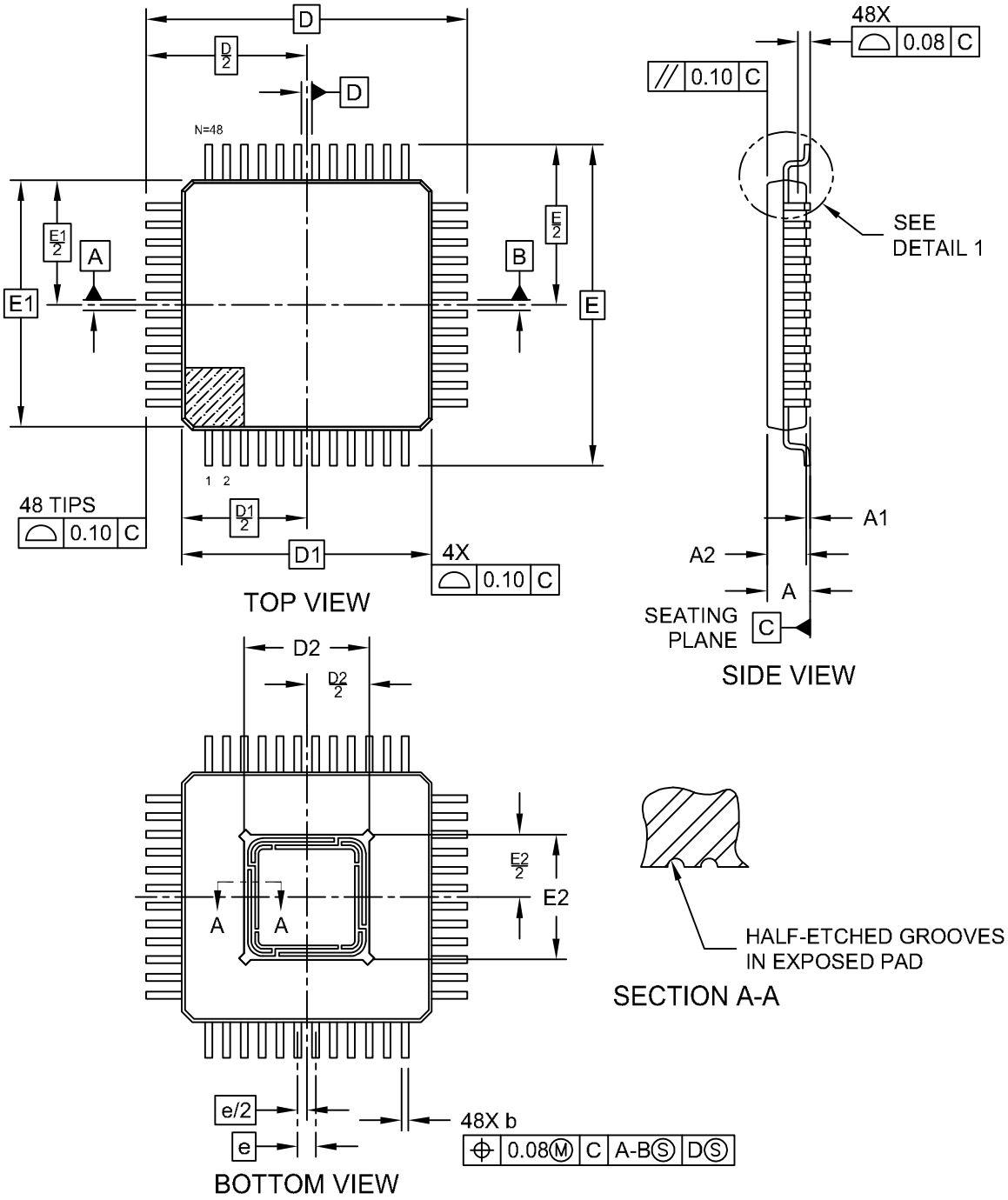
48-Lead Thermally Enhanced Thin Quad Flat Pack (PT) 7x7x1.0 mm Body [TQFP] With Grooved Exposed Pad

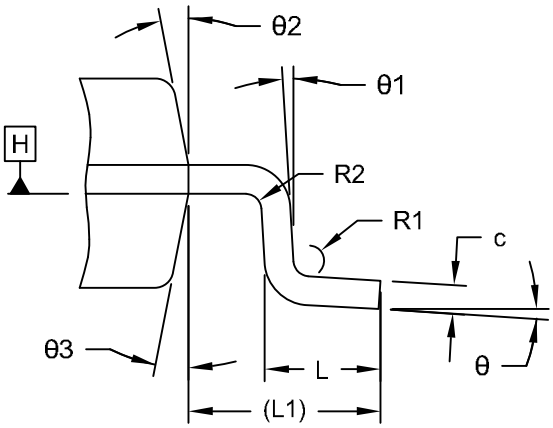
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

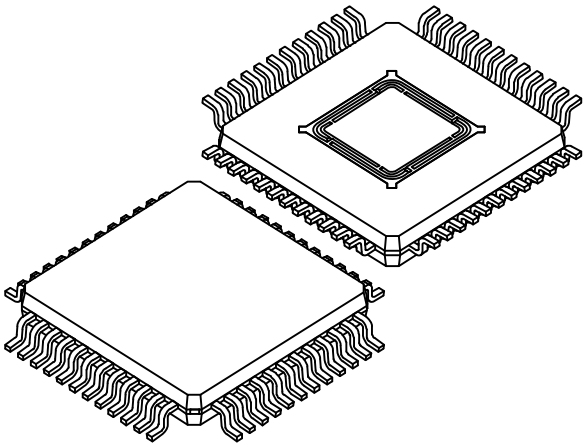


Microchip Technology Drawing C04-183 Rev B Sheet 1 of 2

48-Lead Thermally Enhanced Thin Quad Flat Pack (PT) 7x7x1.0 mm Body [TQFP] With Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL 1

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	48		
Lead Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D	9.00 BSC		
Molded Package Length	D1	7.00 BSC		
Molded Package Length	D2	3.40	3.50	3.60
Overall Width	E	9.00 BSC		
Molded Package Width	E1	7.00 BSC		
Molded Package Length	E2	3.40	3.50	3.60
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Width	b	0.17	0.20	0.27
Lead Thickness	c	0.09	-	0.20
Lead Width	R1	0.08	-	-
Lead Width	R2	0.08	-	0.20
Terminal Foot Angle	θ	0°	3.5°	7°
Lead Angle	θ1	0°	-	-
Mold Draft Angle Top	θ2	11°	12°	13°
Mold Draft Angle Bottom	θ3	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-183 Rev B Sheet 2 of 2

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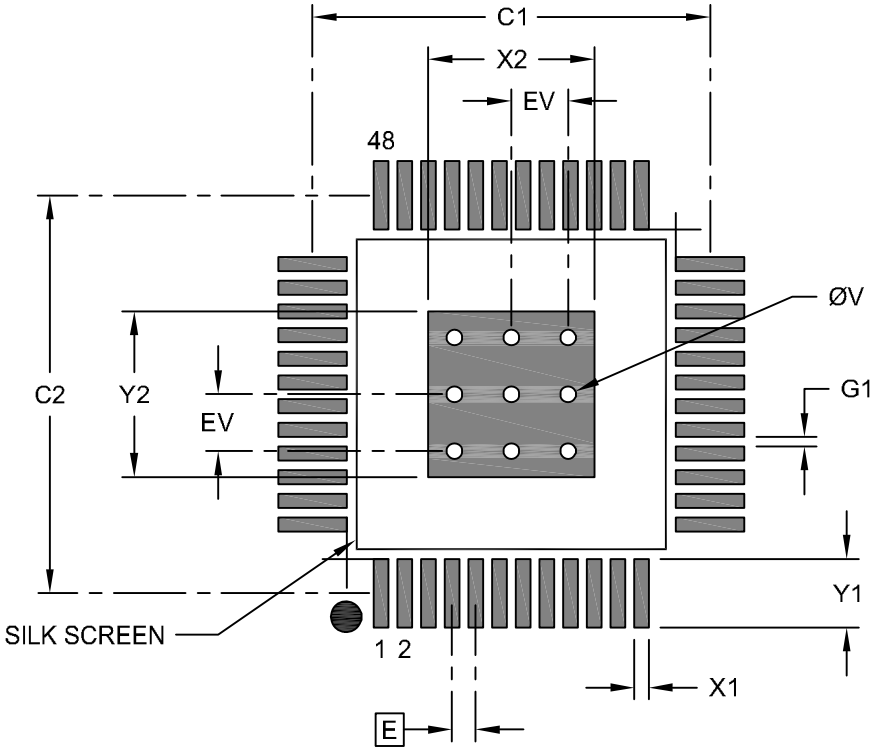
48-Lead Thermally Enhanced Thin Quad Flat Pack (PT) 7x7x1.0 mm Body [TQFP] With Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			3.50
Center Pad Length	Y2			3.50
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.45
Contact Pad to Center Pad (X44)	G1	0.20		
Thermal Via Diameter	ØV		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2183 Rev B

NOTES:

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APPENDIX A: REVISION HISTORY

Revision C (October 2018)

- Updated **“Features”** section, removed **“AEC-Q100 Grade 0 Qualified”**.
- Updated **“Applications”** section.
- Updated **Note 2** in **“AC/DC Characteristics”** table.
- Updated **“ESD, Susceptibility, Surge and Latch-up Testing”** table.
- Updated **Section 4.5.1 “LIN Bus Transceiver (MCP8025A)”**.
- Updated **Section 4.5.2 “Level Translator (MCP8026)”**.
- Updated **Section 6.4 “External MOSFET DUVLO and OCP Detection”**.
- Added **Section 6.10 “Buck Start-up Issue”** in **Section 6.0 “Errata”**.

Revision B (May 2018)

- Updated Figure 5-3.
- Added **Section 6.9 “Start-up DE2 Message”** in **Section 6.0 “Errata”**.

Revision A (November 2017)

- Original release of this document.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[1]	-X	X	/XX
Device	Tape and Reel	Temperature Warning	Temperature Range	Package

Device:

MCP8025A:	3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode and LIN Transceiver
MCP8025AT:	3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode and LIN Transceiver (Tape and Reel)
MCP8026:	3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode and LIN Transceiver
MCP8026T:	3-Phase Brushless DC (BLDC) Motor Gate Driver with Power Module, Sleep Mode and LIN Transceiver (Tape and Reel)

Tape and Reel: T = Tape and Reel [1]
Blank = Tube

Temperature Warning: 115 = +115°C

Temperature Range: E = -40°C to +125°C (Extended)
H = -40°C to +150°C (High)

Package: MP = Plastic Quad Flat, No Lead Package – 5 x 5 mm Body with 3.5 x 3.5 mm Exposed Pad, 40-Lead
PT = Thin Quad Flatpack – 7 x 7 x 1.0 mm Body with Exposed Pad, 48-Lead

Examples:

a) MCP8025A-115E/MP: Extended temperature, 40-Lead 5x5 QFN package
b) MCP8025AT-115E/MP: Tape and Reel, Extended temperature, 40-Lead 5x5 QFN package
c) MCP8025A-115H/MP: High temperature, 40-Lead 5x5 QFN package
d) MCP8025AT-115H/MP: Tape and Reel, High temperature, 40-Lead 5x5 QFN package
e) MCP8026-115E/MP: Extended temperature, 40-Lead 5x5 QFN package
f) MCP8026T-115E/MP: Tape and Reel, Extended temperature, 40-Lead 5x5 QFN package
g) MCP8026-115H/MP: High temperature, 40-Lead 5x5 QFN package
h) MCP8026T-115H/MP: Tape and Reel, High temperature, 40-Lead 5x5 QFN package
i) MCP8025A-115E/PT: Extended temperature, 48-Lead TQFP-EP package
j) MCP8025AT-115E/PT: Tape and Reel, Extended temperature, 48-Lead TQFP-EP package
k) MCP8025A-115H/PT: High temperature, 48-Lead TQFP-EP package
l) MCP8025AT-115H/PT: Tape and Reel, High temperature, 48-Lead TQFP-EP package
m) MCP8026-115E/PT: Extended temperature, 48-Lead TQFP-EP package
n) MCP8026T-115E/PT: Tape and Reel, Extended temperature, 48-Lead TQFP-EP package
o) MCP8026-115H/PT: High temperature, 48-Lead TQFP-EP package
p) MCP8026T-115H/PT: Tape and Reel, High temperature, 48-Lead TQFP-EP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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SYST-01WULB292 - Data Sheet - MCP8025A/MCP8026 3-Phase Brushless DC (BLDC) Motor Gate Driver

Affected Catalog Part Numbers(CPN)

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MCP8025A-115H/MPVAO
MCP8025A-115H/PT
MCP8025AT-115E/MP
MCP8025AT-115E/PT
MCP8025AT-115H/MP
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MCP8025AT-115H/PT
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