

PCN # 1702A

DATE: August 28, 2018

EXPECTED PCN SHIP DATE: August 28, 2018



Quality Assurance
160 Rio Robles
San Jose, CA 95134

www.maximintegrated.com

PROCESS CHANGE NOTICE
 PRODUCT CHANGE NOTICE

MAXIM INTEGRATED HEREBY ISSUES NOTIFICATION OF CHANGE
THAT MAY AFFECT THE FOLLOWING CATEGORIES:

DESIGN WAFER FAB ASSEMBLY TEST ELEC/MECH SPECS

AFFECTED PRODUCT:

Ordering P/N: (See PN listing XLS in PCN ZIP file)

CHANGE FROM: - Maxim products in SOIC(N) package manufactured at current subcontractor	CHANGE TO: - Additional Assembler Greatek in Taiwan/R.O.C.
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JUSTIFICATION: -
Maxim has selected Greatek to expand assembly capacity. Greatek is an established assembly subcontractor and is certified under QS 9000, ISO/TS 16949, ISO 14001 and Sony Green Partner.
This new partnership will enhance Maxim's Supply-Chain to meet capacity demands, flexibility and on-time delivery. Qualification results are reflected in Maxim's Reliability report attached (R29114CQ).
There are no changes to the form, fit, function or quality of the devices.

TRACEABILITY: Maxim Integrated maintains full traceability by device marking, packaging labels and shipment documents.

Maxim Integrated's Change Notification System is designed to keep our customer base apprised of major product, manufacturing, or facility improvements.

Nasser Ali Chaouche

Nasser AliChaouche / PCN Coordinator

For further information, please contact either of the people listed below.

Contact your local Maxim Integrated Company Representative or Nasser AliChaouche, PCN Coordinator
408-601-5660 / pcn.coordinator@maximintegrated.com

Affected product numbers	Customer part number	PCN Proposed Ship Date
ICL7662CBA+		28-Aug-18
ICL7662CBA+T		28-Aug-18
ICL7662CBA+TG002		28-Aug-18
MAX14780EESA+		28-Aug-18
MAX14780EESA+T		28-Aug-18
MAX15013AASA+		28-Aug-18
MAX15013AASA+T		28-Aug-18
MAX1771ESA+		28-Aug-18
MAX1771ESA+T		28-Aug-18
MAX1771ESA+TG002		28-Aug-18
MAX202ECSE+		28-Aug-18
MAX202ECSE+G126		28-Aug-18
MAX202ECSE+T		28-Aug-18
MAX202ECSE+TG002		28-Aug-18
MAX202ECSE+TG068		28-Aug-18
MAX202ECSE+TG074		28-Aug-18
MAX202ECSE+TG126		28-Aug-18
MAX202ECSE+TG52		28-Aug-18
MAX202EESA+		28-Aug-18
MAX202EESA+G126		28-Aug-18
MAX202EESA+T		28-Aug-18
MAX202EESA+TG002		28-Aug-18
MAX202EESA+TG074		28-Aug-18
MAX202EESA+TG126		28-Aug-18
MAX232EESA+		28-Aug-18
MAX232EESA+T		28-Aug-18
MAX253ESA+		28-Aug-18
MAX253ESA+T		28-Aug-18
MAX253ESA+TG002		28-Aug-18
MAX3053ESA+		28-Aug-18
MAX3053ESA+G126		28-Aug-18
MAX3053ESA+T		28-Aug-18
MAX3058ASA+		28-Aug-18
MAX3058ASA+T		28-Aug-18
MAX3082EESA+		28-Aug-18
MAX3082EESA+T		28-Aug-18
MAX3085EESA+		28-Aug-18
MAX3085EESA+T		28-Aug-18
MAX3232CSE+		28-Aug-18
MAX3232CSE+T		28-Aug-18
MAX3232CSE+TG002		28-Aug-18
MAX3232CSE+TG05		28-Aug-18
MAX3232CSE+TG068		28-Aug-18
MAX3232CSE+TG071		28-Aug-18
MAX3232CSE+TG1Z		28-Aug-18
MAX3232EESA+		28-Aug-18

MAX3232ESE+G002		28-Aug-18
MAX3232ESE+G035		28-Aug-18
MAX3232ESE+T		28-Aug-18
MAX3232ESE+TG002		28-Aug-18
MAX3232ESE+TG035		28-Aug-18
MAX3232ESE+TG071		28-Aug-18
MAX3232ESE+TG52		28-Aug-18
MAX3430ESA+		28-Aug-18
MAX3430ESA+T		28-Aug-18
MAX3430ESA+TG002		28-Aug-18
MAX3485EESA+		28-Aug-18
MAX3485EESA+G126		28-Aug-18
MAX3485EESA+T		28-Aug-18
MAX3485EESA+TG002		28-Aug-18
MAX3485EESA+TG126		28-Aug-18
MAX3485EESA+TG52		28-Aug-18
MAX3490EESA+		28-Aug-18
MAX3490EESA+G126		28-Aug-18
MAX3490EESA+T		28-Aug-18
MAX3490EESA+TG126		28-Aug-18
MAX485ECSA+		28-Aug-18
MAX485ECSA+G002		28-Aug-18
MAX485ECSA+T		28-Aug-18
MAX487ECSA+		28-Aug-18
MAX487ECSA+T		28-Aug-18
MAX487EESA+		28-Aug-18
MAX487EESA+T		28-Aug-18
MAX6675ISA+		28-Aug-18
MAX6675ISA+T		28-Aug-18
MAX705ESA+		28-Aug-18
MAX705ESA+T		28-Aug-18
MAX705ESA+TG002		28-Aug-18
MAX705ESA+TGA5		28-Aug-18
MAX706ESA+		28-Aug-18
MAX706ESA+T		28-Aug-18
MAX706ESA+TG002		28-Aug-18
MAX706ESA+TG126		28-Aug-18
MAX706RESA+		28-Aug-18
MAX706RESA+T		28-Aug-18
MAX706RESA+TG035		28-Aug-18
MAX706RESA+TG52		28-Aug-18
MAX706SESA+		28-Aug-18
MAX706SESA+T		28-Aug-18
MAX706SESA+TG002		28-Aug-18
MAX706SESA+TG126		28-Aug-18
MAX706SESA+TG52		28-Aug-18

1) PURPOSE

To qualify assembler Greatek to build SOIC(N) packages with 0.8/1.0/1.3/2.0 mil Au-wire

QUALIFICATION REQUIREMENTS AND RESULTS

Rel#	R29114A	R29114C	R29114D		
Lot#	JQ3AHA023DC	JQ3AHA023DE	JQ3AHA023DG		
Device:	MAX1709ESE+	MAX1709ESE+	MAX1709ESE+		
Die Type:	PX35Y	PX35Y	PX35Y		
Die Size (mils)	86X193 mil	86X193 mil	86X193 mil		
Package Type (code):	S16+8	S16+8	S16+8		
Date Code:	1738	1738	1738		
Topmark:	ZQ3A JCF	ZQ3A JCF	ZQ3A JCF		
Stress Test	Duration	Sampling Plan	Result	Result	Result
Convection Reflow ^{*2,3} 260°C Peak	MSL 1, 3X	0/400	0/399	0/400	0/400
HAST 130°C / 85% R.H. ^{*1,2,3}	96 hrs.	0/77	0/77	0/77	0/77
Unbiased HAST 130°C / 85% R.H. ^{*1,2}	96 hrs.	0/77	0/77	0/77	0/77
Temperature Cycle ^{*1,2,3} -65°C to 150°C (Condition C)	500 cyc	0/77	0/77	0/77	0/77
High Temperature Storage 150°C ^{*1,2,3}	1000 hrs.	0/77	0/77	0/77	0/77
HTOL ^{*2,3,4}	1000 hrs	0/77		0/77	
C-SAM*1	T0, Post-Precon	0/25	0/25	0/25	0/25
Wire Bond Pull Minimum 5 grams-force	T (0), Post-TC	0/200 wires	0/200wires	0/200wires	0/200wires
Solderability (Lead-Free,245C)	T (0)	0/15	0/15	0/15	0/15
Physical Dimension (PD)	T (0)	0/20	0/20	0/20	0/20
Bondcrater	Post-Precon	0/20	0/20	0/20	0/20
Solder Shock		0/15	0/15	0/15	0/15

Note:

- *1. Convection reflow is used as preconditioning for SMD packages.
- *2. Electrical tests pre- and post-stress were performed at +85°C.
- *3. Electrical tests pre- and post-stress were performed at +25°C.
- *4. Electrical tests pre- and post-stress were performed at -40°C.

Rel#	R29114E	R29114F	R29114G		
Lot#	J6Y5GA819FA	J6Y5GA819FB	N380B3108CA		
Device:	MAX5033BASA+	MAX5033BASA+	MAX494CSD+		
Die Type:	NP25U-5Z	NP25U-5Z	OX56Y		
Die Size (mils)	85 X 145	85 X 145	69 X 100		
Package Type (code):	S8+5	S8+5	S14+1		
Date Code:	1744	1744	1744		
Topmark:	Z DM	Z DM	Z380 NCX		
Stress Test	Duration	Sampling Plan	Result	Result	Result
Convection Reflow ^{*2,3,5} 260°C Peak	MSL 1, 3X	0/400	0/400	0/400	0/400
HAST 130°C / 85% R.H. ^{*1,2,3,5}	96 hrs.	0/77	0/77	0/77	0/77
Unbiased HAST 130°C / 85% R.H. ^{*1,2}	96 hrs.	0/77	0/77	0/77	0/77
Temperature Cycle ^{*1,2,3,5} -65°C to 150°C (Condition C)	500 cyc	0/77	0/77	0/77	0/77
High Temperature Storage 150°C ^{*1,2,3}	1000 hrs.	0/77	0/77	0/77	0/77
HTOL ^{*2,3,4}	1000 hrs	0/77	0/77		
C-SAM*1	T0, Post-Precon	0/25	0/25	0/25	0/25
Wire Bond Pull Minimum 5 grams-force	T (0), Post-TC	0/200 wires	0/200wires	0/200wires	0/200wires
Solderability (Lead-Free,245C)	T (0)	0/15	0/15	0/15	0/15
Physical Dimension (PD)	T (0)	0/20	0/20	0/20	0/20
Bondcrater	Post-Precon	0/20	0/20	0/20	0/20
Solder Shock		0/15	0/15	0/15	0/15

Note:

- *1. Convection reflow is used as preconditioning for SMD packages.
- *2. Electrical tests pre- and post-stress were performed at +125°C.
- *3. Electrical tests pre- and post-stress were performed at +25°C.
- *4. Electrical tests pre- and post-stress were performed at -40°C.
- *5. Electrical tests pre- and post-stress were performed at +70°C.

Rel#			R29114K	R29114L
Lot#			JQ9CHA128JA	JQ9CHA128JB
Device:			MAX6198BESA+	MAX6198BESA+
Die Type:			RF23Z-2Z	RF23Z-2Z
Die Size (mils)			44X31	44X31
Package Type (code):			S8+2	S8+2
Date Code:			1742	1742
Topmark:			MAX6198BESA+ / 1742	MAX6198BESA+ / 1742
Stress Test	Duration	Sampling Plan	Result	Result
Convection Reflow *2,3 260°C Peak	MSL 1, 3X	0/400	0/400	0/400
HAST 130°C / 85% R.H. *1,2,3	96 hrs.	0/77	0/77	0/77
Unbiased HAST 130°C / 85% R.H. *1,2	96 hrs.	0/77	0/77	0/77
Temperature Cycle *1,2,3 -65°C to 150°C (Condition C)	500 cyc	0/77	0/77	0/77
High Temperature Storage 150°C *1,2,3	1000 hrs.	0/77	0/77	0/77
HTOL *2,3,4	1000 hrs	0/77	0/77	
Solderability (Lead-Free,245C)	-	0/15	0/15	0/15
C-SAM*1	-	0/25	0/25	0/25
Wire Bond Pull Minimum 5 grams-force	T (0), Post-TC	0/200 wires	0/200 wires	0/200 wires
Physical Dimension (PD)	T (0)	0/20	0/20	0/20
Bondcrater	Post-Precon	0/20	0/20	0/20
Solder Shock		0/15	0/20	0/20

Note:

- *1. Convection reflow is used as preconditioning for SMD packages.
- *2. Electrical tests pre- and post-stress were performed at +85°C.
- *3. Electrical tests pre- and post-stress were performed at +25°C.
- *4. Electrical tests pre- and post-stress were performed at -40°C.

2) CONCLUSION

Qualification lots assembled in Greatek have passed reliability qualification (Full Qualification Requirements / Acceptance Criteria). Therefore, assembler Greatek is fully qualified to build SOIC(N) packages with 0.8/1.0/1.3/2.0 mil Au-wire. These packages, as tested MSL1, are not moisture sensitive, therefore, requires no bake-and-bag precautions for shipment and/or storage.

3) Package Coverage

The following packages can be covered by this qualification result.

S14+1	S14+6	S16+5	S8+17	S8+20	S8+4
S14+4	S16+1	S16+6	S8+18	S8+21	S8+5
S14+5	S16+3	S16+8	S8+2	S8+22	