Product Change Notification - SYST-19IPBJ191

Date:

26 Jun 2018

Product Category:

32-bit PIC Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - SAM L10/L11 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-19IPBJ191

Microchip has released a new DeviceDoc for the SAM L10/L11 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at SAM L10/L11 Family Silicon Errata and Data Sheet Clarification.

ERRATA - SAM L10/L11 Family Silicon Errata and Data Sheet Clarification
Notification Status: Final

Description of Change: 1) Initial release.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 25 Jun 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

SAM L10/L11 Family Silicon Errata and Data Sheet Clarification

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SAM L10/L11 Family

Silicon Errata and Data Sheet Clarification

SAM L10/L11 Family

The SAM L10/L11 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001513B), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in the Silicon Issue Summary.

The errata described in this document will be addressed in future revisions of the SAM L10/L11 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 3. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L10 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML10E16A	0x2084xx00	0x1
SAML10E15A	0x2084xx01	
SAML10E14A	0x2084xx02	
SAML10D16A	0x2084xx03	
SAML10D15A	0x2084xx04	
SAML10D14A	0x2084xx05	

Table 2. SAM L11 Family Silicon Device Identification

Part Number	Device ID (DID[31:0])	Revision (DID.REVISION[3:0])
		B
SAML11E16A	0x2083xx00	0x1
SAML11E15A	0x2083xx01	
SAML11E14A	0x2083xx02	
SAML11D16A	0x2083xx03	
SAML11D15A	0x2083xx04	
SAML11D14A	0x2083xx05	

Note: Refer to the “Device Service Unit” chapter in the current Device Data Sheet (DS60001513B) for detailed information on Device Identification and Revision IDs for your specific device.

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1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Feature	Summary	Affected Silicon Revisions
			B
ADC	Reference Buffer Offset Compensation	First ADC conversions are incorrect when using Reference Buffer Offset Compensation.	X
CCL	PAC protection	Writing the Software Reset bit in the Control A register will trigger a PAC protection error.	X
CCL	Enable-protected Registers	The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit.	X
CCL	Sequential logic	LUT Output is corrupted after enabling CCL when sequential logic is used.	X
Device	Temperature sensor	Temperature sensor is not functional.	X
DMAC	Linked descriptors	When using concurrent channel triggers, DMA write-back descriptors may get corrupted.	X
EIC	PAC protection	EIC reads/writes on the reserved area between the CONFIG and the DEBOUNCEN registers do not generate a PAC protection error.	X
FREQM	PAC protection	FREQM reads on the Control B register generate a PAC protection error.	X
MCLK	PAC protection	Writes to the MCLK Control A register do not generate a PAC protection error even if this register has been write-protected using the PAC.	X
MCLK	DFLLULP clock	Hardfault exception after having selected DFLLULP clock as main clock.	X
OPAMP	Reference buffer	The internal reference REFBUF is not generated when the voltage doubler is disabled.	X
OPAMP	High Gain Instrumentation Amplifier	High Gain Instrumentation Amplifier is not functional.	X
RTC	Tamper detection	Tamper detection limitation when CTRLB.SEPTO = 0.	X
RTC	Event generation	Periodic Daily Event (PERD) Event Generator never occurs in Clock/Calendar mode.	X

Module	Feature	Summary	Affected Silicon Revisions
			B
RTC	Write corruption	RTC COUNT and CLOCK registers write corruption.	X
SERCOM I^2C	High-speed mode	When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	X
SERCOM I^2C	Repeated start	Bus error is generated during a Repeated Start (when QCEN = 1 and SCLSM = 1).	X
SERCOM I^2C	Repeated Start / Master mode 10-bit	Repeated Start in 10-bit addressing mode for Master Write operations does not work.	X
SERCOM I^2C	Repeated Start / Master mode 10-bit	Repeated Start is not supported for High-Speed mode Master Read operations.	X
SERCOM I^2C	Repeated Start / High-Speed mode	Repeated Start is not supported for High-Speed mode Master Write operations.	X
SERCOM I^2C	Slave Mode with DMA	Character lost in I^2C Slave mode with DMA when a NACK occurs.	X
SERCOM I^2C	Slave mode 10-bit	I^2C Slave 10-bit addressing mode is not functional.	X
SERCOM I^2C	Status Flag	BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR Status register bits are not automatically cleared.	X
SERCOM I^2C	Status Flag	The CLKHOLD Status bit is not read only.	X
SERCOM SPI	Data Preload	Data lost in SPI Slave mode with Data Preload Enabled.	X
SERCOM USART	Inverted Bits	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	X
SERCOM USART	ISO7816 Mode	In ISO7816 mode, the SERCOM bus clock continues to run in Stand-by Sleep mode causing an extra power consumption.	X
SERCOM USART	Debug Mode	Debug mode is not functional.	X
SERCOM USART	Collision Detection	Collision Detection does not stop Data Transfer.	X
TC	Flags Synchronization	The SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.	X

Module	Feature	Summary	Affected Silicon Revisions
			B
TC	Capture mode / Over consumption	Over consumption in Capture mode when entering Standby mode.	X
TRNG	Over consumption	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	X

2. SAM L10/L11 Errata Issues

The following issues apply to the SAM L10/L11 Family devices.

2.1 ADC

2.1.1 Reference Buffer Offset Compensation

ADC converted data may be erroneous when using the Reference Buffer (REFCTRL.REFSEL = INTREF, INTVCC0, INTVCC1, VREFA or VREB) and Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1).

Workaround

The first five conversions must be ignored. All further ADC conversions are accurate.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2 Configurable Custom Logic (CCL)

2.2.1 PAC Protection

Writing the Software Reset bit in the Control A register (CTRLA.SWRST) will trigger a PAC protection error.

Workaround

Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.2 Enable Protected Registers

The SEQCTRL0 and LUCTRL0/1 registers are enable-protected by the CTRL.ENABLE bit whereas they should be enable-protected by the LUTCTRL0/1.ENABLE bits.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.2.3 Sequential Logic

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround

Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.3 DEVICE

2.3.1 Temperature Sensor

Temperature Sensor is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.4 Direct Memory Access Controller (DMAC)

2.4.1 Linked Descriptors

When using concurrent channels triggers, DMAC write-back descriptors may get corrupted.

Workaround

Multiple transfers must only be sequenced using linked descriptors on a single channel.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.5 External Interrupt Controller (EIC)

2.5.1 PAC Protection

EIC reads/writes on the reserved area between the CONFIG and the DEBOUNCEN registers do not generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.6 Frequency Meter (FREQM)

2.6.1 PAC Protection

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7 Main Clock (MCLK)

2.7.1 PAC Protection

Writes to the MCLK Control A register (MCLK.CTRLA) do not generate a PAC protection error even if this register has been write-protected using the PAC.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.7.2 DFLLULP Clock

A Hard fault exception can occur after selecting the DFLLULP clock as main clock source (CTRLA.CKSEL = 1).

Workaround
Add 6 NOP instructions after writing the CTRAL.CKSEL bit.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8 Operational Amplifier Controller (OPAMP)

2.8.1 Reference Buffer

The internal reference REFBUF is not generated when the voltage doubler is disabled (CTRLA.LPMUX = 1).

Workaround
Enable the voltage doubler (CTRLA.LPMUX = 0) when the internal REFBUF is used.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.8.2 High Gain Instrumentation Amplifier

High Gain Instrumentation Amplifier is not functional.

Workaround
None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9 RTC

2.9.1 Tamper Detection

When the RTC Separate Tamper Outputs (SEPTO) bit of the CTRLB register is cleared (CTRLB.SEPTO=0) and the Active layer protection 0 (ALSI0) bit of the TAMPCTRLB register is set (TAMCTRLB.ALSI0=1), the RTC pseudo random pattern is only generated on the TrustRAM Active layer.

Workaround

Set the CTRLB.SEPTO bit to '1' if Tamper Detection is required on the RTC Tamper pins.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.2 Event Generation

In RTC Clock mode or Calendar mode (CTRLA.MODE = 2), the Periodic Daily Event (PERD) is not generated.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.9.3 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround
Write the registers with:

- A 32-bit write access for:
  - COUNT register in COUNT32 mode
  - CLOCK register in CLOCK mode
- A 16-bit write access for:
  - COUNT register in COUNT16 mode

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10 Serial Communication Interface Inter-Integrated Circuit (SERCOM I²C)

2.10.1 High-Speed Mode

When configured in HS or Fast-Mode Plus, SDA and SCL fall times are shorter than I²C specification requirement and can lead to reflection.

Workaround
When reflection is observed, a 100 ohm serial resistor can be added on the impacted line.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.2 Repeated Start

When Quick command is enabled (CTRLB.QCEN = 1), the software can issue a Repeated Start by either writing the CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM = 1, a bus error will be generated.

Workaround
Use Quick Command mode (CTRLB.QCEN = 1) only if SCL Stretch mode is CTRLA.SCLSM = 0.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.3 Repeated Start

For Master Write operations (excluding High-Speed mode), in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not issue correctly a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate properly a Repeated Start.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.4 Repeated Start

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.5 Repeated Start

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.6 Slave Mode with DMA

In I^2C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Since a NACK was received, the transfer on the I^2C bus will not occur causing the loss of this data.

Workaround

Configure the DMA transfer size to the number of data to be received by the I^2C master. DMA cannot be used if the number of data to be received by the master is not known.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.7 Slave Mode 10-bit

I^2C slave 10-bit addressing mode is not functional.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.8 Status Flags

In Slave mode, the BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR STATUS register bits are not automatically cleared when INTFLAG.AMATCH is cleared.

Workaround

Clear the STATUS register bits, BUSERR, COLL, LOWTOUT, SEXTTOUT and LENERR, by writing these STATUS bits to '1' when INTFLAG.AMATCH is cleared.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.10.9 Status Flags

The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.

Workaround

Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.11 Serial Communication Serial Peripheral Interface (SERCOM SPI)

2.11.1 Data Preload

In SPI Slave mode with Slave Data Preload Enabled (CTRLB.PLOADEN = 1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select pin low until the end of transmission.

Workaround

In SPI Slave mode, the Slave Select (SS) pin must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN = 1).

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12 Serial Communication Interface USART (SERCOM USART)

2.12.1 Inverted Bits

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

Workaround

In software, interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.2 ISO7816 Mode

When the SERCOM USART is in ISO7816 mode, the SERCOM bus clock continues to run in Standby Sleep mode causing extra power consumption.

Workaround

Disable the USART before entering Standby Sleep mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.3 Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP = 1, data transmission is not halted when entering Debug mode.

Workaround

None.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.12.4 Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN = 1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB clock is lower than the SERCOM generic clock.

Workaround
The SERCOM APB clock must always be higher than the SERCOM generic clock to support collision detection.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13 Timer Counter (TC)

2.13.1 Flags Synchronization

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround
Successively, clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is properly restored before updating it.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.13.2 Capture Mode / Over consumption

If the Time Counter x (TCx) is in Capture mode (TC.CTRLA.CAPTENx=1) and TC.CTRLA.RUNSTBY=0, the clock source driving GCLK_TCx can be kept running in Standby mode causing extra power consumption.

Workaround
Disable the Time Counter x (TCx) (TC.CTRLA.ENABLE=0) which has a channel configured in Capture mode before going to Standby mode.

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

2.14 True Random Number Generator (TRNG)

2.14.1 Over consumption

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround

Disable the TRNG module twice:

- TRNG > CTRLA.reg = 0;
- TRNG > CTRLA.reg = 0;

Affected Silicon Revisions

Device Family	B						
SAM L10	X						
SAM L11	X						

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001513B):

Note: Corrections in tables, registers, and texts are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No clarifications to report at this time.

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SYST-19IPBJ191 - ERRATA - SAM L10/L11 Family Silicon Errata and Data Sheet Clarification

Affected Catalog Part Numbers(CPN)

ATSAML10D14A-MU
ATSAML10D14A-MUT
ATSAML10D14A-YU
ATSAML10D14A-YUT
ATSAML10D15A-MU
ATSAML10D15A-MUT
ATSAML10D15A-YU
ATSAML10D15A-YUT
ATSAML10D16A-MU
ATSAML10D16A-MUT
ATSAML10D16A-YU
ATSAML10D16A-YUT
ATSAML10E14A-AU
ATSAML10E14A-AUT
ATSAML10E14A-MU
ATSAML10E14A-MUT
ATSAML10E15A-AU
ATSAML10E15A-AUT
ATSAML10E15A-MU
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