Product Change Notification - SYST-21FEDM490

Date:

25 Jun 2018

Product Category:

32-bit PIC Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errat

Notification text:

SYST-21FEDM490

Microchip has released a new DeviceDoc for the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errat of devices. If you are using one of these devices please read the document located at PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errat.

Notification Status: Final

Description of Change: 1.) Updated to include silicon revision B2 2.) Added silicon issue 30. Module: (Security)

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Estimated First Ship Date: 25 Jun 2018
NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachment(s):

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errat

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to change your product/process change notification (PCN) profile please log on to our website at http://www.microchip.com/PCN sign into myMICROCHIP to open the myMICROCHIP home page, then select a profile option from the left navigation bar.

To opt out of future offer or information emails (other than product change notification emails), click here to go to microchipDIRECT and login, then click on the "My account" link, click on "Update profile" and un-check the box that states "Future offers or information about Microchip's products or services."

PIC32MZ EF FAMILY

PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001320E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (B2).

Data Sheet clarifications and corrections (if applicable) start on page 13, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ EF Family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A1	A3	B2
PIC32MZ0512EFE064	0x7201053	0x1	0x3	0x6
PIC32MZ0512EFF064	0x7206053			
PIC32MZ0512EFK064	0x722E053			
PIC32MZ1024EFE064	0x7202053			
PIC32MZ1024EFF064	0x7207053			
PIC32MZ1024EFK064	0x722F053			
PIC32MZ1024EFG064	0x7203053			
PIC32MZ1024EFH064	0x7208053			
PIC32MZ1024EFM064	0x7230053			
PIC32MZ2048EFG064	0x7204053			
PIC32MZ2048EFH064	0x7209053			
PIC32MZ2048EFM064	0x7231053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001320E) for detailed information on Device and Revision IDs for your specific device.

© 2015-2018 Microchip Technology Inc.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)		
		A1	A3	B2
PIC32MZ0512EFE100	0x720B053	0x1	0x3	0x6
PIC32MZ0512EFF100	0x7210053			
PIC32MZ0512EFK100	0x7238053			
PIC32MZ1024EFE100	0x720C053			
PIC32MZ1024EFF100	0x7211053			
PIC32MZ1024EFK100	0x7239053			
PIC32MZ1024EFG100	0x720D053			
PIC32MZ1024EFH100	0x7212053			
PIC32MZ1024EFM100	0x723A053			
PIC32MZ2048EFG100	0x720E053			
PIC32MZ2048EFH100	0x7213053			
PIC32MZ2048EFM100	0x723B053			
PIC32MZ0512EFE124	0x7215053	0x1	0x3	0x6
PIC32MZ0512EFF124	0x721A053			
PIC32MZ0512EFK124	0x7242053			
PIC32MZ1024EFE124	0x7216053			
PIC32MZ1024EFF124	0x721B053			
PIC32MZ1024EFK124	0x7243053			
PIC32MZ1024EFG124	0x7217053			
PIC32MZ1024EFH124	0x721C053			
PIC32MZ1024EFM124	0x7244053			
PIC32MZ2048EFG124	0x7218053			
PIC32MZ2048EFH124	0x721D053			
PIC32MZ2048EFM124	0x7245053			
PIC32MZ0512EFE144	0x721F053	0x1	0x3	0x6
PIC32MZ0512EFF144	0x7224053			
PIC32MZ0512EFK144	0x724C053			
PIC32MZ1024EFE144	0x7220053			
PIC32MZ1024EFF144	0x7225053			
PIC32MZ1024EFK144	0x724D053			
PIC32MZ1024EFG144	0x7221053			
PIC32MZ1024EFH144	0x7226053			
PIC32MZ1024EFM144	0x724E053			
PIC32MZ2048EFG144	0x7222053			
PIC32MZ2048EFH144	0x7227053			
PIC32MZ2048EFM144	0x724F053			

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001320E) for detailed information on Device and Revision IDs for your specific device.

© 2015-2018 Microchip Technology Inc.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Issue	Issue Summary	Affected Revisions(1)		
				A1	A3	B2
Oscillator	Reference Clock	1.	The Reference Clock cannot divide input frequencies greater than 100 MHz.	X	X	
Oscillator	Primary Oscillator Crystal	2.	**Revision A1 Silicon:** A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/OSC2 pins). **Revision A3 Silicon:** The Primary Oscillator has been tested in a normal power-up sequence and supports specific crystal operation.	X	X	X
Oscillator	FRC Tuning	3.	The OSCTUN register only increases the frequency of the FRC.	X		
Secondary Oscillator	Crystal Use	4.	The Secondary Oscillator (SOSC) does not support crystal operation.	X	X	
Power-Saving	PMD bits	5.	Turning off REFCLK through the PMD bits causes unpredictable device behavior.	X	X	
I^2C	—	6.	The I^2C module does not function reliably under certain conditions.	X	X	
UART	Auto-baud	7.	The Auto-baud feature does not function to set the baud rate.	X	X	X
UART	Synchronization	8.	On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.	X	X	X
USB	Suspend Mode	9.	The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.	X	X	X
Power-Saving Modes	Sleep Mode	10.	The device may not exit Sleep mode.	X	X	
ADC	Digital Filters	11.	Using multiple digital filters may result in data not being captured accurately.	X	X	
ADC	Level Trigger	12.	The ADC level trigger will not perform burst conversions in Debug mode.	X	X	
ADC	DNL	13.	In Differential mode, DNL for code 3072 is out of specification.	X	X	X
ADC	Low-voltage Operation	14.	When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.	X	X	X
ADC	Turbo Mode	15.	Turbo mode is not functional.	X	X	X
USB	Resume	16.	The USB module does not support remote wake-up.	X	X	X
Oscillator	External Clock Mode	17.	The EC mode timing specifications for the Primary Oscillator (POSC) are not met.	X		
Temperature Sensor	—	18.	The Temperature Sensor does not function.	X	X	X
ICSP	TDO	19.	The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair.	X	X	X
DMA	PMD bits	20.	Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or the DMA peripheral.	X	X	X
PMP	Status Bits	21.	The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are set as soon as the PMP is turned on in Slave mode (when TTLEN = 1).	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Issue	Issue Summary	Affected Revisions(1)		
				A1	A3	B2
Sleep	IPD	22.	A 3 mA increase occurs during Sleep mode when PB5DIV is disabled.	X	X	X
SQI	RX/TX FIFO	23.	The SQI may continuously receive invalid data or fail to transmit when the SQICLKDIV is used.	X	X	X
POR	GPIO	24.	Whenever VDD is less than VPOR, the I/O pin states may be indeterminate.	X	X	
Crypto	Partial Packet	25.	The cryptographic DMA module does not support partial packet processing.	X	X	X
Crypto	Zero Length Packet	26.	Zero length packets fail to process. The crypto DMA does not support an empty string hash.	X	X	X
SPI	Block Transmission	27.	At the end of a transmission, the SRMT bit can indicate the completion of the transmission for one PBCLK even though the transmission has one block remaining.	X	X	X
SQI	Special Function Registers	28.	The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled after a Reset.	X	X	X
Sleep	Wake-ups	29.	Multiple sleep attempts which occur before the CPU has fully awakened, may stall the CPU until the next reset event.	X	X	X
Security	System Bus Access	30.	The note at the end of the CFGPG register (Register no. 34-10) indicates that the CPU as system bus initiator is controlled within the CPU core is incorrect. The CPU core internal state will not control the CPU system bus initiator permission group.	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

© 2015-2018 Microchip Technology Inc.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B2**).

1. Module: Oscillator

The Reference Module cannot divide input frequencies greater than 100 MHz. Therefore, SYSCLK cannot be divided if the SYSCLK operates at frequencies greater than 100 MHz.

Work around

Instead of using SYSCLK, use PBCLK1 as the input, which is limited to 100 MHz and is synchronized to SYSCLK.

Alternatively, do not divide the SYSCLK and allow the destination peripheral (i.e., SQI, SPI) to divide it as needed. To do this, set the RODIV<14:0> bits and the ROTRIM<8:0> bits to '0'.

Affected Silicon Revisions

A1	A3	B2					
X	X						

2. Module: Oscillator

Revision A1 Silicon: A crystal oscillator cannot be used as an input to the Primary Oscillator (POSC) pins OSC1 and OSC2.

Revision A1 Silicon Work around

Use an external clock or the Internal FRC Oscillator.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

Revision A3 Silicon: The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

Revision A3 Silicon Work around 1

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz, 12 MHz, and 24 MHz when the circuit in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

FIGURE 1: POSC CRYSTAL CIRCUIT

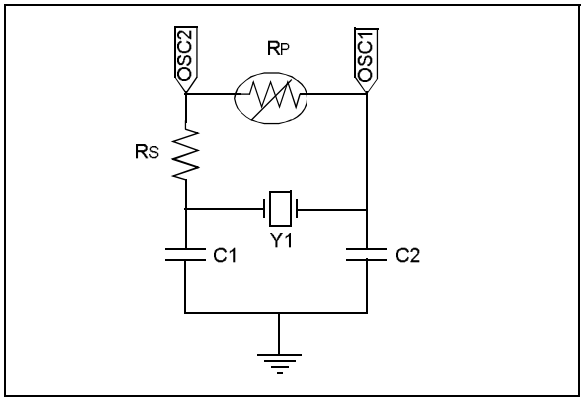

TABLE 3: CRYSTAL SPECIFICATIONS

Crystal Frequency (see Note 1)	Series Resistor (Rs)	POSC Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19>)	POSC Boost Setting POSCBOOST (DEVCFG0<21>)
8 MHz	2 kΩ	'0b00 (GAIN_0)	'0b1 (ON)
12 MHz	1 kΩ	'0b00 (GAIN_0)	'0b1 (ON)
24 MHz	0 kΩ	'0b00 (GAIN_0))	'0b1 (ON)

Note 1: Using any other crystal frequency will require special component selection and characterization.

2: A parallel resistor (RP) should not be used to increase the gain of the POSC.

Revision A3 Silicon Work around 2

Alternatively, use an external clock or the Internal FRC oscillator.

Affected Silicon Revisions

A1	A3	B2					
X							

3. Module: Oscillator

The OSCTUN register only increases the frequency of the FRC, which results in the TUN<5:0> bits (OSCTUN<5:0>) functioning as follows:

TUN<5:0>: FRC Oscillator Tuning bits

`111111` = Center frequency +4%

`111110` =

•
•
•

`000001` =

`000000` = Center frequency; Oscillator runs at nominal frequency (8 MHz)

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X							

4. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins SOSCI and SOSCO.

Silicon Work around

Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

Affected Silicon Revisions

A1	A3	B2					
X	X						

5. Module: Power-Saving

Turning off the REFCLK modules through the PMD bits causes unpredictable behavior.

Work around

None. Do not disable the REFCLK modules through the PMD bits.

Affected Silicon Revisions

A1	A3	B2					
X	X						

© 2015-2018 Microchip Technology Inc.

6. Module: I²C

Indeterminate I²C module behavior may result when data rates > 100 kHz and/or continuous sequential data transfers > 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  False Master Bus Collision Detect (Master-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).
- **False Error Condition 2:**
  Receive Overflow (Master or Slave modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).
- **False Error Condition 3:**
  Suspended I²C Module Operations (Master or Slave modes) – I²C transactions in progress are inadvertently suspended without error indications.

Note:	All three false error conditions are recoverable in software.

Revision A1 Silicon Work around 1

False Error Condition 1:

Clear the Master Bus Collision Detect (BCL bit (I2CxSTAT<10>), after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P bit (I2CxSTAT<4>) to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I²C bus is free, the software can resume communication by asserting a new Start condition.

False Error Condition 2:

Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

False Error Condition 3:

First, initialize a Timer to slightly greater than the worst case I²C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I²C transaction.

Then, during the Timer interrupt (meaning the I²C transaction has timed out), disable the I²C module by setting the ON bit (I2CxCON<15>) = `0`. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Then, re-enable the I²C module by setting the ON bit = `1` and resume normal operation.

Revision A1 Silicon Work around 2

Instead of using the hardware I²C module, use a software “bit-bang” implementation.

Revision A3 Silicon Work around

The work arounds described for revision A1 silicon will also work for silicon revision A3, with the exception of I2C3, as I2C3 must use a software “bit-bang” implementation.

Affected Silicon Revisions

A1	A3	B2					
X	X						

7. Module: UART

The UART automatic baud rate feature is intended to set the baud rate during run-time based on external data input. However, this feature does not function.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

8. Module: UART

During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:

Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:

If avoiding RX FIFO overruns is not possible, implement an ACK/NAK software handshake protocol to repeat lost packet transfers after restoring the UART synchronization.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

9. Module: USB

The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.

Work around

Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to '0'.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

10. Module: Power-Saving Modes

The device may not exit Sleep mode when Flash is powered down through the FSLEEP bit in the DEVCFG0/ADEVCFG0 Configuration register.

Work around

Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 Configuration register.

Affected Silicon Revisions

A1	A3	B2					
X	X						

11. Module: ADC

When using multiple digital filters, the filters may not capture data correctly when the assigned data sources are ready at the same time.

Work around

Only one digital filter may be used at a time.

Affected Silicon Revisions

A1	A3	B2					
X	X						

12. Module: ADC

The ADC level trigger will not perform burst conversions in Debug mode.

Work around

Do not use Debug mode with the ADC level trigger.

Affected Silicon Revisions

A1	A3	B2					
X	X						

13. Module: ADC

In Differential mode, code 3072 has a DNL of +3.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

© 2015-2018 Microchip Technology Inc.

14. Module: ADC

When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

15. Module: ADC

Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

16. Module: USB

The USB module does not support remote wakeup through the USBRIE bit (USBCRCON<1>).

Work around

None.

USB descriptors must inform the host that the device does not support remote wake-up.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

17. Module: Oscillator

The Primary Oscillator in EC mode only functions up to 24 MHz

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X							

18. Module: Temperature Sensor

The temperature sensor does not function.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

19. Module: ICSP

Regardless of other functions shared on the TDO pin, the TDO function becomes an active output and toggles while programming on any ICSP PGECx/PGEDx pair.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X	x					

20. Module: DMA

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or the DMA peripheral.

Work around

Use the ON bit (DMACON<15>) to enable or disable the DMA globally, or use the CHEN bit (DCHxCON<7>) to enable or disable the individual channels.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

21. Module: PMP

The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are set as soon as the PMP is turned on in Slave mode (when TTLEN = 1).

Work around

After PMP initial initialization is complete, and before the PMP and interrupts are enabled, clear the TTLEN bits in user software.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

22. Module: Sleep

If the ON bit (PB5DIV<15>) = 0 and PBCLK5 is disabled, a 3mA increase in Sleep IPD current occurs.

Work around

Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

23. Module: SQI

When the SQI clock divider is used (by setting CLKDIV ≠ 0), any one of the following error conditions may occur on some of the devices, which are depending on the DDRMODE setting:

- With DDRMODE = 0, the SQI fails in reception only.
- With DDRMODE = 1, the SQI may fail in both reception and transmission.

Work around

Set the CLKDIV bits to '0' and use the REFCLK02 as the SQI base clock.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

24. Module: POR

Whenever VDD is less than VPOR, the I/O pin I/O State and logic level may be indeterminate.

Work around

None.

Affected Silicon Revisions

A1	A3	B2					
X	X						

25. Module: Crypto

Attempting to run part of a cryptographic packet through the peripheral may not result in a usable initial vector for continuing the cryptographic operation.

Work around

Do not interrupt a cryptographic operation with another, instead, always process a hash completely.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

26. Module: Crypto

Using the crypto DMA on an empty hash string will cause the peripheral to time out and not return a valid hash.

Work around

Use the fixed known hash of the empty string.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

27. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL = 0).

Work around

Use the interrupt notification rather than polling the SRMT bit to determine when a transmission has completed.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

© 2015-2018 Microchip Technology Inc.

28. Module: SQI

After a Reset, the first access to the SQI SFRs must be a write. A read access can stall the CPU, requiring a Reset to clear. The typical initialization code may include a write to the SQIEN bit. The SQI1CFGbits.SQIEN=0 instruction is a read, modify, and write sequence. After a Reset, this sequence will stall the CPU. Similarly, only reading the SQI SFRs will also stall the CPU if that read is the first access after a Reset.

Work around

Be sure to enable the REFCLKO2 before reading the registers from the SQI peripheral. Do not use the "SQI1CFGbits.SQIEN=0" instruction to enable the SQI, instead use the "SQI1CFGCLR= "_SQICFG_SQIEN_MASK" instruction.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

29. Module: Sleep

Multiple sleep attempts (WAIT instruction with OSCCON<4>=1) which occur within 20 µs of a wake event, before the CPU has fully awakened, can cause the CPU to stall until a Power-on Reset (POR) event.

Work around

Be sure that at least 20 µs elapse before attempting to put the CPU to sleep (WAIT instruction with OSCCON<4>=1) after it awakens from a previous sleep.

Affected Silicon Revisions

A1	A3	B2					
X	X	X					

30. Module: Security

The note at the end of the CFGPG register (Register no. 34-10) indicates that the CPU as a system bus initiator is controlled within the CPU core is incorrect. The CPU core internal state will not control the CPU system bus initiator permission group.

Work around

Use the CFGPG register reserved bits <1:0> to control the permission group ID of the CPU as a system bus initiator.

11 = Initiator is assigned to permission group 3

10 = Initiator is assigned to permission group 2

01 = Initiator is assigned to permission group 1

00 = Initiator is assigned to permission group 0

Also, the reserved bits <:14:12> of the DEVCFG0 and ADEVCFG0 registers can be used to control the permission group ID of the CPU in Debug mode, as in:

- 1xx = Allow CPU access to permission group 2 permission regions
- x1x = Allow CPU access to permission group 1 permission regions
- xx1 = Allow CPU access to permission group 0 permission regions
- 0xx = Deny CPU access to permission group 2 permission regions
- x0x = Deny CPU access to permission group 1 permission regions
- xx0 = Deny CPU access to permission group 0 permission regions

When the CPU is in Debug mode and CFGPG<1:0> are set to a denied permission group as defined by the DEVCFG0<14:12>, the transaction request is assigned Group 3 permissions.

Affected Silicon Revisions

A1	A3	B2					
X	X						

© 2015-2018 Microchip Technology Inc.

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001320E):

Note:	Corrections in tables are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No issues to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (7/2015)

Initial release of this document issued for revision A1 silicon, which includes silicon issues 1. Module: (Oscillator), 2. Module: (Oscillator), 3. Module: (Oscillator), 4. Module: (Secondary Oscillator), 5. Module: (Power-Saving), 6. Module: (I^2C), 7. Module: (UART), 8. Module: (UART), 9. Module: (USB), and Power-Saving Modes.

Rev B Document (4/2016)

Added silicon issues 11. Module: (ADC) and 12. Module: (ADC).

Updated silicon issues 2. Module: (Oscillator) and 10. Module: (Power-Saving Modes).

Rev C Document (7/2016)

Updated to include silicon revision A3.

Updated silicon issues 2. Module: (Oscillator), 6. Module: (I^2C), and 11. Module: (ADC).

Added silicon issues 13. Module: (ADC), 14. Module: (ADC), 15. Module: (ADC), and 16. Module: (USB).

Added data sheet clarifications 1. Module: (Resets) and 2. Module: (Interrupt Controller).

Rev D Document (9/2016)

Updated Figure 1 and Table 3 in silicon issue 2. Module: (Oscillator).

Added silicon issues 17. Module: (Oscillator) and 18. Module: (Temperature Sensor).

Added data sheet clarification 3. Module: (External Clock Timing Requirements).

Rev E Document (3/2018)

Internal release, minor content edits gone into this release.

Rev F Document (4/2018)

Added silicon issues: 19. Module: (ICSP), 20. Module: (DMA), 21. Module: (PMP), 22. Module: (Sleep), 23. Module: (SQI), 24. Module: (POR), 25. Module: (Crypto), 26. Module: (Crypto), 27. Module: (SPI), 28. Module: (SQI), and 29. Module: (Sleep).

All data sheet clarifications were removed.

Rev G Document (6/2018)

Updated to include silicon revision B2.

Added silicon issue **30. Module: (Security)**.

© 2015-2018 Microchip Technology Inc.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

ISO/TS 16949

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, memBrain, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2018, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-3202-9

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

© 2015-2018 Microchip Technology Inc.

SYST-21FEDM490 - ERRATA - PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silic

Affected Catalog Part Numbers(CPN)

PIC32MZ0512EFE064-E/MR
PIC32MZ0512EFE064-E/MRA21
PIC32MZ0512EFE064-E/PT
PIC32MZ0512EFE064-I/MR
PIC32MZ0512EFE064-I/PT
PIC32MZ0512EFE064-I/PTA21
PIC32MZ0512EFE064-I/PTA22
PIC32MZ0512EFE064T-E/MR
PIC32MZ0512EFE064T-E/MRA21
PIC32MZ0512EFE064T-E/PT
PIC32MZ0512EFE064T-I/MR
PIC32MZ0512EFE064T-I/PT
PIC32MZ0512EFE064T-I/PTA21
PIC32MZ0512EFE064T-I/PTA22
PIC32MZ0512EFE100-E/GJX
PIC32MZ0512EFE100-E/PF
PIC32MZ0512EFE100-E/PT
PIC32MZ0512EFE100-I/GJX
PIC32MZ0512EFE100-I/PF
PIC32MZ0512EFE100-I/PT
PIC32MZ0512EFE100T-E/GJX
PIC32MZ0512EFE100T-E/PF
PIC32MZ0512EFE100T-E/PT
PIC32MZ0512EFE100T-I/GJX
PIC32MZ0512EFE100T-I/PF
PIC32MZ0512EFE100T-I/PT
PIC32MZ0512EFE124-E/TL
PIC32MZ0512EFE124-I/TL
PIC32MZ0512EFE124E-E/TL
PIC32MZ0512EFE124T-E/TL
PIC32MZ0512EFE124T-I/TL
PIC32MZ0512EFE144-E/JWX
PIC32MZ0512EFE144-E/PH
PIC32MZ0512EFE144-E/PL
PIC32MZ0512EFE144-E/TR
PIC32MZ0512EFE144-I/JWX
PIC32MZ0512EFE144-I/PH
PIC32MZ0512EFE144-I/PL
PIC32MZ0512EFE144-I/TR
PIC32MZ0512EFE144T-E/JWX
PIC32MZ0512EFE144T-E/PH
PIC32MZ0512EFE144T-E/PL

PIC32MZ0512EFE144T-I/JWX
PIC32MZ0512EFE144T-I/PH
PIC32MZ0512EFE144T-I/PL
PIC32MZ0512EFF064-E/MR
PIC32MZ0512EFF064-E/MRV01
PIC32MZ0512EFF064-E/PT
PIC32MZ0512EFF064-I/MR
PIC32MZ0512EFF064-I/PT
PIC32MZ0512EFF064-I/PTVAO
PIC32MZ0512EFF064T-E/MR
PIC32MZ0512EFF064T-E/MRV01
PIC32MZ0512EFF064T-E/PT
PIC32MZ0512EFF064T-I/MR
PIC32MZ0512EFF064T-I/PT
PIC32MZ0512EFF100-E/GJX
PIC32MZ0512EFF100-E/PF
PIC32MZ0512EFF100-E/PT
PIC32MZ0512EFF100-I/GJX
PIC32MZ0512EFF100-I/PF
PIC32MZ0512EFF100-I/PT
PIC32MZ0512EFF100T-E/GJX
PIC32MZ0512EFF100T-E/PF
PIC32MZ0512EFF100T-E/PT
PIC32MZ0512EFF100T-I/GJX
PIC32MZ0512EFF100T-I/PF
PIC32MZ0512EFF100T-I/PT
PIC32MZ0512EFF124-E/TL
PIC32MZ0512EFF124-I/TL
PIC32MZ0512EFF124-I/TLN21
PIC32MZ0512EFF124T-E/TL
PIC32MZ0512EFF124T-I/TL
PIC32MZ0512EFF124T-I/TLN21
PIC32MZ0512EFF144-E/JWX
PIC32MZ0512EFF144-E/PH
PIC32MZ0512EFF144-E/PL
PIC32MZ0512EFF144-E/TR
PIC32MZ0512EFF144-I/JWX
PIC32MZ0512EFF144-I/PH
PIC32MZ0512EFF144-I/PL
PIC32MZ0512EFF144-I/TR
PIC32MZ0512EFF144T-E/JWX
PIC32MZ0512EFF144T-E/PH
PIC32MZ0512EFF144T-E/PL
PIC32MZ0512EFF144T-I/JWX
PIC32MZ0512EFF144T-I/PH
PIC32MZ0512EFF144T-I/PL
PIC32MZ0512EFK064-E/MR

PIC32MZ0512EFK064-E/PT
PIC32MZ0512EFK064-I/MR
PIC32MZ0512EFK064-I/PT
PIC32MZ0512EFK064T-E/MR
PIC32MZ0512EFK064T-E/PT
PIC32MZ0512EFK064T-I/MR
PIC32MZ0512EFK064T-I/PT
PIC32MZ0512EFK100-E/GJX
PIC32MZ0512EFK100-E/PF
PIC32MZ0512EFK100-E/PT
PIC32MZ0512EFK100-I/GJX
PIC32MZ0512EFK100-I/PF
PIC32MZ0512EFK100-I/PT
PIC32MZ0512EFK100T-E/GJX
PIC32MZ0512EFK100T-E/PF
PIC32MZ0512EFK100T-E/PT
PIC32MZ0512EFK100T-I/GJX
PIC32MZ0512EFK100T-I/PF
PIC32MZ0512EFK100T-I/PT
PIC32MZ0512EFK124-E/TL
PIC32MZ0512EFK124-I/TL
PIC32MZ0512EFK124T-E/TL
PIC32MZ0512EFK124T-I/TL
PIC32MZ0512EFK144-E/JWX
PIC32MZ0512EFK144-E/PH
PIC32MZ0512EFK144-E/PL
PIC32MZ0512EFK144-E/TR
PIC32MZ0512EFK144-I/JWX
PIC32MZ0512EFK144-I/PH
PIC32MZ0512EFK144-I/PL
PIC32MZ0512EFK144-I/TR
PIC32MZ0512EFK144T-E/JWX
PIC32MZ0512EFK144T-E/PH
PIC32MZ0512EFK144T-E/PL
PIC32MZ0512EFK144T-I/JWX
PIC32MZ0512EFK144T-I/PH
PIC32MZ0512EFK144T-I/PL
PIC32MZ1024EFE064-E/MR
PIC32MZ1024EFE064-E/PT
PIC32MZ1024EFE064-I/MR
PIC32MZ1024EFE064-I/PT
PIC32MZ1024EFE064T-E/MR
PIC32MZ1024EFE064T-E/PT
PIC32MZ1024EFE064T-I/MR
PIC32MZ1024EFE064T-I/PT
PIC32MZ1024EFE100-E/GJX
PIC32MZ1024EFE100-E/PF

PIC32MZ1024EFE100-E/PT
PIC32MZ1024EFE100-I/GJX
PIC32MZ1024EFE100-I/PF
PIC32MZ1024EFE100-I/PT
PIC32MZ1024EFE100-I/PTE21
PIC32MZ1024EFE100T-E/GJX
PIC32MZ1024EFE100T-E/PF
PIC32MZ1024EFE100T-E/PT
PIC32MZ1024EFE100T-I/GJX
PIC32MZ1024EFE100T-I/PF
PIC32MZ1024EFE100T-I/PT
PIC32MZ1024EFE124-E/TL
PIC32MZ1024EFE124-I/TL
PIC32MZ1024EFE124T-E/TL
PIC32MZ1024EFE124T-I/TL
PIC32MZ1024EFE144-E/JWX
PIC32MZ1024EFE144-E/PH
PIC32MZ1024EFE144-E/PL
PIC32MZ1024EFE144-E/TR
PIC32MZ1024EFE144-I/JWX
PIC32MZ1024EFE144-I/PH
PIC32MZ1024EFE144-I/PL
PIC32MZ1024EFE144-I/TR
PIC32MZ1024EFE144T-E/JWX
PIC32MZ1024EFE144T-E/PH
PIC32MZ1024EFE144T-E/PL
PIC32MZ1024EFE144T-I/JWX
PIC32MZ1024EFE144T-I/PH
PIC32MZ1024EFE144T-I/PL
PIC32MZ1024EFF064-E/MR
PIC32MZ1024EFF064-E/PT
PIC32MZ1024EFF064-I/MR
PIC32MZ1024EFF064-I/PT
PIC32MZ1024EFF064-I/PTF21
PIC32MZ1024EFF064T-E/MR
PIC32MZ1024EFF064T-E/PT
PIC32MZ1024EFF064T-I/MR
PIC32MZ1024EFF064T-I/PT
PIC32MZ1024EFF064T-I/PTF21
PIC32MZ1024EFF100-E/GJX
PIC32MZ1024EFF100-E/PF
PIC32MZ1024EFF100-E/PT
PIC32MZ1024EFF100-I/GJX
PIC32MZ1024EFF100-I/PF
PIC32MZ1024EFF100-I/PT
PIC32MZ1024EFF100T-E/GJX
PIC32MZ1024EFF100T-E/PF

PIC32MZ1024EFF100T-E/PT
PIC32MZ1024EFF100T-I/GJX
PIC32MZ1024EFF100T-I/PF
PIC32MZ1024EFF100T-I/PT
PIC32MZ1024EFF124-E/TL
PIC32MZ1024EFF124-I/TL
PIC32MZ1024EFF124T-E/TL
PIC32MZ1024EFF124T-I/TL
PIC32MZ1024EFF144-E/JWX
PIC32MZ1024EFF144-E/PH
PIC32MZ1024EFF144-E/PL
PIC32MZ1024EFF144-E/TR
PIC32MZ1024EFF144-I/JWX
PIC32MZ1024EFF144-I/PH
PIC32MZ1024EFF144-I/PL
PIC32MZ1024EFF144-I/TR
PIC32MZ1024EFF144T-E/JWX
PIC32MZ1024EFF144T-E/PH
PIC32MZ1024EFF144T-E/PL
PIC32MZ1024EFF144T-I/JWX
PIC32MZ1024EFF144T-I/PH
PIC32MZ1024EFF144T-I/PL
PIC32MZ1024EFG064-E/MR
PIC32MZ1024EFG064-E/MRVAO
PIC32MZ1024EFG064-E/PT
PIC32MZ1024EFG064-I/MR
PIC32MZ1024EFG064-I/PT
PIC32MZ1024EFG064-I/PTN22
PIC32MZ1024EFG064-I/PTRB2
PIC32MZ1024EFG064T-E/MR
PIC32MZ1024EFG064T-E/MRVAO
PIC32MZ1024EFG064T-E/PT
PIC32MZ1024EFG064T-I/MR
PIC32MZ1024EFG064T-I/PT
PIC32MZ1024EFG064T-I/PTN22
PIC32MZ1024EFG064T-I/PTRB2
PIC32MZ1024EFG100-250I/PT
PIC32MZ1024EFG100-E/GJX
PIC32MZ1024EFG100-E/PF
PIC32MZ1024EFG100-E/PT
PIC32MZ1024EFG100-I/GJX
PIC32MZ1024EFG100-I/PF
PIC32MZ1024EFG100-I/PT
PIC32MZ1024EFG100-I/PTG21
PIC32MZ1024EFG100T-250I/PT
PIC32MZ1024EFG100T-E/GJX
PIC32MZ1024EFG100T-E/PF

PIC32MZ1024EFG100T-E/PT
PIC32MZ1024EFG100T-I/GJX
PIC32MZ1024EFG100T-I/PF
PIC32MZ1024EFG100T-I/PT
PIC32MZ1024EFG124-E/TL
PIC32MZ1024EFG124-I/TL
PIC32MZ1024EFG124T-E/TL
PIC32MZ1024EFG124T-I/TL
PIC32MZ1024EFG144-E/JWX
PIC32MZ1024EFG144-E/PH
PIC32MZ1024EFG144-E/PL
PIC32MZ1024EFG144-E/TR
PIC32MZ1024EFG144-I/JWX
PIC32MZ1024EFG144-I/PH
PIC32MZ1024EFG144-I/PL
PIC32MZ1024EFG144-I/PLG21
PIC32MZ1024EFG144-I/TR
PIC32MZ1024EFG144T-E/JWX
PIC32MZ1024EFG144T-E/PH
PIC32MZ1024EFG144T-E/PL
PIC32MZ1024EFG144T-I/JWX
PIC32MZ1024EFG144T-I/PH
PIC32MZ1024EFG144T-I/PL
PIC32MZ1024EFH064-E/MR
PIC32MZ1024EFH064-E/PT
PIC32MZ1024EFH064-I/MR
PIC32MZ1024EFH064-I/PT
PIC32MZ1024EFH064-I/PTH21
PIC32MZ1024EFH064T-E/MR
PIC32MZ1024EFH064T-E/PT
PIC32MZ1024EFH064T-I/MR
PIC32MZ1024EFH064T-I/PT
PIC32MZ1024EFH064T-I/PTH21
PIC32MZ1024EFH100-E/GJX
PIC32MZ1024EFH100-E/PF
PIC32MZ1024EFH100-E/PT
PIC32MZ1024EFH100-I/GJX
PIC32MZ1024EFH100-I/PF
PIC32MZ1024EFH100-I/PT
PIC32MZ1024EFH100-I/PTH21
PIC32MZ1024EFH100T-E/GJX
PIC32MZ1024EFH100T-E/PF
PIC32MZ1024EFH100T-E/PT
PIC32MZ1024EFH100T-I/GJX
PIC32MZ1024EFH100T-I/PF
PIC32MZ1024EFH100T-I/PT
PIC32MZ1024EFH100T-I/PTH21

PIC32MZ1024EFH100T-I/PTVAO
PIC32MZ1024EFH124-E/TL
PIC32MZ1024EFH124-I/TL
PIC32MZ1024EFH124T-E/TL
PIC32MZ1024EFH124T-I/TL
PIC32MZ1024EFH144-E/JWX
PIC32MZ1024EFH144-E/PH
PIC32MZ1024EFH144-E/PL
PIC32MZ1024EFH144-E/TR
PIC32MZ1024EFH144-I/JWX
PIC32MZ1024EFH144-I/PH
PIC32MZ1024EFH144-I/PL
PIC32MZ1024EFH144-I/TR
PIC32MZ1024EFH144T-E/JWX
PIC32MZ1024EFH144T-E/PH
PIC32MZ1024EFH144T-E/PL
PIC32MZ1024EFH144T-I/JWX
PIC32MZ1024EFH144T-I/PH
PIC32MZ1024EFH144T-I/PL
PIC32MZ1024EFK064-E/MR
PIC32MZ1024EFK064-E/PT
PIC32MZ1024EFK064-I/MR
PIC32MZ1024EFK064-I/PT
PIC32MZ1024EFK064T-E/MR
PIC32MZ1024EFK064T-E/PT
PIC32MZ1024EFK064T-I/MR
PIC32MZ1024EFK064T-I/PT
PIC32MZ1024EFK100-E/GJX
PIC32MZ1024EFK100-E/PF
PIC32MZ1024EFK100-E/PT
PIC32MZ1024EFK100-I/GJX
PIC32MZ1024EFK100-I/PF
PIC32MZ1024EFK100-I/PT
PIC32MZ1024EFK100-I/PTK21
PIC32MZ1024EFK100T-E/GJX
PIC32MZ1024EFK100T-E/PF
PIC32MZ1024EFK100T-E/PT
PIC32MZ1024EFK100T-I/GJX
PIC32MZ1024EFK100T-I/PF
PIC32MZ1024EFK100T-I/PT
PIC32MZ1024EFK124-E/TL
PIC32MZ1024EFK124-I/TL
PIC32MZ1024EFK124T-E/TL
PIC32MZ1024EFK124T-I/TL
PIC32MZ1024EFK144-E/JWX
PIC32MZ1024EFK144-E/PH
PIC32MZ1024EFK144-E/PL

PIC32MZ1024EFK144-E/TR
PIC32MZ1024EFK144-I/JWX
PIC32MZ1024EFK144-I/PH
PIC32MZ1024EFK144-I/PL
PIC32MZ1024EFK144-I/TR
PIC32MZ1024EFK144T-E/JWX
PIC32MZ1024EFK144T-E/PH
PIC32MZ1024EFK144T-E/PL
PIC32MZ1024EFK144T-I/JWX
PIC32MZ1024EFK144T-I/PH
PIC32MZ1024EFK144T-I/PL
PIC32MZ1024EFM064-E/MR
PIC32MZ1024EFM064-E/PT
PIC32MZ1024EFM064-I/MR
PIC32MZ1024EFM064-I/PT
PIC32MZ1024EFM064T-E/MR
PIC32MZ1024EFM064T-E/PT
PIC32MZ1024EFM064T-I/MR
PIC32MZ1024EFM064T-I/PT
PIC32MZ1024EFM100-E/GJX
PIC32MZ1024EFM100-E/PF
PIC32MZ1024EFM100-E/PT
PIC32MZ1024EFM100-I/GJX
PIC32MZ1024EFM100-I/PF
PIC32MZ1024EFM100-I/PT
PIC32MZ1024EFM100T-E/GJX
PIC32MZ1024EFM100T-E/PF
PIC32MZ1024EFM100T-E/PT
PIC32MZ1024EFM100T-I/GJX
PIC32MZ1024EFM100T-I/PF
PIC32MZ1024EFM100T-I/PT
PIC32MZ1024EFM124-E/TL
PIC32MZ1024EFM124-I/TL
PIC32MZ1024EFM124T-E/TL
PIC32MZ1024EFM124T-I/TL
PIC32MZ1024EFM144-E/JWX
PIC32MZ1024EFM144-E/PH
PIC32MZ1024EFM144-E/PL
PIC32MZ1024EFM144-E/TR
PIC32MZ1024EFM144-I/JWX
PIC32MZ1024EFM144-I/PH
PIC32MZ1024EFM144-I/PL
PIC32MZ1024EFM144-I/TR
PIC32MZ1024EFM144T-E/JWX
PIC32MZ1024EFM144T-E/PH
PIC32MZ1024EFM144T-E/PL
PIC32MZ1024EFM144T-I/JWX

PIC32MZ1024EFM144T-I/PH
PIC32MZ1024EFM144T-I/PL
PIC32MZ2048EFG064-E/MR
PIC32MZ2048EFG064-E/PT
PIC32MZ2048EFG064-I/MR
PIC32MZ2048EFG064-I/PT
PIC32MZ2048EFG064T-E/MR
PIC32MZ2048EFG064T-E/PT
PIC32MZ2048EFG064T-I/MR
PIC32MZ2048EFG064T-I/PT
PIC32MZ2048EFG100-E/GJX
PIC32MZ2048EFG100-E/PF
PIC32MZ2048EFG100-E/PT
PIC32MZ2048EFG100-I/GJX
PIC32MZ2048EFG100-I/PF
PIC32MZ2048EFG100-I/PT
PIC32MZ2048EFG100-I/PTL21
PIC32MZ2048EFG100-I/PTL22
PIC32MZ2048EFG100T-E/GJX
PIC32MZ2048EFG100T-E/PF
PIC32MZ2048EFG100T-E/PT
PIC32MZ2048EFG100T-I/GJX
PIC32MZ2048EFG100T-I/PF
PIC32MZ2048EFG100T-I/PT
PIC32MZ2048EFG100T-I/PTL22
PIC32MZ2048EFG124-E/TL
PIC32MZ2048EFG124-I/TL
PIC32MZ2048EFG124T-E/TL
PIC32MZ2048EFG124T-I/TL
PIC32MZ2048EFG144-E/JWX
PIC32MZ2048EFG144-E/PH
PIC32MZ2048EFG144-E/PL
PIC32MZ2048EFG144-E/TR
PIC32MZ2048EFG144-I/JWX
PIC32MZ2048EFG144-I/PH
PIC32MZ2048EFG144-I/PHL21
PIC32MZ2048EFG144-I/PL
PIC32MZ2048EFG144-I/TR
PIC32MZ2048EFG144T-E/JWX
PIC32MZ2048EFG144T-E/PH
PIC32MZ2048EFG144T-E/PL
PIC32MZ2048EFG144T-I/JWX
PIC32MZ2048EFG144T-I/PH
PIC32MZ2048EFG144T-I/PHL21
PIC32MZ2048EFG144T-I/PL
PIC32MZ2048EFH064-250I/MR
PIC32MZ2048EFH064-250I/PT

PIC32MZ2048EFH064-250I/PTC21
PIC32MZ2048EFH064-E/MR
PIC32MZ2048EFH064-E/PT
PIC32MZ2048EFH064-I/MR
PIC32MZ2048EFH064-I/PT
PIC32MZ2048EFH064-I/PTREL
PIC32MZ2048EFH064-I/PTV02
PIC32MZ2048EFH064T-250I/MR
PIC32MZ2048EFH064T-250I/PT
PIC32MZ2048EFH064T-250I/PTC21
PIC32MZ2048EFH064T-E/MR
PIC32MZ2048EFH064T-E/PT
PIC32MZ2048EFH064T-I/MR
PIC32MZ2048EFH064T-I/PT
PIC32MZ2048EFH100-250I/GJX
PIC32MZ2048EFH100-250I/PF
PIC32MZ2048EFH100-250I/PT
PIC32MZ2048EFH100-E/GJX
PIC32MZ2048EFH100-E/PF
PIC32MZ2048EFH100-E/PT
PIC32MZ2048EFH100-I/GJX
PIC32MZ2048EFH100-I/PF
PIC32MZ2048EFH100-I/PFM21
PIC32MZ2048EFH100-I/PT
PIC32MZ2048EFH100-I/PTM21
PIC32MZ2048EFH100T-250I/GJX
PIC32MZ2048EFH100T-250I/PF
PIC32MZ2048EFH100T-250I/PT
PIC32MZ2048EFH100T-E/GJX
PIC32MZ2048EFH100T-E/PF
PIC32MZ2048EFH100T-E/PT
PIC32MZ2048EFH100T-I/GJX
PIC32MZ2048EFH100T-I/PF
PIC32MZ2048EFH100T-I/PT
PIC32MZ2048EFH124-E/TL
PIC32MZ2048EFH124-I/TL
PIC32MZ2048EFH124T-E/TL
PIC32MZ2048EFH124T-I/TL
PIC32MZ2048EFH144-250I/JWX
PIC32MZ2048EFH144-250I/PH
PIC32MZ2048EFH144-250I/PL
PIC32MZ2048EFH144-E/JWX
PIC32MZ2048EFH144-E/PH
PIC32MZ2048EFH144-E/PL
PIC32MZ2048EFH144-E/TR
PIC32MZ2048EFH144-I/JWX
PIC32MZ2048EFH144-I/PH

PIC32MZ2048EFH144-I/PHM21
PIC32MZ2048EFH144-I/PL
PIC32MZ2048EFH144-I/TR
PIC32MZ2048EFH144T-250I/JWX
PIC32MZ2048EFH144T-250I/PH
PIC32MZ2048EFH144T-250I/PL
PIC32MZ2048EFH144T-E/JWX
PIC32MZ2048EFH144T-E/PH
PIC32MZ2048EFH144T-E/PL
PIC32MZ2048EFH144T-I/JWX
PIC32MZ2048EFH144T-I/PH
PIC32MZ2048EFH144T-I/PL
PIC32MZ2048EFM064-E/MR
PIC32MZ2048EFM064-E/PT
PIC32MZ2048EFM064-I/MR
PIC32MZ2048EFM064-I/PT
PIC32MZ2048EFM064-I/PTN21
PIC32MZ2048EFM064T-E/MR
PIC32MZ2048EFM064T-E/PT
PIC32MZ2048EFM064T-I/MR
PIC32MZ2048EFM064T-I/PT
PIC32MZ2048EFM064T-I/PTN21
PIC32MZ2048EFM100-E/GJX
PIC32MZ2048EFM100-E/PF
PIC32MZ2048EFM100-E/PT
PIC32MZ2048EFM100-I/GJX
PIC32MZ2048EFM100-I/PF
PIC32MZ2048EFM100-I/PT
PIC32MZ2048EFM100-I/PTBR2
PIC32MZ2048EFM100-I/PTN21
PIC32MZ2048EFM100T-E/GJX
PIC32MZ2048EFM100T-E/PF
PIC32MZ2048EFM100T-E/PT
PIC32MZ2048EFM100T-I/GJX
PIC32MZ2048EFM100T-I/PF
PIC32MZ2048EFM100T-I/PT
PIC32MZ2048EFM100T-I/PTBR2
PIC32MZ2048EFM100T-I/PTN21
PIC32MZ2048EFM124-E/TL
PIC32MZ2048EFM124-I/TL
PIC32MZ2048EFM124T-E/TL
PIC32MZ2048EFM124T-I/TL
PIC32MZ2048EFM144-E/JWX
PIC32MZ2048EFM144-E/PH
PIC32MZ2048EFM144-E/PL
PIC32MZ2048EFM144-E/TR
PIC32MZ2048EFM144-I/JWX

PIC32MZ2048EFM144-I/PH
PIC32MZ2048EFM144-I/PHN21
PIC32MZ2048EFM144-I/PHN22
PIC32MZ2048EFM144-I/PHN23
PIC32MZ2048EFM144-I/PL
PIC32MZ2048EFM144-I/TR
PIC32MZ2048EFM144T-E/JWX
PIC32MZ2048EFM144T-E/PH
PIC32MZ2048EFM144T-E/PL
PIC32MZ2048EFM144T-I/JWX
PIC32MZ2048EFM144T-I/PH
PIC32MZ2048EFM144T-I/PHN21
PIC32MZ2048EFM144T-I/PHN22
PIC32MZ2048EFM144T-I/PL