Product / Process Change Notification

N° 2018-013-A

Dear Customer,

Please find attached our INFINEON Technologies PCN:

Capacity Extension by Introduction of 300mm Wafer Diameter for Dedicated OptiMOS™ Products at Infineon Technologies Dresden, Germany & Harmonization of Bill of Material (BoM)

Important information for your attention:

- Please respond to this PCN by indicating your decision on the approval form, sign it and return to your sales partner before **27th July 2018**.
- Infineon aligns with the widely-recognized JEDEC STANDARD **"JESD46",** which stipulates: **"Lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change."**

Your prompt reply will help Infineon Technologies to assure a smooth and well executed transition. If Infineon does not hear from your side by the due date, we will assume your full acceptance to this proposed change and its implementation.

Your attention and response to this matter is greatly appreciated.

Infineon Technologies AG
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Chairman of the Supervisory Board: Dr. Eckart Sünner
Management Board: Dr. Reinhard Ploss (CEO), Dominik Asam, Dr. Helmut Gassel, Jochen Hanebeck
Registered Office: Neubiberg Commercial Register
Amtsgericht München HRB 126492

Product / Process Change Notification

N° 2018-013-A

▸ Products affected:

Please refer to attached affected product list 1_cip18013_a.xlsx

▸ Detailed Change Information:

Subject:

(a) Introduction of 300mm wafer diameter at Infineon Technologies Dresden GmbH.

(b) Standardization of pad design and metallization process

(c) Standardization of mould compound for TDSON-8 package

(d) Standardization of gate wire bond for TDSON-8 package

Reason:

(a) Next phase of Front End capacity expansion by introduction of 300mm wafer diameter to support continuous increasing customer demand.

(b), (c), (d) Standardization of bill of material (BoM) allows Infineon to improve efficiency & flexibility in the manufacturing environment by significant complexity reduction within the whole production chain.

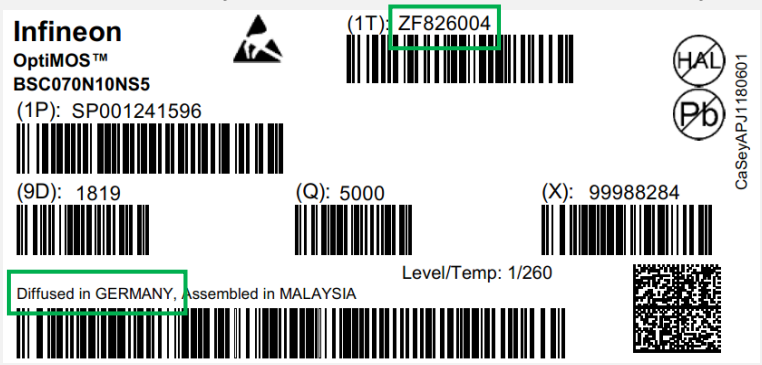
Description:	**Old**	**New**
(a) Wafer production sites with wafer diameter:	■ Infineon Technologies Austria AG, Villach, Austria (200mm)	■ Infineon Technologies Austria AG, Villach, Austria (200mm) *and* ■ Infineon Technologies Dresden GmbH, Germany (300mm)
(b) Standardization of pad design and metallization process:	■ Al/Cu *and* ■ Cu	■ Cu
(c) Standardizing mould compound TDSON-8 package:	■ Hitachi CEL 1772	■ Hitachi CEL 9240
(d) Standardizing of gate wire bond TDSON-8 package:	■ 38µm Au *and* ■ 30µm Au	■ 30µm Au

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▸ Product Identification:

External traceability: assured via Waferlot number & country of diffusion



▸ Impact of Change:

NO change on electrical, thermal parameters and reliability as proven via product qualification and characterization.

NO change in existing datasheet parameters

NO change in quality and reliability. Processes are optimized to meet product performance according to already applied Infineon specification.

▸ Attachments:

Affected product list	1_cip18013_a.xlsx
Qualification Report	2_cip18013_a.pdf

▸ Time Schedule:

■ Final qualification report:	available
■ First samples available:	on request
■ Intended start of delivery:	01-09-2018 or earlier upon customer approval

Summary:

All changes to be applied reflect Infineon's efforts to respond to increasing customer demand in mid and long term.

If you have any questions, please do not hesitate to contact your local Sales office.

PCN N° PCN 2018-013-A

Capacity extension by introduction of 300mm wafer diameter for dedicated OptiMOS™ products at Infineon Technologies Dresden, Germany & harmonization of bill of material (BoM)

Final Qualification Report **Date: 2018-05-02**

Reason for choosing following test vehicle:	IPT029N08N5, IPT015N10N5: medium and largest chip size in HSOF package platform BSC035N10NS5, BSC070N10NS5, BSZ146N10LS5: small, medium and largest chip size in PG-TSDSON/TDSON package platform IPA083N10N5, IPP083N10N5, IPB020N10N5, IPB017N10N5: small and largest chip size in PG-TO220/263 package platfom OptiMOS™ 80V and 100V share the same library catalogue and process flow technology node. 80V technology products can be referenced to 100V technology products.
Assessment of Q-Results	The 300mm wafer diameter products in all affected packages pass the qualification acc. JEDEC. This is based on positive results from all reliability stress tests performed.

Reference Products				**IPT029N08N5**	**IPT015N10N5**	**BSC035N10NS5**	**BSC070N10NS5**	**BSZ146N10LS5**	**IPA083N10N5**	**IPP083N10N5**	**IPB020N10N5**	**IPB017N10N5**
Package type				PG-HSOF-8	PG-HSOF-8	PG-TDSON-8	PG-TDSON-8	PG-TSDSON-8	PG-TO220-3	PG-TO220-3	PG-TO263-3	PG-TO263-7
Test description	**Abbr.**	Condition	Readout									
Pre-Conditioning J-STD020 / JESD22 A113	**PC**[1]	MSL reflow 3x @260°C 85°C/ 85% RH	refer to below precon readouts	MSL1	MSL1	MSL1	MSL1	MSL1	na (through hole device)	na (through hole device)	MSL1	MSL1
Temperature Cycling JESD22 A104	**TC**	Ta min = -55 °C Ta max = +150 °C	0 cyc precon 1000 cyc	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 na 0 / 77	0 / 77 na 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
Unbiased Highly Accelerated Stress Test JESD22 A118	**UHAST**	Ta = 130°C RH = 85%	0 h precon 96 h	0 / 77 0 / 77 0 / 77	referenced to IPT029N08N5 [2]	0 / 77 0 / 77 0 / 77	referenced to BSC035N10NS5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 na 0 / 77	referenced to IPA083N10N5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
High Humidity High Temp. Reverse Bias JESD22 A101	**H3TRB**	Ta = 85 °C RH = 85% V = 80% of Vds max	0 h precon 1000 h	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC070N10NS5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 na 0 / 77	referenced to IPA083N10N5 [2]	0 / 77 0 / 77 0 / 77	referenced to IPB020N10N5 [2]
High Temperature Reverse Bias JESD22 A108	**HTRB**	Tj = Tj max V = 100% of Vds max	0 h precon 1000 h	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC070N10NS5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 na 0 / 77	referenced to IPA083N10N5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
High Temperature Gate stress JESD22 A108	**HTGS**	Ta = 175°C Vgs = ±20 V for NL device Vgs = ±16 V for LL device	0 h precon 1000 h	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 na 0 / 77	referenced to IPA083N10N5 [2]	0 / 77 0 / 77 0 / 77	referenced to IPB020N10N5 [2]
Intermitted Operational Life Test MIL-STD 750/Meth.1037	**IOL**	ΔT = 100 K	0 cyc precon 10000 cyc	0 / 77 0 / 77 0 / 77	referenced to IPT029N08N5 [2]	referenced to BSC070N10NS5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to IPP083N10N5 [2]	0 / 77 na 0 / 77	referenced to IPA083N10N5 [2]	referenced to IPP083N10N5 [2]
ESD Human Body Model ANSI/ESDA/JEDEC JS-001-2014	**HBM**	-	classification	2	3A	2	1C	1B	referenced to IPP083N10N5 [3]	1C	3B	referenced to IPB020N10N5 [3]
ESD Charged Device Model ANSI/ESDA/JEDEC JS-002-2014	**CDM**	-	classification	C3	C3	C3	C3	C3	referenced to IPP083N10N5 [3]	C3	C3	referenced to IPB020N10N5 [3]

1) PC is done only for SMD Packages before stress tests
2) referencing is based on same package type
3) referencing is based on same chip in representative mechanical package type

Abbreviations:

MSL = Moisture Sensitivity Level
na = not applicable
a = ambient
RH = relative humidity
j = junction
NL = normal level gate threshold voltage
LL = normal level gate threshold voltage

PCN N° PCN 2018-013-A

Capacity extension by introduction of 300mm wafer diameter for dedicated OptiMOS™ products at Infineon Technologies Dresden, Germany & harmonization of bill of material (BoM)

Final Qualification Report **Date: 2018-06-08**

Reason for choosing following test vehicle:	biggest chip size and different technology in PG-TDSON-8 package platform
Assessment of Q-Results	Products pass the qualification acc. JEDEC. This is based on positive results from all reliability stress tests performed.

Reference Products				**BSC046N10NS3**	**BSC016N04LS**	**BSC017N04NS**	**BSC014N06NS**	**BSC026N08NS5**	**BSC040N08NS5**	**BSC117N08NS5**	**BSC035N10NS5**	**BSC070N10NS**	**BSC093N15NS5**
Package type				PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8	PG-TDSON-8
Test description	**Abbr.**	Condition	Readout										
Pre-Conditioning J-STD020 / JESD22 A113	**PC**[1]	MSL reflow 3x @260°C 85°C/ 85% RH	refer to below precon readouts	MSL1	MSL1	MSL1	MSL1	MSL1	MSL1	MSL1	MSL1	MSL1	MSL1
Temperature Cycling JESD22 A104	**TC**	Ta min = -55 °C Ta max = +150 °C	0 cyc precon 1000 cyc	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
Unbiased Highly Accelerated Stress Test JESD22 A118	**UHAST**	Ta = 130°C RH = 85%	0 h precon 96 h	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC040N08NS5 [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC070N10NS [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
High Humidity High Temp. Reverse Bias JESD22 A101	**H3TRB**	Ta = 85 °C RH = 85% V = 80% of Vds max	0 h precon 1000 h	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS [2]	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS, BSC026N08NS5 [3]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC040N08NS5 [2]	referenced to BSC070N10NS [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
High Temperature Reverse Bias JESD22 A108	**HTRB**	Tj = Tj max V = 100% of Vds max	0 h precon 1000 h	0 / 77 0 / 77 0 / 77	referenced to BSC026N08NS5 [2]	referenced to BSC026N08NS5 [3]	referenced to BSC026N08NS5 [3]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC040N08NS5 [2]	referenced to BSC070N10NS [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
High Temperature Gate stress JESD22 A108	**HTGS**	Tj = Tj max Vgs = ±20 V for NL device Vgs = ±16 V for LL device	0 h precon 1000 h	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS [2]	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS, BSC026N08NS5 [3]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC040N08NS5 [2]	referenced to BSC070N10NS [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77
Intermitted Operational Life Test MIL-STD 750/Meth.1037	**IOL**	ΔT = 100 K	0 cyc precon 10000 cyc	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS [2]	0 / 77 0 / 77 0 / 77	referenced to BSC017N04NS, BSC026N08NS5 [3]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77	referenced to BSC070N10NS [2]	0 / 77 0 / 77 0 / 77	0 / 77 0 / 77 0 / 77

1) PC is done only for SMD Packages before stress tests

2) reference based on same technology in same package type

3) reference based on same device construction in same package type

Abbreviations:

MSL = Moisture Sensitivity Level

na = not applicable

a = ambient

RH = relative humidity

j = junction

NL = normal level gate threshold voltage

LL = normal level gate threshold voltage

AFFECTED MPN

BSC026N08NS5ATMA1
BSC030N08NS5ATMA1
BSC035N10NS5ATMA1
BSC037N08NS5ATMA1
BSC040N08NS5ATMA1
BSC040N10NS5ATMA1
BSC040N10NS5E8203ATMA1
BSC052N08NS5ATMA1
BSC061N08NS5ATMA1
BSC070N10NS5ATMA1
BSC072N08NS5ATMA1
BSC098N10NS5ATMA1
BSC117N08NS5ATMA1
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BSZ075N08NS5ATMA1
BSZ084N08NS5ATMA1
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IPA083N10N5XKSA1
IPA083N10N5E8191XKSA1
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