Cypress Semiconductor Corporation, 198 Champion Court, San Jose, CA 95134. Tel: (408) 943-2600

PRODUCT INFORMATION NOTIFICATION

PIN: PIN181001 **Date:** March 06, 2018

Subject: 64Kb/256Kb Processor Companion I2C F-RAM Product Family Datasheet Update to include Oscillator Start-Up Time Parameter

To: FUTURE ELECTRONICS
FUTURE ELE
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Change Type: Minor

Description of Change:
Cypress announces an update to the 64kb/256kb processor companion I2C F-RAM product family datasheets to include the oscillator start-up time (t_{OSC}) parameter for the Real Time Clock (RTC). 't_{OSC}' is the time taken to start the RTC oscillator after it is enabled by setting oscillator enable bit (/OSCEN) to zero (0). The addition of this parameter is meant to align customer expectations to internal test requirements.

The following table shows the parameter that is added to the datasheet.

Parameter	Description	Min	Typ	Max	Units
t_{OSC}	Time to start RTC oscillator	-	-	2	sec

There are no changes to ordering part numbers. Updated product datasheets can be downloaded from the Cypress Website (www.cypress.com).

Benefit of Change:
This change will improve product testing and reduce lead times.

Part Numbers Affected: 14
See the attached 'Affected Parts List' file for a list of all part numbers affected by this change. Note that any new parts that are introduced after the publication of this PIN will include all changes outlined in this PIN.

Approximate Implementation Date:
This change will be effective with the date of this notification.

Anticipated Impact:
Cypress recommends that customers review this change against their system design and environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
This is an information only announcement. No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration

FM31L276/FM31L278

64-Kbit/256-Kbit Integrated Processor Companion with F-RAM

Features

- 64-Kbit/256-Kbit ferroelectric random access memory (F-RAM)
  - Logically organized as 8K × 8 (FM31L276)/ 32K × 8 (FM31L278)
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See Data Retention and Endurance on page 29)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- High Integration Device Replaces Multiple Parts
  - Serial nonvolatile memory
  - Real time clock (RTC)
  - Low voltage reset
  - Watchdog timer
  - Early power-fail warning/NMI
  - Two 16-bit event counter
  - Serial number with write-lock for security
- Real-time Clock/Calendar
  - Backup current at 2 V: 1.15 µA at +25 °C
  - Seconds through centuries in BCD format
  - Tracks leap years through 2099
  - Uses standard 32.768 kHz crystal (6 pF/12.5 pF)
  - Software calibration
  - Supports battery or capacitor backup
- Processor Companion
  - Active-low reset output for V_{DD} and watchdog
  - Programmable low-V_{DD} reset trip point
  - Manual reset filtered and debounced
  - Programmable watchdog timer
  - Dual Battery-backed event counter tracks system intrusions or other events
  - Comparator for power-fail interrupt
  - 64-bit programmable serial number with lock
- Fast 2-wire serial interface (I^2C)
  - Up to 1-MHz frequency
  - Supports legacy timings for 100 kHz and 400 kHz
  - RTC, Supervisor controlled via I^2C interface
  - Device select pins for up to 4 memory devices
- Low power consumption
  - 1.5 mA active current at 1 MHz
  - 120 µA standby current
- Operating voltage: V_{DD} = 2.7 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- 14-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant
- Underwriters laboratory (UL) recognized

Functional Description

The FM31L276/FM31L278 device integrates F-RAM memory with the most commonly needed functions for processor-based systems. Major features include nonvolatile memory, real time clock, low-V_{DD} reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or any other purpose.

The FM31L276/FM31L278 is a 64-Kbit/256-Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. This memory is truly nonvolatile rather than battery backed. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by other nonvolatile memories. The FM31L276/FM31L278 is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

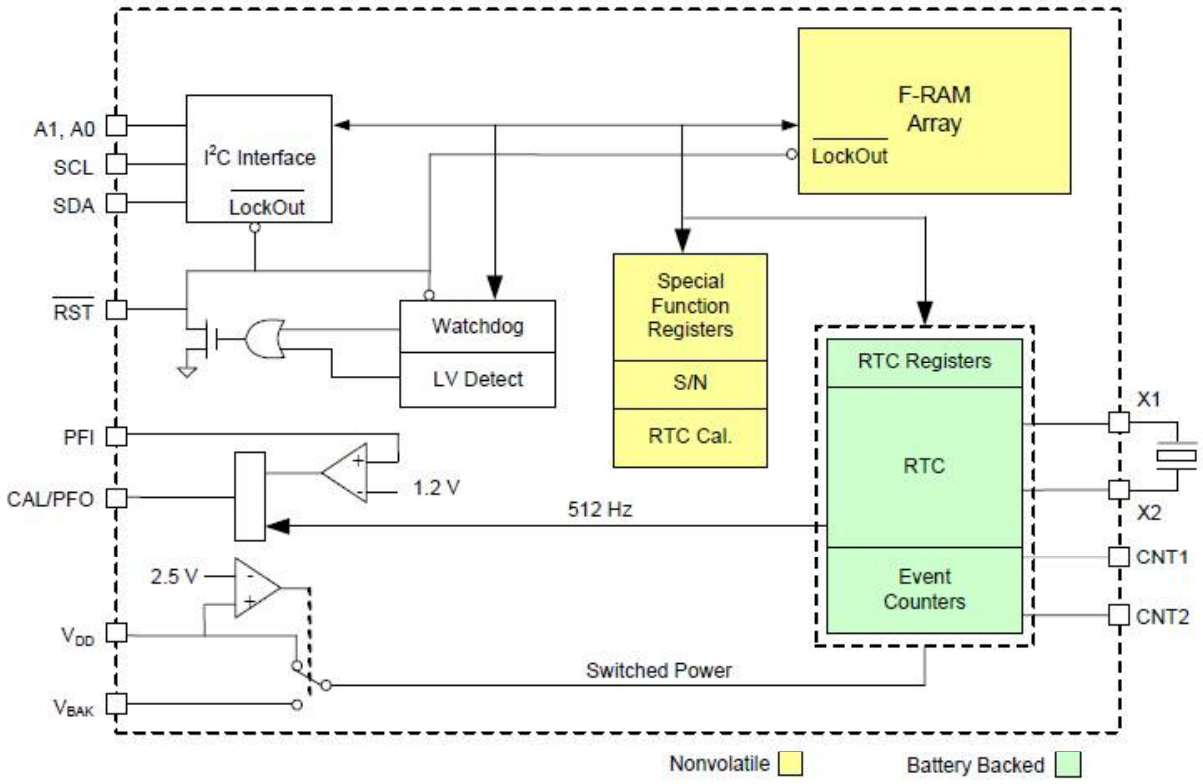
The real time clock (RTC) provides time and date information in BCD format. It can be permanently powered from an external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low V_{DD} condition or a watchdog timeout. $\overline{RST}$ goes active when V_{DD} drops below a programmable threshold and remains active for 100 ms after V_{DD} rises above the trip point. A programmable watchdog timer runs from 100 ms to 3 seconds. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host before the timeout. A flag-bit indicates the source of the reset.

A comparator on PFI compares an external input pin to the onboard 1.2 V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers a dual battery-backed event counter that tracks the number of rising or falling edges detected on a dedicated input pin.

For a complete list of related documentation, click here.

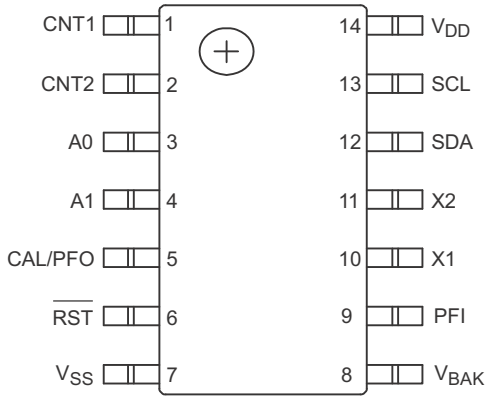
Logic Block Diagram



Contents

Pinout

Figure 1. 14-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A1–A0	Input	**Device Select Address 1–0**. These pins are used to select one of up to 4 devices of the same type on the same I^2C bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data/Address**. This is a bi-directional pin for the I^2C interface. It is open-drain and is intended to be wire-OR'd with other devices on the I^2C bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the I^2C interface. Data is clocked out of the device on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
CNT1, CNT2	Input	**Event Counter Inputs**. These battery-backed inputs increment counters when an edge is detected on the corresponding CNT pin. The polarity is programmable. These pins should not be left floating. Tie to ground if these pins are not used.
X1, X2	Input/Output	32.768 kHz crystal connection. When using an external oscillator, apply the clock to X1 and a DC mid-level to X2. These pins should be left unconnected if RTC is not used.
$\overline{RST}$	Input/Output	**Reset**. This active-low output is open drain with weak pull-up. It is also an input when used as a manual reset. This pin should be left floating if unused.
PFI	Input	**Early Power-fail Input**. Typically connected to an unregulated power supply to detect an early power failure. This pin must be tied to ground if unused.
CAL/PFO	Output	**Calibration/Early Power-fail Output**. In calibration mode, this pin supplies a 512 Hz square-wave output for clock calibration. In normal operation, this is the early power-fail output.
V_{BAK}	Power supply	**Backup supply voltage**. Connected to a 3 V battery or a large value capacitor. If no backup supply is used, this pin should be tied to ground and the VBC bit should be cleared in the RTC register 0Bh. The trickle charger is UL recognized and ensures no excessive current when using a lithium battery.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Functional Overview

The FM31L276/FM31L278 device combines a serial nonvolatile RAM with a real time clock (RTC) and a processor companion. The companion is a highly integrated peripheral including a processor supervisor, a comparator used for early power-fail warning, nonvolatile event counters, and a 64-bit serial number. The FM31L276/FM31L278 integrates these complementary but distinct functions under a common interface in a single package. The product is organized as two logical devices. The first is a memory and the second is the companion which includes all the remaining functions. From the system perspective they appear to be two separate devices with unique IDs on the serial bus.

The memory is organized as a standalone nonvolatile I^2C memory using standard device ID value. The real time clock and supervisor functions are accessed with a separate I^2C device ID. This allows clock/calendar data to be read while maintaining the most recently used memory address. The clock and supervisor functions are controlled by 25 special function registers. The RTC and event counter circuits are maintained by the power source on the V_{BAK} pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Architecture

The FM31L276/FM31L278 device is available in memory size 64-Kbit/256-Kbit. The device uses two-byte addressing for the memory portion of the chip. This makes the device software compatible with its standalone memory counterparts, but makes them compatible within the entire family.

The memory array is logically organized as 8,192 × 8 bits/ 32,768 × 8 bits and is accessed using an industry-standard I^2C interface. The memory is based on F-RAM technology. Therefore it can be treated as RAM and is read or written at the speed of the I^2C bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The I^2C protocol is described on I2C Interface on page 21.

The memory array can be write-protected by software. Two bits in the processor companion area (WP1, WP0 in register 0Bh) control the protection setting. Based on the setting, the protected addresses cannot be written and the I^2C interface will not acknowledge any data to protected addresses. The special function registers containing these bits are described in detail in Table 1 below.

Table 1. Block Memory Write Protection

WP1	WP0	Protected Address Range
0	0	None
0	1	Bottom 1/4
1	0	Bottom 1/2
1	1	Full array

Processor Companion

In addition to nonvolatile RAM, the FM31L276/FM31L278 incorporates a real time clock and highly integrated processor companion. The companion includes a low-V_{DD} reset, a programmable watchdog timer, a battery-backed event counters, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

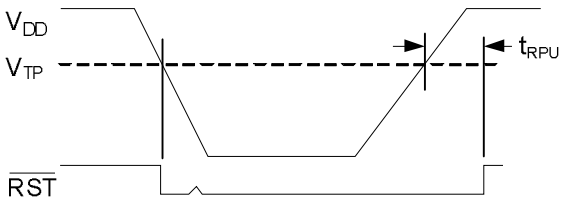
Supervisors provide a host processor two basic functions: detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. The FM31L276/FM31L278 has a reset pin ($\overline{RST}$) to drive a processor reset input during power faults, power-up, and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the $\overline{RST}$ pin. When V_{DD} is above the programmed trip point, $\overline{RST}$ output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}), the $\overline{RST}$ pin will be driven LOW. It will remain LOW until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, $\overline{RST}$ continues to drive LOW for at least 100 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the $\overline{RST}$ pin will return to the weak HIGH state. While $\overline{RST}$ is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

Table 2 below shows how bit VTP controls the trip point of the low-V_{DD} reset. They are located in register 0Bh, bits 1 and 0. The reset pin will drive LOW when V_{DD} is below the selected V_{TP} voltage, and the I^2C interface and F-RAM array will be locked out. Note that the bit 1 location is a don't care. Figure 2 illustrates the reset operation in response to a low V_{DD}.

Table 2. VTP setting

VTP Setting	VTP
2.6 V	0
2.9 V	1

Figure 2. Low V_{DD} Reset

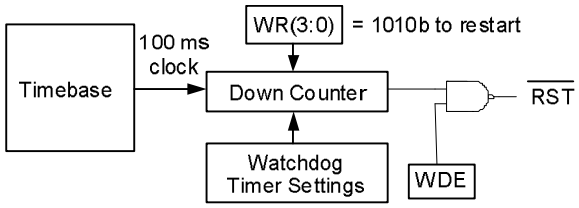


A watchdog timer can also be used to drive an active reset signal. The watchdog is a free-running programmable timer. The timeout period can be software programmed from 100 ms to 3 seconds in 100 ms increments via a 5-bit nonvolatile register. All programmed settings are minimum values and vary with temperature according to the operating specifications. The watchdog has two additional controls associated with its operation, a watchdog enable bit (WDE) and timer restart bits (WR). Both the enable bit must be set and the watchdog must timeout in order to drive $\overline{RST}$ active. If a reset event occurs, the timer will automatically restart on the rising edge of the reset pulse. If WDE = '0', the watchdog timer runs but a watchdog fault will not cause $\overline{RST}$ to be asserted LOW. The WTR flag will be set, indicating a watchdog fault. This setting is useful during software development if the developer does not want $\overline{RST}$ to drive. Note that setting the maximum timeout setting (11111b) disables the counter to save power. The second control is a nibble that restarts the timer preventing a reset. The timer should be restarted after changing the timeout value.

The watchdog timeout value is located in register 0Ah, bits 4:0, and the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 09h. Writing this pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout period will be set immediately after enabling. The watchdog is disabled when V_{DD} is below V_{TP}. The following table summarizes the watchdog bits. A block diagram follows.

Watchdog Timeout	WDT(4:0)	0Ah, bits 4:0
Watchdog Enable	WDE	0Ah, bit 7
Watchdog Restart	WR(3:0)	09h, bits 3:0

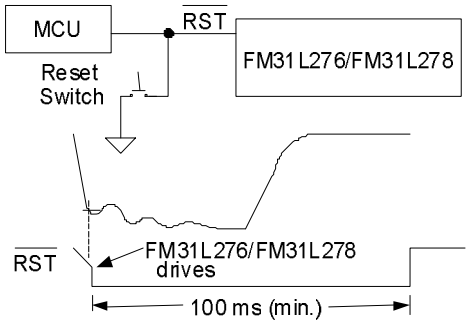
Figure 3. Watchdog Timer



Manual Reset

The $\overline{RST}$ is a bi-directional signal allowing the FM31L276/FM31L278 to filter and de-bounce a manual reset switch. The $\overline{RST}$ input detects an external low condition and responds by driving the $\overline{RST}$ signal LOW for 100 ms.

Figure 4. Manual Reset



Note The internal weak pull-up eliminates the need for additional external components.

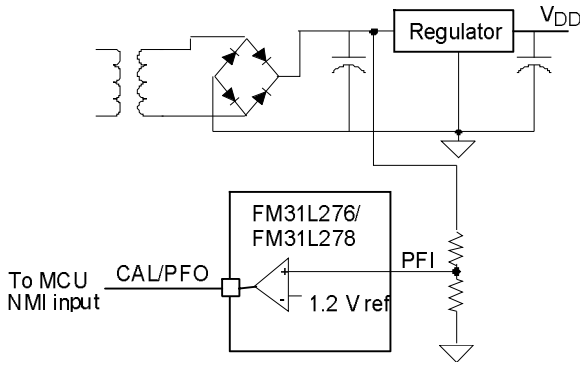
Reset Flags

In case of a reset condition, a flag bit will be set to indicate the source of the reset. A low-V_{DD} reset is indicated by the POR flag, register 09h bit 6. A watchdog reset is indicated by the WTR flag, register 09h bit 7. Note that the flags are internally set in response to reset sources, but they must be cleared by the user. When the register is read, it is possible that both flags are set if both have occurred since the user last cleared them.

Early Power Fail Comparator

An early power fail warning can be provided to the processor well before V_{DD} drops out of spec. The comparator is used to create a power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to the unregulated power supply via a resistor divider. An application circuit is shown below.

Figure 5. Comparator as a Power-Fail Warning



The voltage on the PFI input pin is compared to an onboard 1.2 V reference. When the PFI input voltage drops below this threshold, the comparator will drive the CAL/PFO pin to a LOW state. The comparator has 100 mV (max) of hysteresis to reduce noise sensitivity, only for a rising PFI signal. For a falling PFI edge, there is no hysteresis.

The comparator is a general purpose device and its application is not limited to the NMI function.

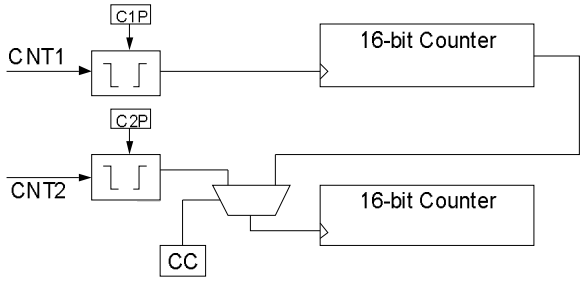
The comparator is not integrated into the special function registers except as it shares its output pin with the CAL output. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the CAL/PFO output pin will be driven with a 512 Hz square wave and the comparator will be ignored. Since most users only invoke the calibration mode during production, this should have no impact on system operations using the comparator.

Note The maximum voltage on the comparator input PFI is limited to 3.75 V under normal operating conditions.

Event Counter

The FM31L276/FM31L278 offers the user two battery-backed event counters. Input pins CNT1 and CNT2 are programmable edge detectors. Each clocks a 16-bit counter. When an edge occurs, the counters will increment their respective registers. Counter 1 is located in registers 0Dh and 0Eh, Counter 2 is located in registers 0Fh and 10h. These register values can be read anytime V_{DD} is above V_{TP}, and they will be incremented as long as a valid V_{BAK} power source is provided. To read, set the RC bit register 0Ch bit 3 to 1. This takes a snapshot of all four counter bytes allowing a stable value even if a count occurs during the read. The registers can be written by software allowing the counters to be cleared or initialized by the system. Counts are blocked during a write operation. The two counters can be cascaded to create a single 32-bit counter by setting the CC control bit (register 0Ch, bit 2). When cascaded, the CNT1 input will cause the counter to increment. CNT2 is not used in this mode and should be tied to ground.

Figure 6. Event Counter



The control bits for event counting are located in register 0Ch. Counter 1 Polarity is bit C1P, bit 0; Counter 2 Polarity is C2P, bit 1; the Cascade Control is CC, bit 2; and the Read Counter bit is RC, bit 3.

The polarity bits must be set prior to setting the counter value(s). If a polarity bit is changed, the counter may inadvertently increment. If the counter pins are not being used, tie them to ground.

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writeable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via the device ID for the Processor Companion. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. However, once the lock bit is set, the values cannot be altered and the lock cannot be removed. Once locked the serial number registers can still be read by the system.

The serial number is located in registers 11h to 18h. The lock bit is SNL (register 0Bh, bit 7). Setting the SNL bit to a '1' disables writes to the serial number registers, and the SNL bit cannot be cleared.

Real-time Clock Operation

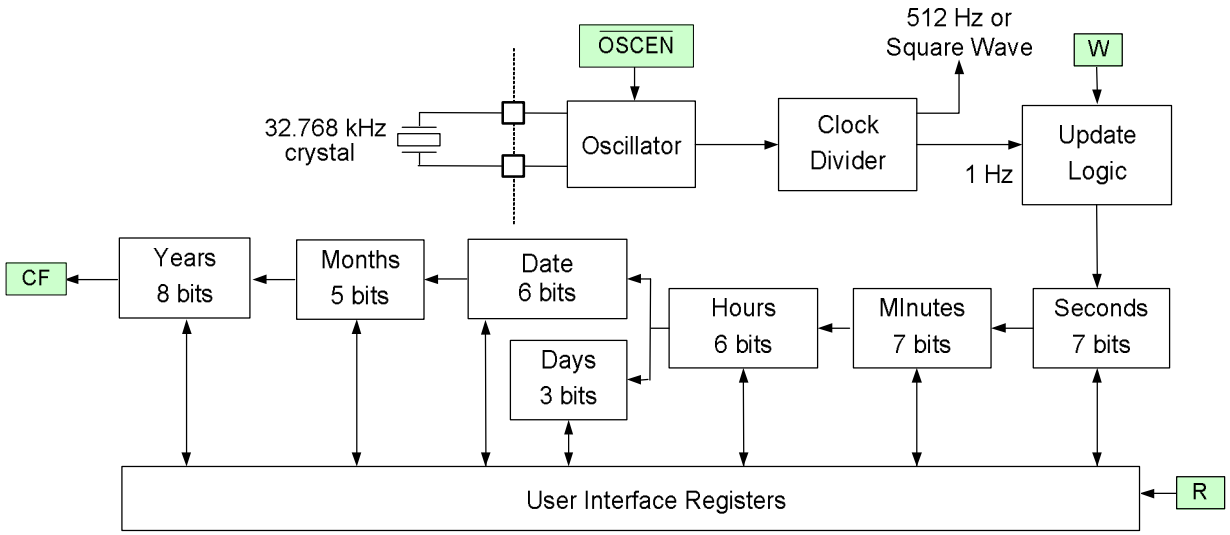
The real-time clock (RTC) is a timekeeping device that can be battery or capacitor backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1 Hz). Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram (Figure 7) illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h described below. Changing the R bit from '0' to '1' transfers timekeeping information from the core into holding registers that can be read by the user. If a timekeeper update is pending when R is set, then the core will be updated prior to loading the user registers. The registers are frozen and will not be updated again until the R bit is cleared to '0'. R is used for reading the time.

Setting the W bit to '1' locks the user registers. Clearing it to '0' causes the values in the user registers to be loaded into the timekeeper core. W bit is used for writing new time values. Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

Figure 7. Real-Time Clock Core Block Diagram

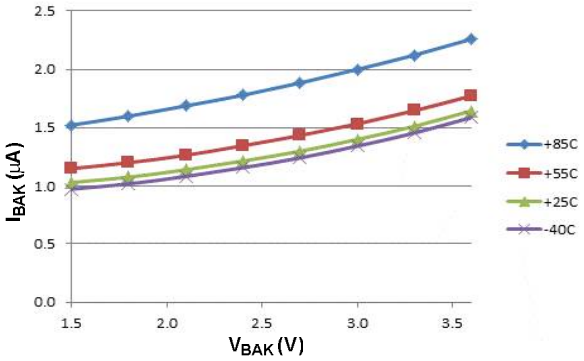


Backup Power

The real-time clock/calendar is intended to be permanently powered. When the primary system power fails, the voltage on the V_{DD} pin will drop. When V_{DD} is less than 2.5 V, the RTC (and event counters) will switch to the backup power supply on V_{BAK}. The clock operates at extremely low current in order to maximize battery or capacitor life. However, an advantage of combining a clock function with F-RAM memory is that data is not lost regardless of the backup power source.

The I_{BAK} current varies with temperature and voltage (see DC Electrical Characteristics on page 27). The following graph shows I_{BAK} as a function of V_{BAK}. These curves are useful for calculating backup time when a capacitor is used as the V_{BAK} source.

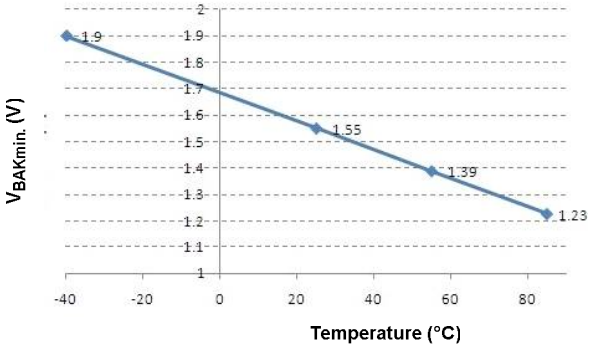
Figure 8. I_{BAK} vs. V_{BAK} Voltage



The minimum V_{BAK} voltage varies linearly with temperature. The user can expect the minimum V_{BAK} voltage to be 1.23 V at +85 °C and 1.90 V at -40 °C. The tested limit is 1.55 V at +25 °C.

Note The minimum V_{BAK} voltage has been characterized at -40 °C and +85 °C but is not 100% tested.

Figure 9. V_{BAK}(min.) vs Temperature



Trickle Charger

To facilitate capacitor backup the V_{BAK} pin can optionally provide a trickle charge current. When the VBC bit (register 0Bh, bit 2) is set to '1', the V_{BAK} pin will source approximately 80 µA until V_{BAK} reaches V_{DD}. This charges the capacitor to V_{DD} without an external diode and resistor charger. There is a Fast Charge mode which is enabled by the FC bit (register 0Bh, bit 5). In this mode the trickle charger current is set to approximately 1 mA, allowing a large backup capacitor to charge more quickly.

In the case where no battery is used, the V_{BAK} pin should be tied to V_{SS}. Be sure to turn off the trickle charger (VBC = '0'), otherwise charger current will be shunted to ground from V_{DD}.

Note Systems using lithium batteries should clear the VBC bit to '0' to prevent battery charging. The V_{BAK} circuitry includes an internal 1 KΩ series resistor as a safety element. The trickle charger is UL Recognized.

Calibration

When the CAL bit in the register 00h is set to '1', the clock enters calibration mode. In calibration mode, the CAL/PFO output pin is dedicated to the calibration function and the power fail output is temporarily unavailable. Calibration operates by applying a digital correction to the counter based on the frequency error. In this mode, the CAL/PFO pin is driven with a 512 Hz (nominal) square wave. Any measured deviation from 512 Hz translates into a timekeeping error. The user converts the measured error in ppm and writes the appropriate correction value to the calibration register. The correction factors are listed in the table below. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to '1', whereas negative ppm adjustments have CALS = '0'. After calibration, the clock will have a maximum error of ±2.17 ppm or ±0.09 minutes per month at the calibrated temperature.

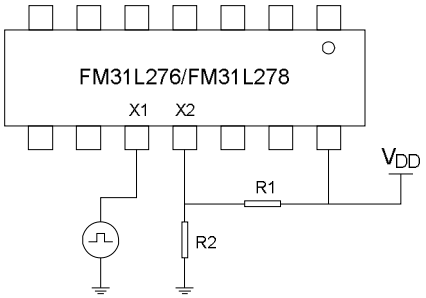
The calibration setting is stored in F-RAM so it is not lost should the backup source fail. It is accessed with bits CAL(4:0) in register 01h. This value can be written only when the CAL bit is set to a '1'. To exit the calibration mode, the user must clear the CAL bit to a '0'. When the CAL bit is '0', the CAL/PFO pin will revert to the power fail output function.

Crystal Oscillator

The crystal oscillator is designed to use a 6 pF/12.5 pF crystal without the need for external components, such as loading capacitors. The FM31L276/FM31L278 device has built-in loading capacitors that are optimized for use with 6 pF crystals, but which work well with 12.5 pF crystals. For either crystal, no additional external loading capacitors are required nor suggested.

If a 32.768 kHz crystal is not used, an external oscillator may be connected to the FM31L276/FM31L278. Apply the oscillator to the X1 pin. Its high and low voltage levels can be driven rail-to-rail or amplitudes as low as approximately 500 mV p-p. To ensure proper operation, a DC bias must be applied to the X2 pin. It should be centered between the high and low levels on the X1 pin. This can be accomplished with a voltage divider.

Figure 10. External Oscillator

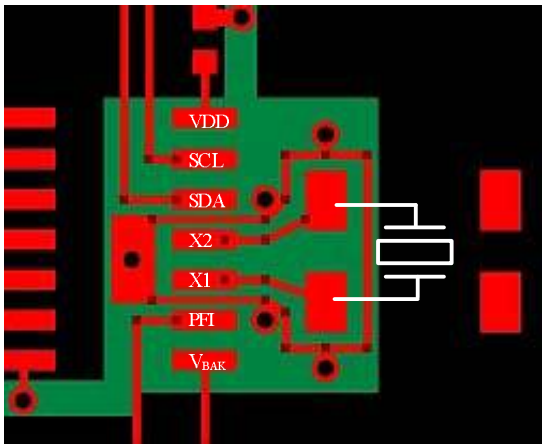


In the example, R1 and R2 are chosen such that the X2 voltage is centered around the X1 oscillator drive levels. If you wish to avoid the DC current, you may choose to drive X1 with an external clock and X2 with an inverted clock using a CMOS inverter.

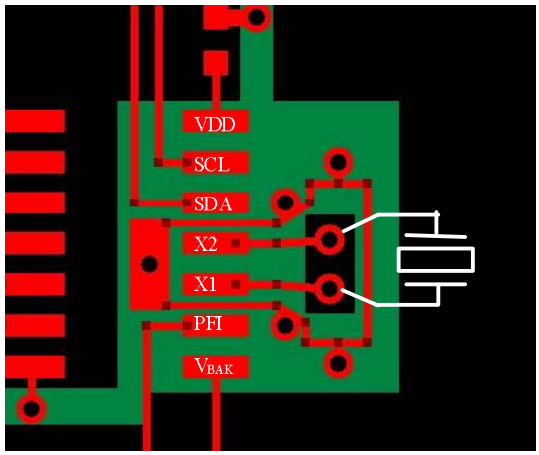
Layout Recommendations

The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring must be placed around these pads and the guard ring grounded. SDA and SCL traces should be routed away from the X1 / X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.

Figure 11. Layout Recommendations



Layout for Surface Mount Crystal
(red = top layer, green = bottom layer)



Layout for Through Hole Crystal
(red = top layer, green = bottom layer)

Table 3. Digital Calibration Adjustments

S.No.	Measured Frequency Range		Error Range (PPM)		Program Calibration Register to:
	Min	Max	Min	Max	
Positive Calibration for slow clocks: Calibration will achieve ±2.17 PPM after calibration					
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

Table 3. Digital Calibration Adjustments (continued)

S.No.	Measured Frequency Range		Error Range (PPM)		Program Calibration Register to:
	Min	Max	Min	Max	
Negative Calibration for fast clocks: Calibration will achieve ±2.17 PPM after calibration					
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001
2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

Register Map

The RTC and processor companion functions are accessed via 25 special function registers, which are mapped to a separate I^2C device ID. The interface protocol is described on I2C Interface on page 21. The registers contain timekeeping data, control bits, and information flags. A description of each register follows the summary table.

Table 4. Register Map Summary Table

Nonvolatile = ☐ Battery-backed = ☐

Address	Data								Function	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
18h	Serial Number Byte 7								Serial Number 7	FFh
17h	Serial Number Byte 6								Serial Number 6	FFh
16h	Serial Number Byte 5								Serial Number 5	FFh
15h	Serial Number Byte 4								Serial Number 4	FFh
14h	Serial Number Byte 3								Serial Number 3	FFh
13h	Serial Number Byte 2								Serial Number 2	FFh
12h	Serial Number Byte 1								Serial Number 1	FFh
11h	Serial Number Byte 0								Serial Number 0	FFh
10h	Counter 2 MSB								Event Counter 2 MSB	FFh
0Fh	Counter 2 LSB								Event Counter 2 LSB	FFh
0Eh	Counter 1 MSB								Event Counter 1 MSB	FFh
0Dh	Counter 1 LSB								Event Counter 1 LSB	FFh
0Ch	–	–	–	–	RC	CC	C2P	C1P	Event Count Control	
0Bh	SNL	–	FC	WP1	WP0	VBC	–	VTP	Companion Control	
0Ah	WDE	–	–	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog Control	
09h	WTR	POR	LB	–	WR3	WR2	WR1	WR0	Watchdog Restart/Flags	
08h	10 years				years				Years	00–99
07h	0	0	0	10 months	months				Month	01–12
06h	0	0	10 date		date				Date	01–31
05h	0	0	0	0	0	day			Day	01–07
04h	0	0	10 hours		hours				Hours	00–23
03h	0	10 minutes			minutes				Minutes	00–59
02h	0	10 seconds			seconds				Seconds	00–59
01h	$\overline{\text{OSCEN}}$	reserved	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL Control	
00h	reserved	CF	reserved	reserved	reserved	CAL	W	R	RTC Control	

Note When the device is first powered up and programmed, all timekeeping registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers. All other register values should be treated as unknown.

Table 5. Default Register Values

Address	Hex Value
18h	0x00
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00
12h	0x00
11h	0x00
0Bh	0x00

Address	Hex Value
0Ah	0x1F
08h	0x00
07h	0x01
06h	0x01
05h	0x01
04h	0x00
03h	0x01
02h	0x00
01h	0x80

Table 6. Register Description

Address	Description							
18h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
	Upper byte of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
17h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
16h	Byte 6 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
	Serial Number Byte 5							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
	Byte 5 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
15h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
	Byte 4 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
14h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24
	Byte 3 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
13h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
	Byte 2 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
12h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
	Byte 1 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
11h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	LSB of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
10h	**Counter 2 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.15	C2.14	C2.13	C2.12	C2.11	C2.10	C2.9	C2.8
	Event Counter 2 MSB. Increments on overflows from Counter 2 LSB. Battery-backed, read/write.							

Table 6. Register Description (continued)

Address	Description							
0Fh	**Counter 2 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
	Event Counter 2 LSB. Increments on programmed edge event on CNT2 input or overflows from Counter 1 MSB when CC = '1'. Battery-backed, read/write.							
0Eh	**Counter 1 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.15	C1.14	C1.13	C1.12	C1.11	C1.10	C1.9	C1.8
	Event Counter 1MSB. Increments on overflows from Counter 1 LSB. Battery-backed, read/write.							
0Dh	**Counter 1 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Event Counter 1 LSB. Increments on programmed edge event on CNT1 input. Battery-backed, read/write.							
0Ch	**Event Counter Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	–	–	–	–	RC	CC	C2P	C1P
RC	Read Counter. Setting this bit to '1' takes a snapshot of the four counters bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.							
CC	Counter Cascade. When CC = '0', the event counters operate independently according to the edge programmed by C1P and C2P respectively. When CC = '1', the counters are cascaded to create one 32-bit counter. The registers of Counter 2 represent the most significant 16-bits of the counter and CNT1 is the controlling input. Bit C2P is don't care when CC = '1'. Battery-backed, read/write.							
C2P	CNT2 detects falling edges when C2P = '0', rising edges when C2P = '1'. C2P is "don't care" when CC = '1'. The value of Event Counter 2 may inadvertently increment if C2P is changed. Battery-backed, read/write.							
C1P	CNT1 detects falling edges when C1P = '0', rising edges when C1P = '1'. The value of Event Counter 1 may inadvertently increment if C1P is changed. Battery-backed, read/write.							
0Bh	**Companion Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SNL	–	FC	WP1	WP0	VBC	–	VTP
SNL	Serial Number Lock: Setting to a '1' makes registers 11h to 18h and SNL permanently read-only. SNL cannot be cleared once set to '1'. Nonvolatile, read/write.							
FC	Fast Charge: Setting FC to '1' (and VBC = '1') causes a ~1 mA trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.							
WP(1:0)	Write Protect. These bits control the write protection of the memory array. Nonvolatile, read/write. Write protect address: None – WP1=0, WP0=0; Bottom 1/4 – WP1=0, WP0=1; Bottom 1/2 – WP1=1, WP0=0; Full array – WP1=1, WP0=1							
VBC	V_{BAK} Charger Control. Setting VBC to '1' (and FC = '0') causes a 80 µA (1 mA if FC = '1') trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.							

Table 6. Register Description (continued)

Address	Description
VTP	VTP Select. This bit control the reset trip point for the low V_{DD} reset function. Nonvolatile, read/write. Trip Volatge VTP 2.60 V 0 2.90 V 1
0Ah	**Watchdog Control**

D7	D6	D5	D4	D3	D2	D1	D0
WDE	–	–	WDT4	WDT3	WDT2	WDT1	WDT0

WDE	Watchdog Enable. When WDE = '1', a watchdog timer fault will cause the $\overline{RST}$ signal to go active. When WDE = '0' the timer runs but has no effect on $\overline{RST}$, however the WTR flag will be set when a fault occurs. Note as the timer is free-running, users should restart the timer using WR(3:0) prior to setting WDE = '1'. This assures a full watchdog timeout interval occurs. Nonvolatile, read/write.
WDT(4:0)	Watchdog Timeout. Indicates the minimum watchdog timeout interval with 100 ms resolution. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). Nonvolatile, read/write.

Watchdog Timeout	WDT4	WDT3	WDT2	WDT1	WDT0
Invalid - default 100 ms	0	0	0	0	0
100 ms	0	0	0	0	1
200 ms	0	0	0	1	0
300 ms	0	0	0	1	1
.					
.					
2000 ms	1	0	1	0	0
2100 ms	1	0	1	0	1
2200 ms	1	0	1	1	0
.					
.					
2900 ms	1	1	1	0	1
3000 ms	1	1	1	1	0
Disable Counter	1	1	1	1	1

09h	**Watchdog Restart and Flags**

D7	D6	D5	D4	D3	D2	D1	D0
WTR	POR	LB	–	WR3	WR2	WR1	WR0

WTR	Watchdog Timer Reset Flag: When a watchdog timer fault occurs, the WTR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
POR	Power-on Reset Flag: When the $\overline{RST}$ pin is activated by $V_{DD} < V_{TP}$, the POR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
LB	Low Backup Flag: On power up, if the V_{BAK} source is below the minimum voltage to operate the RTC and event counters, this bit will be set to '1'. The user should clear it to '0' when initializing the system. Battery-backed. Read/Write (internally set, user can clear bit).
WR(3:0)	Watchdog Restart: Writing a pattern 1010b to WR(3:0) restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR(3:0) has no effect on the timer. This allows users to clear the WTR, POR, and LB flags without affecting the watchdog timer. Battery-backed, Write-only.

Table 6. Register Description (continued)

Address	Description							
08h	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99. Battery-backed, read/write.							
07h	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12. Battery-backed, read/write.							
06h	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1–31. Battery-backed, read/write.							
05h	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.							
04h	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours.2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23. Battery-backed, read/write.							
03h	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59. Battery-backed, read/write.							
02h	**Timekeeping – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							
01h	**CAL/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{\text{OSCEN}}$	Reserved	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0

Table 6. Register Description (continued)

Address	Description							
$\overline{\text{OSCEN}}$	Oscillator Enable. When set to '1', the oscillator is halted. When set to '0', the oscillator runs after t_{OSC} time. Disabling the oscillator can save battery power during storage. On a power-up without battery, this bit is set to '1'. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to '0'.							
CALS	Calibration Sign: Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit can be written only when CAL = '1'. Nonvolatile, read/write.							
CAL(4:0)	Calibration Setting: These five bits control the calibration of the clock. These bits can be written only when CAL = '1'. Nonvolatile, read/write.							
00h	**RTC Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	Reserved	CF	Reserved	Reserved	Reserved	CAL	W	R
CF	Century Overflow Flag. This bit is set to a '1' when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to '0' when the Flag register is read. It is read-only for the user. Battery-backed.							
CAL	Calibration Setting. When set to '1', the clock enters calibration mode. When CAL is set to '0', the clock operates normally, and the CAL/PFO pin is controlled by the power fail comparator. Battery-backed, read/write.							
W	Write Time. Setting the W bit to '1' freezes the clock. The user can then write the timekeeping registers with updated values. Resetting the W bit to '0' causes the contents of the time registers to be transferred to the timekeeping counters and restarts the clock. Battery-backed, read/write.							
R	Read Time. Setting the R bit to '1' copies a static image of the timekeeping core and place it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from '0' to '1' causes the timekeeping capture, so the bit must be returned to '0' prior to reading again. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to '0'.							

I²C Interface

The FM31L276/FM31L278 employs an industry standard I²C bus that is familiar to many users. This product is unique since it incorporates two logical devices in one chip. Each logical device can be accessed individually. Although monolithic, it appears to the system software to be two separate products. One is a memory device. It has a Slave Address (Slave ID = 1010b) that operates the same as a stand-alone memory device. The second device is a real-time clock and processor companion which have a unique Slave Address (Slave ID = 1101b).

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM31L276/FM31L278 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 12 and Figure 13 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

STOP Condition (P)

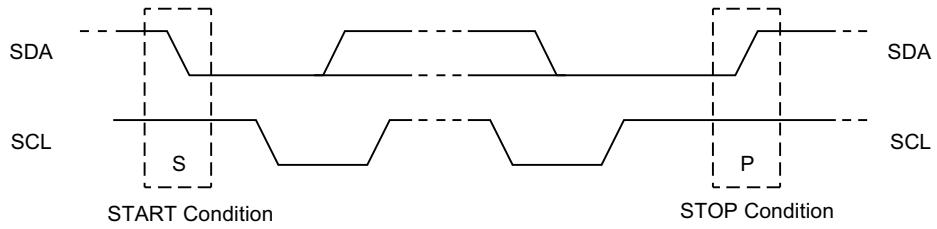
A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM31L276/FM31L278 should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM31L276/FM31L278 for a new operation.

If during operation the power supply drops below the specified V_{TP} minimum, any I²C transaction in progress will be aborted and the system should issue a START condition prior to performing another operation.

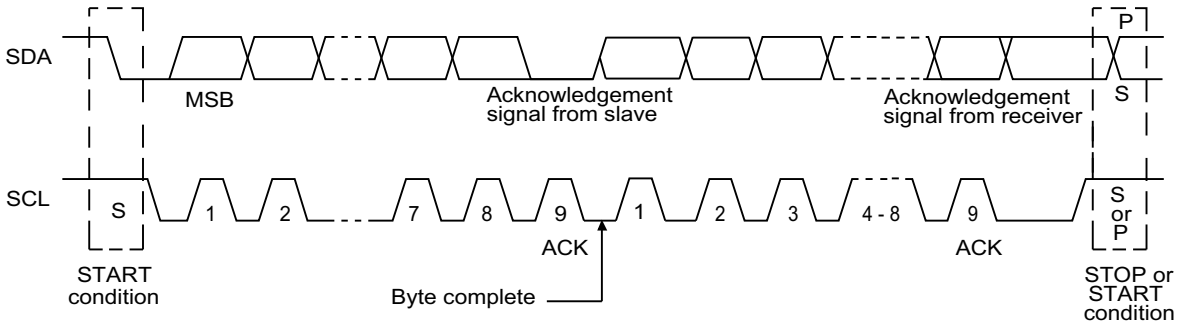
Figure 12. START and STOP Conditions



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

Figure 13. Data Transfer on the I²C Bus



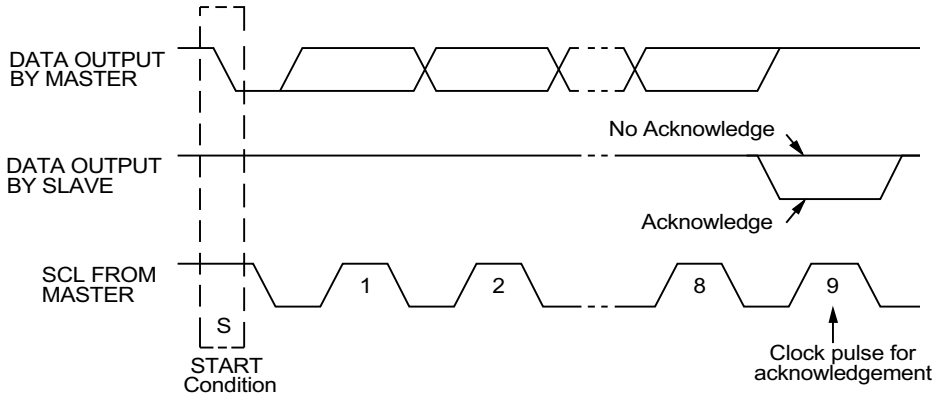
Acknowledge/No-acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the device can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM31L276/FM31L278 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM31L276/FM31L278 to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 14. Acknowledge on the I²C Bus



Slave Address

The first byte that the FM31L276/FM31L278 expects after a START condition is the slave address. As shown in Figure 15 and Figure 16, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

The FM31L276/FM31L278 has two Slave Addresses (Slave IDs) associated with two logical devices. Bits 7–4 are the device type (slave ID) and should be set to 1010b for the memory device. The other logical device within the FM31L276/FM31L278 is the real-time clock and companion. Bits 7–4 are the device type (slave ID) and should be set to 1101b for the RTC and companion. A bus transaction with this slave address will not affect the memory in any way. The figures below illustrate the two Slave Addresses.

Bits 2-1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to four FM31L276/FM31L278 devices can reside on the same I²C bus by assigning a different address to each. Bit 0 is the read/write bit (R/$\overline{W}$). R/$\overline{W}$ = '1' indicates a read operation and R/$\overline{W}$ = '0' indicates a write operation.

Figure 15. Memory Slave Device Address

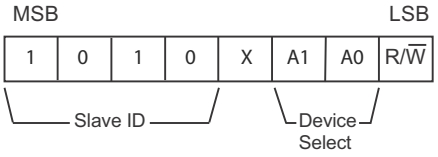
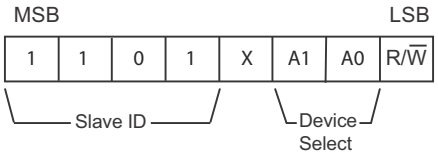


Figure 16. Companion Slave Device Address



Addressing Overview - Memory

After the FM31L276/FM31L278 (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 15-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as $V_{DD} > V_{TP}$ or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM31L276/FM31L278 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Addressing Overview - RTC & Companion

The RTC and Processor Companion operate in a similar manner to the memory, except that it uses only one byte of address. Addresses 00h to 18h correspond to special function registers. Attempting to load addresses above 18h is an illegal condition; the FM31L276/FM31L278 will return a NACK and abort the I^2C transaction.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM31L276/FM31L278 can begin. For a read operation the FM31L276/FM31L278 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM31L276/FM31L278 will transfer the next sequential byte. If the acknowledge is not sent, the FM31L276/FM31L278 will end the read operation. For a write operation, the FM31L276/FM31L278 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM31L276/FM31L278 is designed to operate in a manner very similar to other I^2C interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM31L276/FM31L278 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

The memory address for FM31L276 range from 0x0000 to 0x1FFFF, and for FM31L278, they range from 0x0000 to 0x7FFF. Memory functionality is described with respect to FM31L278 in the following sections.

Memory Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/$\overline{W}$ bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM31L276/FM31L278 uses no page buffering.

Figure 17 and Figure 18 below illustrate a single-byte and multiple-byte write cycles.

Figure 17. Single-Byte Write

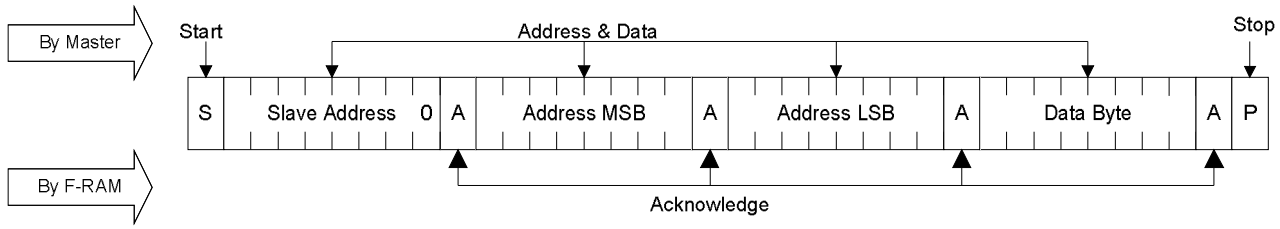
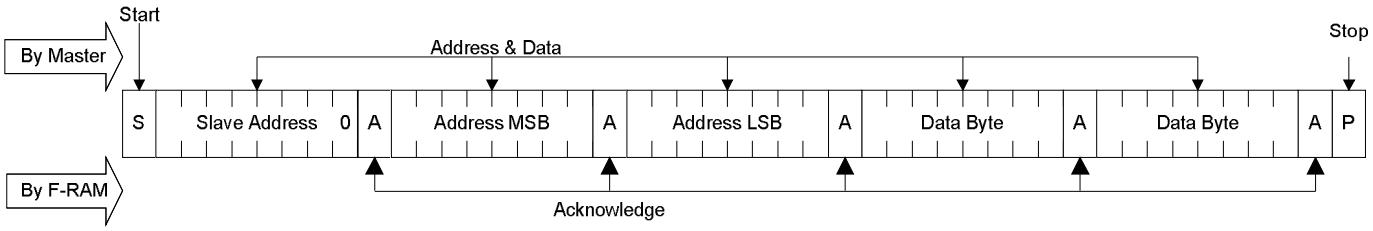


Figure 18. Multi-Byte Write



Memory Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM31L276/FM31L278 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM31L276/FM31L278 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM31L276/FM31L278 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM31L276/FM31L278 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM31L276/FM31L278 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. Figure 19 and Figure 20 below show the proper operation for current address reads.

Figure 19. Current Address Read

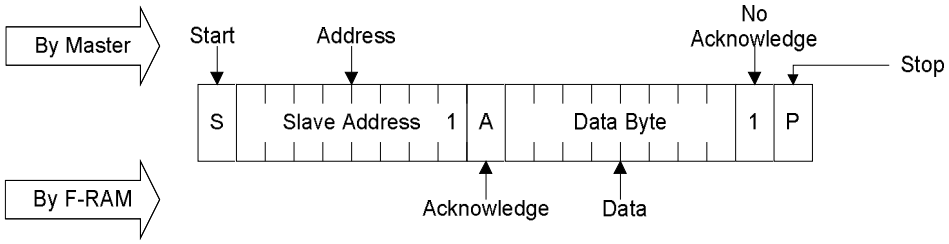
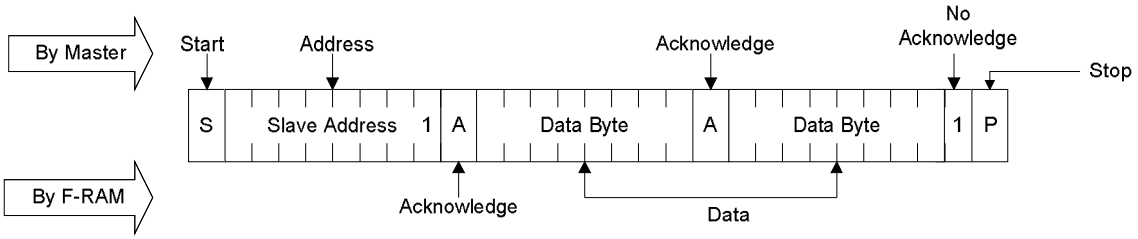


Figure 20. Sequential Read

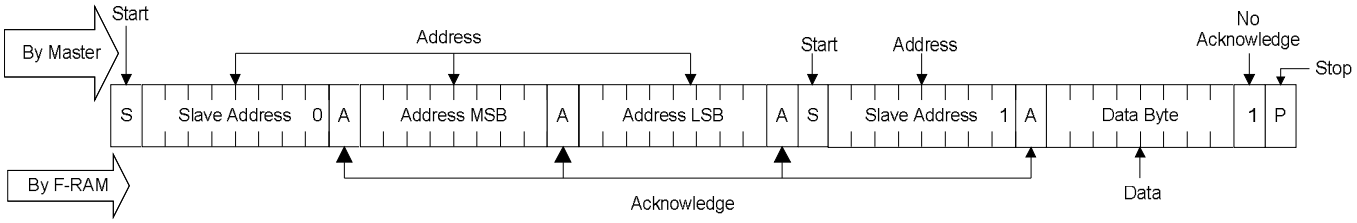


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB (R/$\overline{W}$) set to '0'. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM31L276/FM31L278 acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 21. Selective (Random) Read

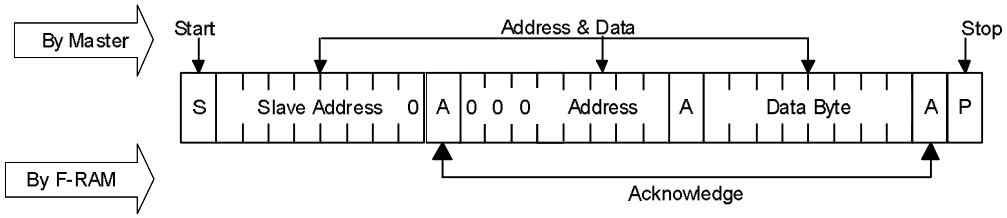


RTC/Companion Write Operation

All RTC and Companion writes operate in a similar manner to memory writes. The distinction is that a different device ID is used and only one byte address is needed instead of two byte address. Figure 22 illustrates a single byte write to this device.

Note Although not required, it is recommended that A5-A7 in the register address byte are zeros in order to preserve compatibility with future devices.

Figure 22. Single Byte Write



RTC/Companion Read Operation

As with writes, a read operation begins with the Slave Address. To perform a register read, the bus master supplies a Slave Address with the LSB set to '1'. This indicates that a read operation is requested. After receiving the complete Slave Address, the FM31L276/FM31L278 will begin shifting data out from the current register address on the next clock. Auto-increment operates for the special function registers as with the memory address. A current address read for the registers look exactly like the memory except that the device ID is different.

The FM31L276/FM31L278 contains two separate address registers, one for the memory address and the other for the register address. This allows the contents of one address register to be modified without affecting the current address of the other register. For example, this would allow an interrupted read to the memory while still providing fast access to an RTC register. A subsequent memory read will then continue from the memory address where it previously left off, without requiring the load of a new memory address. However, a write sequence always requires an address to be supplied.

Addressing FRAM Array in the FM31L276/FM31L278 Family

The FM31L276/FM31L278 family includes 64-Kbit and 256-Kbit memory densities. The following 2-byte address field is shown for each density.

Part Number	1st Address Byte								2nd Address Byte							
FM31L276	X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
FM31L278	X	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Ambient Temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +5.0 V

Input voltage ..... –1.0 V to +5.0 V and $V_{IN} < V_{DD} + 1.0$ V

Backup supply voltage .....–1.0 V to +4.5 V

DC voltage applied to outputs in High-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260°C

DC output current (1 output at a time, 1s duration) ..... 15 mA

Electrostatic Discharge Voltage
Human Body Model (AEC-Q100-002 Rev. D) ..... 2 kV
Charged Device Model (AEC-Q100-011 Rev. B) ..... 1.25 kV
Machine Model (AEC-Q100-003 Rev. E) ..... 100 V

Latch-up current ..... > ±100 mA

Note PFI input voltage must not exceed 4.5 V. The "$V_{IN} < V_{DD} + 1.0$ V" restriction does not apply to the SCL and SDA inputs which do not employ a diode to V_{DD}.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{DD}[2]	Power supply			2.7	–	3.6	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.3 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.3 V.	f_{SCL} = 100 kHz	–	–	500	µA
			f_{SCL} = 400 kHz	–	–	900	µA
			f_{SCL} = 1 MHz	–	–	1500	µA
I_{SB}	V_{DD} standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	–	120	µA
V_{BAK}[3]	RTC backup voltage		T_A = +25 °C to +85 °C	1.55	–	3.75	V
			T_A = –40 °C to +25 °C	1.90	–	3.75	V
I_{BAK}	RTC backup current	V_{BAK} = 3.0 V, V_{DD} < 2.4 V, oscillator running, CNT1, CNT2 at V_{BAK}.	T_A = +25 °C, V_{BAK} = 3.0 V	–	–	1.4	µA
			T_A = +85 °C, V_{BAK} = 3.0 V	–	–	2.1	µA
			T_A = +25 °C, V_{BAK} = 2.0 V	–	–	1.15	µA
			T_A = +85 °C, V_{BAK} = 2.0 V	–	–	1.75	µA
I_{BAKTC}[4]	Trickle charge current with V_{BAK} = 0 V		Fast Charge Off (FC = '0')	50	–	120	µA
			Fast Charge On (FC = '1')	200	–	2500	µA

Notes
1. Typical values are at 25 °C, $V_{DD} = V_{DD}$(typ). Not 100% tested.
2. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
3. The V_{BAK} trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
4. V_{BAK} will source current when trickle charge is enabled (VBC bit = '1'), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$ max.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{TP1}	V_{DD} trip point voltage, VTP = 0	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$		2.55	2.60	2.70	V
V_{TP2}	V_{DD} trip point voltage, VTP = 1	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$		2.85	2.90	3.00	V
V_{RST}[5]	V_{DD} for valid $\overline{RST}$	I_{OL} = 80 µA at V_{OL}	$V_{BAK} > V_{BAK}$ min	0	–	–	V
			$V_{BAK} < V_{BAK}$ min	1.6	–	–	V
I_{LI}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$. Does not apply to A0, A1, X1, PFI, $\overline{RST}$, or X2		–	–	±1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$. Does not apply to $\overline{RST}$, X1, or X2		–	–	±1	µA
V_{IL}[6]	Input LOW voltage		All inputs except as listed below	– 0.3	–	0.3 × V_{DD}	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	– 0.3	–	0.5	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	– 0.3	–	0.8	V
V_{IH}	Input HIGH voltage		All inputs except as listed below	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	V_{BAK} – 0.5	–	V_{BAK} + 0.3	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			PFI (comparator input)	–	–	3.75	V
V_{OH}	Output HIGH voltage	I_{OH} = –2 mA		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		–	–	0.4	V
R_{RST}	Pull-up resistance for $\overline{RST}$ inactive			50	–	400	kΩ
R_{in}	Input resistance (A1-A0)	For $V_{IN} = V_{IL}$(Max)		20	–	–	kΩ
		For $V_{IN} = V_{IH}$(Min)		1	–	–	MΩ
V_{PFI}	Power fail input reference voltage			1.175	1.20	1.225	V
V_{HYS}	Power fail input (PFI) hysteresis (rising)			–	–	100	mV

Notes
5. The minimum V_{DD} to guarantee the level of $\overline{RST}$ remains a valid V_{OL} level.
6. Includes $\overline{RST}$ input detection of external reset condition to trigger driving of $\overline{RST}$ signal by FM31L276/FM31L278.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

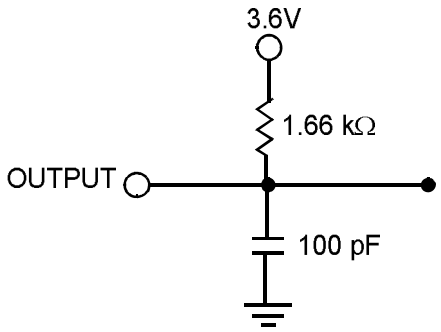
Parameter [7]	Description	Test Conditions	Typ	Max	Unit
C_{IO}	Input/Output pin capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	–	8	pF
C_{XTL} [8]	X1, X2 crystal pin capacitance		12	–	pF

Thermal Resistance

Parameter [7]	Description	Test Conditions	14-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	80	°C/W
Θ_{JC}	Thermal resistance (junction to case)		29	°C/W

AC Test Loads and Waveforms

Figure 23. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels ..... 10% and 90% of V_{DD}

Input rise and fall times ..... 10 ns

Input and output timing reference levels ..... 0.5 × V_{DD}

Output load capacitance ..... 100 pF

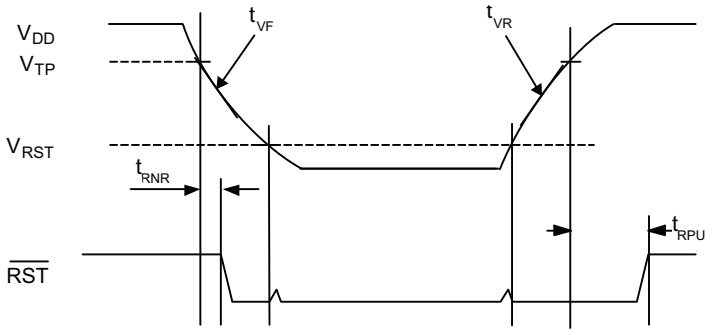
Notes
7. This parameter is characterized and not 100% tested.
8. The crystal attached to the X1/X2 pins must be rated as 6 pF/12.5 pF.

Supervisor Timing

Over the Operating Range

Parameter	Description	Min	Max	Units
t_{RPU}	$\overline{RST}$ active (LOW) after $V_{DD} > V_{TP}$	100	200	ms
t_{RNR}[9]	$\overline{RST}$ response time to $V_{DD} < V_{TP}$ (noise filter)	10	25	µs
t_{VR}[9, 10]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF}[9, 10]	V_{DD} power-down ramp rate	100	–	µs/V
t_{WDP}[11]	Pulse width of $\overline{RST}$ for watchdog reset	100	200	ms
t_{WDOG}[11]	Timeout of watchdog	t_{DOG}	$2 \times t_{DOG}$	ms
f_{CNT}	Frequency of event counters	0	10	MHz
t_{OSC}	RTC Oscillator time to start	–	2	s

Figure 24. $\overline{RST}$ Timing



Notes
9. This parameter is characterized and not 100% tested.
10. Slope measured at any point on V_{DD} waveform.
11. t_{DOG} is the programmed time in register in register 0Ah, $V_{DD} > V_{TP}$, and t_{RPU} satisfied.

AC Switching Characteristics

Over the Operating Range

Parameter[12]		Description	Min	Max	Min	Max	Min	Max	Unit
Cypress Parameter	Alt. Parameter								
f_{SCL}		SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{SU;STA}$		Start condition setup for repeated Start	4.7	–	0.6	–	0.25	–	µs
$t_{HD;STA}$		Start condition hold time	4.0	–	0.6	–	0.25	–	µs
t_{LOW}		Clock LOW period	4.7	–	1.3	–	0.6	–	µs
t_{HIGH}		Clock HIGH period	4.0	–	0.6	–	0.4	–	µs
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	250	–	100	–	100	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	–	0	–	ns
t_{DH}		Data output hold (from SCL @ V_{IL})	0	–	0	–	0	–	ns
t_R[13]	t_r	Input rise time	–	1000	–	300	–	300	ns
t_F[13]	t_f	Input fall time	–	300	–	300	–	100	ns
$t_{SU;STO}$		STOP condition setup	4	–	0.6		0.25	–	µs
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	3	–	0.9	–	0.55	µs
t_{BUF}		Bus free before new transmission	4.7	–	1.3	–	0.5	–	µs
t_{SP}		Noise suppression time constant on SCL, SDA	–	50	–	50	–	50	ns

Figure 25. Read Bus Timing Diagram

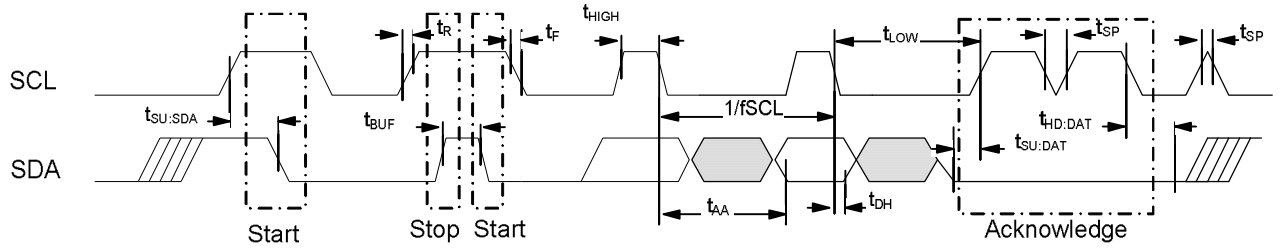
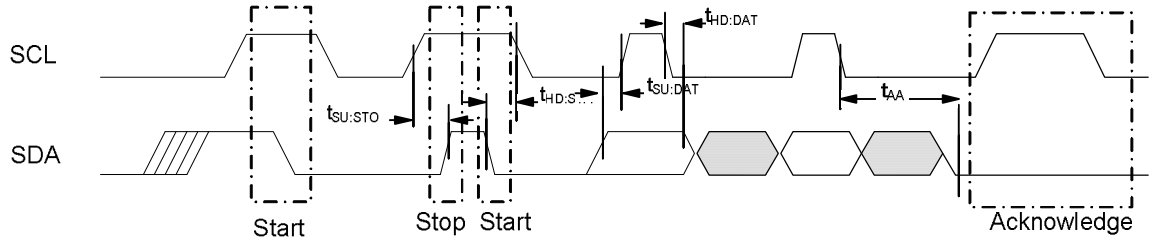


Figure 26. Write Bus Timing Diagram



Notes

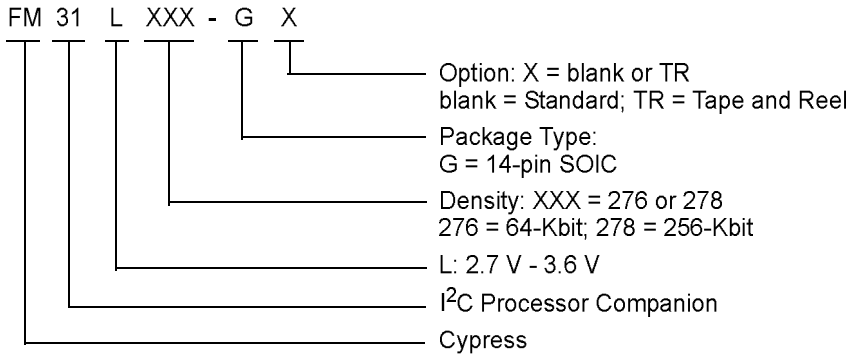
12. Test conditions assume a signal transition time of 10 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 100 pF load capacitance shown in Figure 23 on page 29.
13. This parameter is characterized and not 100% tested.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM31L276-G	51-85067	14-pin SOIC	Industrial
FM31L276-GTR	51-85067	14-pin SOIC	
FM31L278-G	51-85067	14-pin SOIC	
FM31L278-GTR	51-85067	14-pin SOIC	

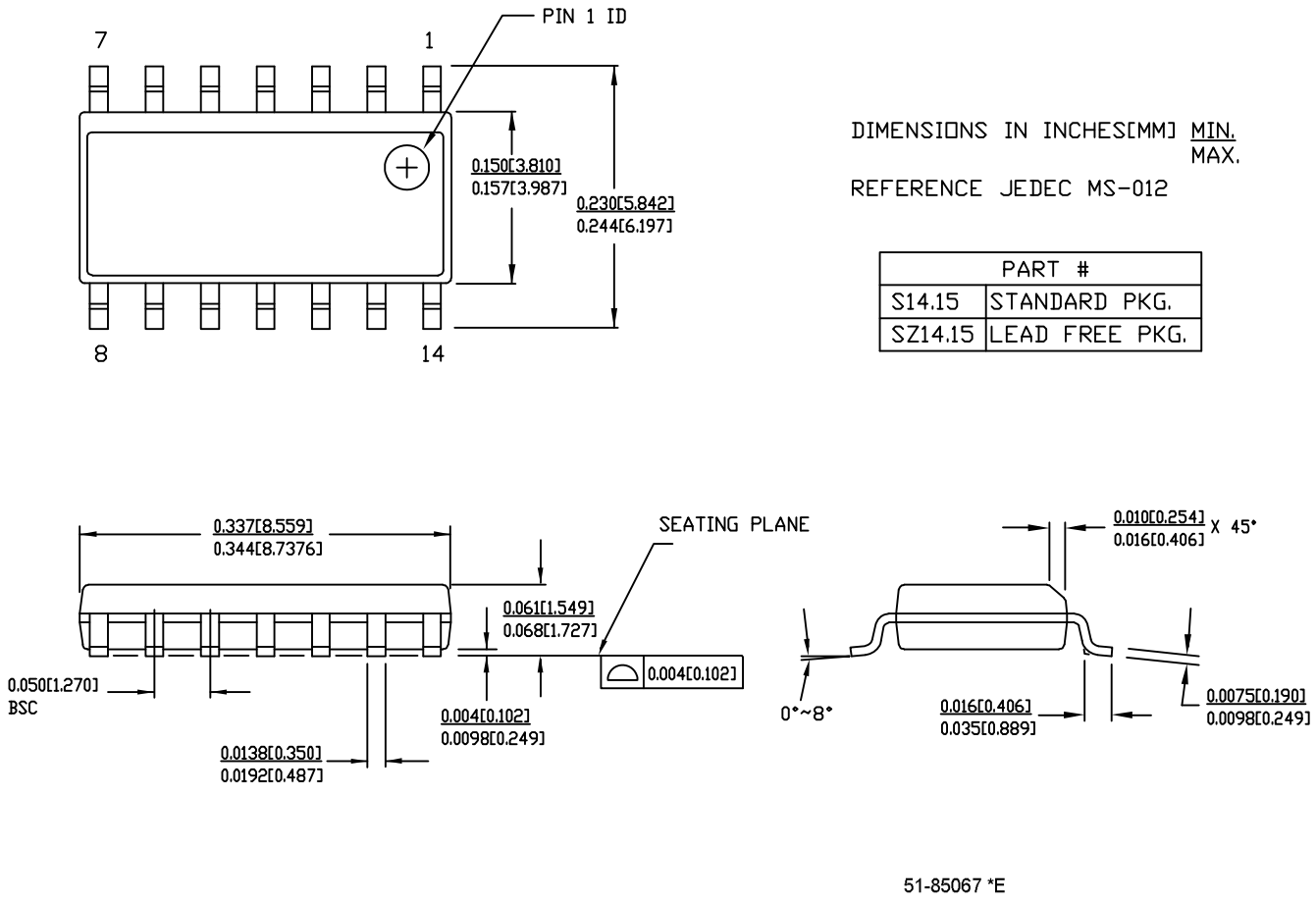
All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 27. 14-pin SOIC (150 Mils) Package Outline, 51-85067



Acronyms

Acronym	Description
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
NMI	Non Maskable interrupt
RoHS	Restriction of Hazardous Substances
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM31L276/FM31L278, 64-Kbit/256-Kbit Integrated Processor Companion with F-RAM Document Number: 001-86392				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3916894	GVCH	02/28/2013	New spec.
*A	4333096	GVCH	05/05/2014	Updated Real-time Clock Operation: Updated Crystal Oscillator: Updated description (Added use of 6 pF crystal). Updated Maximum Ratings: Removed "Package Moisture Sensitivity Level" and its corresponding details. Added "Maximum junction temperature" and its corresponding details. Added "DC voltage applied to outputs in High-Z state" and its corresponding details. Added "Transient voltage (< 20 ns) on any pin to ground potential" and its corresponding details. Added "Package power dissipation capability (T_A = 25 °C)" and its corresponding details. Added "DC output current (1 output at a time, 1s duration)" and its corresponding details. Added "Latch-up current" and its corresponding details. Updated Data Retention and Endurance: Updated details corresponding to T_{DR} parameter (Removed details corresponding to Test Condition "T_A = 80 °C"; added details corresponding to Test Condition "T_A = 65 °C"). Added NV_C parameter and its details. Updated Capacitance: Changed typical value of C_{XTL} parameter from 25 pF to 12 pF. Added Thermal Resistance. Updated Package Diagram: Removed Package Marking Scheme. Updated to Cypress template.
*B	4562106	GVCH	11/05/2014	Updated Functional Description: Added "For a complete list of related documentation, click here." at the end.
*C	6083685	GVCH	02/28/2018	Updated Register Map: Updated Table 6: Removed "VTP1" bit from bit 1 corresponding to address "0Bh". Replaced "VTP0" with "VTP" in bit 0 corresponding to address "0Bh". Updated details in "Description" column corresponding to $\overline{OSCEN}$ (to add t_{OSC} time in the 01h register). Updated Maximum Ratings: Removed "Maximum junction temperature" and its corresponding details. Added "Ambient Temperature with power applied" and its corresponding details. Updated Supervisor Timing: Added t_{OSC} parameter and its details. Updated Package Diagram: spec 51-85067 – Changed revision from *D to *E. Updated to new template.

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FM3164/FM31256

64-Kbit/256-Kbit Integrated Processor Companion with F-RAM

Features

- 64-Kbit/256-Kbit ferroelectric random access memory (F-RAM)
  - Logically organized as 8K × 8 (FM3164)/32K × 8 (FM31256)
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- High Integration Device Replaces Multiple Parts
  - Serial nonvolatile memory
  - Real time clock (RTC)
  - Low voltage reset
  - Watchdog timer
  - Early power-fail warning/NMI
  - Two 16-bit event counter
  - Serial number with write-lock for security
- Real-time Clock/Calendar
  - Backup current at 2 V: 1.15 µA at +25 °C
  - Seconds through centuries in BCD format
  - Tracks leap years through 2099
  - Uses standard 32.768 kHz crystal (6 pF)
  - Software calibration
  - Supports battery or capacitor backup
- Processor Companion
  - Active-low reset output for V_{DD} and watchdog
  - Programmable low-V_{DD} reset trip point
  - Manual reset filtered and debounced
  - Programmable watchdog timer
  - Dual Battery-backed event counter tracks system intrusions or other events
  - Comparator for power-fail interrupt
  - 64-bit programmable serial number with lock
- Fast 2-wire serial interface (I^2C)
  - Up to 1-MHz frequency
  - Supports legacy timings for 100 kHz and 400 kHz
  - RTC, Supervisor controlled via I^2C interface
  - Device select pins for up to 4 memory devices
- Low power consumption
  - 1.5 mA active current at 1 MHz
  - 150 µA standby current
- Operating voltage: V_{DD} = 2.7 V to 5.5 V
- Industrial temperature: –40 °C to +85 °C
- 14-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The FM3164/FM31256 device integrates F-RAM memory with the most commonly needed functions for processor-based systems. Major features include nonvolatile memory, real time clock, low-V_{DD} reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or any other purpose.

The FM3164/FM31256 is a 64-Kbit/256-Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. This memory is truly nonvolatile rather than battery backed. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by other nonvolatile memories. The FM3164/FM31256 is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

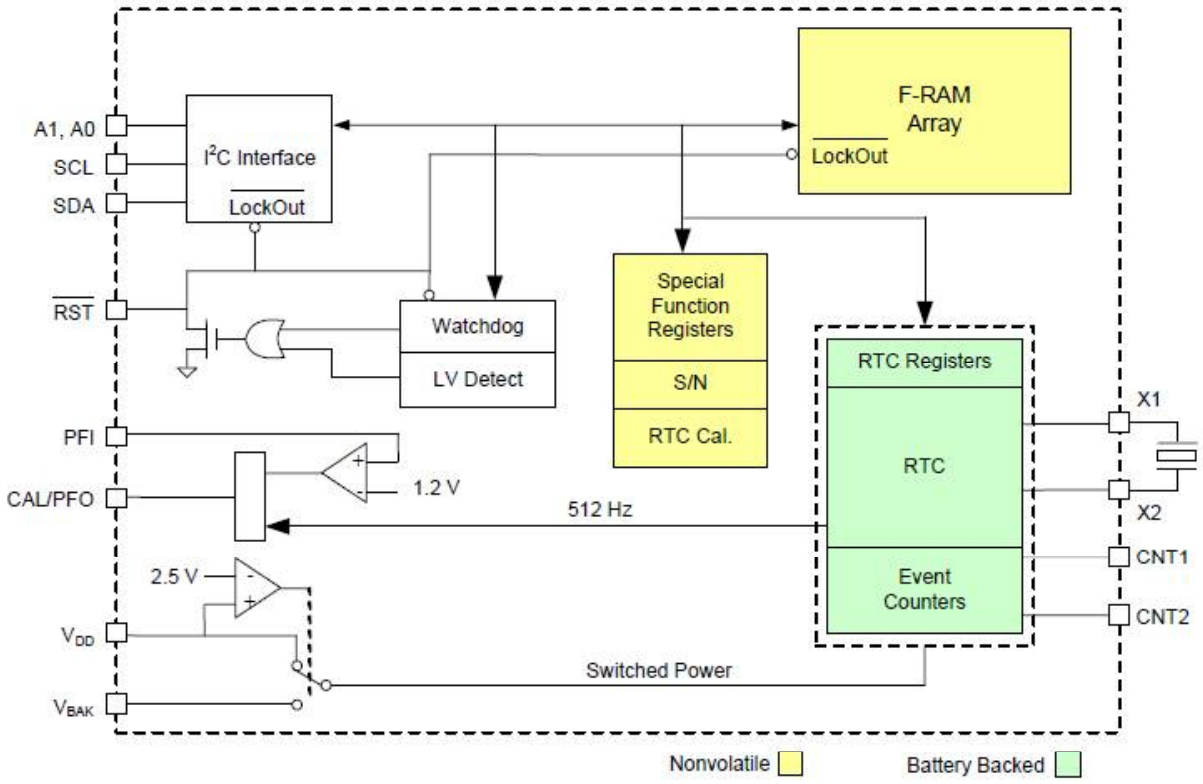
The real time clock (RTC) provides time and date information in BCD format. It can be permanently powered from an external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low V_{DD} condition or a watchdog timeout. $\overline{RST}$ goes active when V_{DD} drops below a programmable threshold and remains active for 100 ms after V_{DD} rises above the trip point. A programmable watchdog timer runs from 100 ms to 3 seconds. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host before the timeout. A flag-bit indicates the source of the reset.

A comparator on PFI compares an external input pin to the onboard 1.2 V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers a dual battery-backed event counter that tracks the number of rising or falling edges detected on a dedicated input pin.

For a complete list of related documentation, click here.

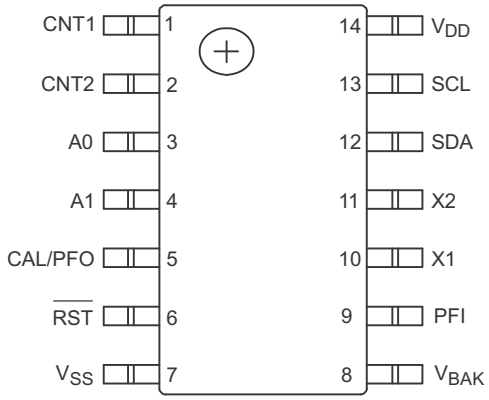
Logic Block Diagram



Contents

Pinout

Figure 1. 14-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A1–A0	Input	**Device Select Address 1-0**. These pins are used to select one of up to 4 devices of the same type on the same I^2C bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data/Address**. This is a bi-directional pin for the I^2C interface. It is open-drain and is intended to be wire-OR'd with other devices on the I^2C bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the I^2C interface. Data is clocked out of the device on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
CNT1, CNT2	Input	**Event Counter Inputs**. These battery-backed inputs increment counters when an edge is detected on the corresponding CNT pin. The polarity is programmable. These pins should not be left floating. Tie to ground if these pins are not used.
X1, X2	Input/Output	32.768 kHz crystal connection. When using an external oscillator, apply the clock to X1 and a DC mid-level to X2. These pins should be left unconnected if RTC is not used.
$\overline{RST}$	Input/Output	**Reset**. This active-low output is open drain with weak pull-up. It is also an input when used as a manual reset. This pin should be left floating if unused.
PFI	Input	**Early Power-fail Input**. Typically connected to an unregulated power supply to detect an early power failure. This pin must be tied to ground if unused.
CAL/PFO	Output	**Calibration/Early Power-fail Output**. In calibration mode, this pin supplies a 512 Hz square-wave output for clock calibration. In normal operation, this is the early power-fail output.
V_{BAK}	Power supply	**Backup supply voltage**. Connected to a 3 V battery or a large value capacitor. If $V_{DD} \leq 3.6$ V and no backup supply is used, this pin should be tied to V_{DD}. If $V_{DD} > 3.6$ V and no backup supply is used, this pin should be left floating and the VBC bit should be set in the RTC register 0Bh.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Functional Overview

The FM3164/FM31256 device combines a serial nonvolatile RAM with a real time clock (RTC) and a processor companion. The companion is a highly integrated peripheral including a processor supervisor, a comparator used for early power-fail warning, nonvolatile event counters, and a 64-bit serial number. The FM3164/FM31256 integrates these complementary but distinct functions under a common interface in a single package. The product is organized as two logical devices. The first is a memory and the second is the companion which includes all the remaining functions. From the system perspective they appear to be two separate devices with unique IDs on the serial bus.

The memory is organized as a standalone nonvolatile I^2C memory using standard device ID value. The real time clock and supervisor functions are accessed with a separate I^2C device ID. This allows clock/calendar data to be read while maintaining the most recently used memory address. The clock and supervisor functions are controlled by 25 special function registers. The RTC and event counter circuits are maintained by the power source on the V_{BAK} pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Architecture

The FM3164/FM31256 device is available in memory size 64-Kbit/256-Kbit. The device uses two-byte addressing for the memory portion of the chip. This makes the device software compatible with its standalone memory counterparts, but makes them compatible within the entire family.

The memory array is logically organized as 8,192 × 8 bits/ 32,768 × 8 bits and is accessed using an industry-standard I^2C interface. The memory is based on F-RAM technology. Therefore it can be treated as RAM and is read or written at the speed of the I^2C bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The I^2C protocol is described on page 20.

The memory array can be write-protected by software. Two bits in the processor companion area (WP1, WP0 in register 0Bh) control the protection setting. Based on the setting, the protected addresses cannot be written and the I^2C interface will not acknowledge any data to protected addresses. The special function registers containing these bits are described in detail below.

Table 1. Block Memory Write Protection

WP1	WP0	Protected Address Range
0	0	None
0	1	Bottom 1/4
1	0	Bottom 1/2
1	1	Full array

Processor Companion

In addition to nonvolatile RAM, the FM3164/FM31256 incorporates a real time clock and highly integrated processor companion. The companion includes a low-V_{DD} reset, a programmable watchdog timer, a battery-backed event counters, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

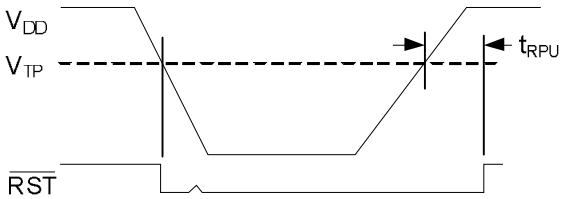
Supervisors provide a host processor two basic functions: detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. The FM3164/FM31256 has a reset pin ($\overline{RST}$) to drive a processor reset input during power faults, power-up, and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the $\overline{RST}$ pin. When V_{DD} is above the programmed trip point, $\overline{RST}$ output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}), the $\overline{RST}$ pin will be driven LOW. It will remain LOW until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, $\overline{RST}$ continues to drive LOW for at least 100 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the $\overline{RST}$ pin will return to the weak HIGH state. While $\overline{RST}$ is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

Table 1 below shows how bits VTP(1:0) control the trip point of the low-V_{DD} reset. They are located in register 0Bh, bits 1 and 0. The reset pin will drive LOW when V_{DD} is below the selected V_{TP} voltage, and the I^2C interface and F-RAM array will be locked out. Figure 2 illustrates the reset operation in response to a low V_{DD}.

Table 2. VTP setting

VTP Setting	VTP1	VTP0
2.6 V	0	0
2.9 V	0	1
3.9 V	1	0
4.4 V	1	1

Figure 2. Low V_{DD} Reset

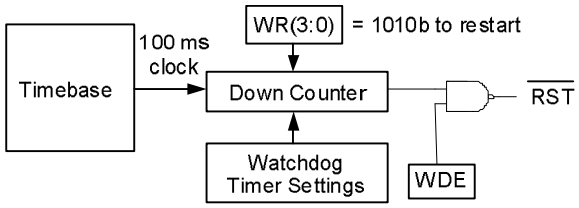


A watchdog timer can also be used to drive an active reset signal. The watchdog is a free-running programmable timer. The timeout period can be software programmed from 100 ms to 3 seconds in 100 ms increments via a 5-bit nonvolatile register. All programmed settings are minimum values and vary with temperature according to the operating specifications. The watchdog has two additional controls associated with its operation, a watchdog enable bit (WDE) and timer restart bits (WR). Both the enable bit must be set and the watchdog must timeout in order to drive $\overline{RST}$ active. If a reset event occurs, the timer will automatically restart on the rising edge of the reset pulse. If WDE = '0', the watchdog timer runs but a watchdog fault will not cause $\overline{RST}$ to be asserted LOW. The WTR flag will be set, indicating a watchdog fault. This setting is useful during software development if the developer does not want $\overline{RST}$ to drive. Note that setting the maximum timeout setting (11111b) disables the counter to save power. The second control is a nibble that restarts the timer preventing a reset. The timer should be restarted after changing the timeout value.

The watchdog timeout value is located in register 0Ah, bits 4:0, and the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 09h. Writing this pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout period will be set immediately after enabling. The watchdog is disabled when V_{DD} is below V_{TP}. The following table summarizes the watchdog bits. A block diagram follows.

Watchdog Timeout	WDT(4:0)	0Ah, bits 4:0
Watchdog Enable	WDE	0Ah, bit 7
Watchdog Restart	WR(3:0)	09h, bits 3:0

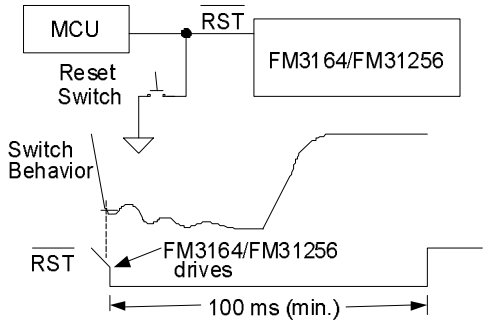
Figure 3. Watchdog Timer



Manual Reset

The $\overline{RST}$ is a bi-directional signal allowing the FM3164/FM31256 to filter and de-bounce a manual reset switch. The $\overline{RST}$ input detects an external low condition and responds by driving the $\overline{RST}$ signal LOW for 100 ms.

Figure 4. Manual Reset



Note The internal weak pull-up eliminates the need for additional external components.

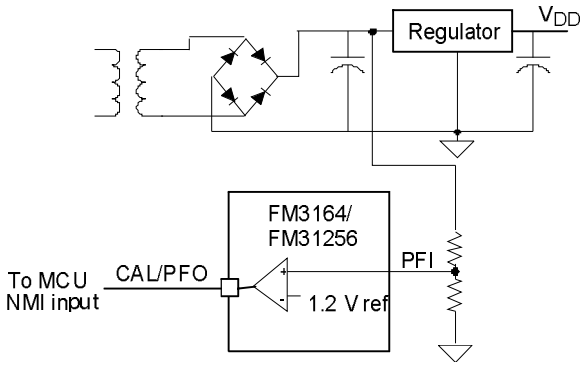
Reset Flags

In case of a reset condition, a flag bit will be set to indicate the source of the reset. A low-V_{DD} reset is indicated by the POR flag, register 09h, bit 6. A watchdog reset is indicated by the WTR flag, register 09h, bit 7. Note that the flags are internally set in response to reset sources, but they must be cleared by the user. When the register is read, it is possible that both flags are set if both have occurred since the user last cleared them.

Early Power Fail Comparator

An early power fail warning can be provided to the processor well before V_{DD} drops out of spec. The comparator is used to create a power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to the unregulated power supply via a resistor divider. An application circuit is shown below.

Figure 5. Comparator as a Power-Fail Warning



The voltage on the PFI input pin is compared to an onboard 1.2 V reference. When the PFI input voltage drops below this threshold, the comparator will drive the CAL/PFO pin to a LOW state. The comparator has 100 mV (max) of hysteresis to reduce noise sensitivity, only for a rising PFI signal. For a falling PFI edge, there is no hysteresis.

The comparator is a general purpose device and its application is not limited to the NMI function.

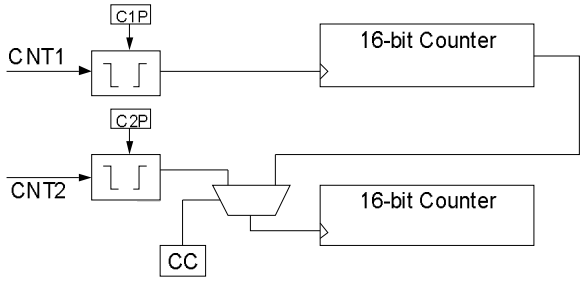
The comparator is not integrated into the special function registers except as it shares its output pin with the CAL output. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the CAL/PFO output pin will be driven with a 512 Hz square wave and the comparator will be ignored. Since most users only invoke the calibration mode during production, this should have no impact on system operations using the comparator.

Note The maximum voltage on the comparator input PFI is limited to 3.75 V under normal operating conditions.

Event Counter

The FM3164/FM31256 offers the user two battery-backed event counters. Input pins CNT1 and CNT2 are programmable edge detectors. Each clocks a 16-bit counter. When an edge occurs, the counters will increment their respective registers. Counter 1 is located in registers 0Dh and 0Eh, Counter 2 is located in registers 0Fh and 10h. These register values can be read anytime V_{DD} is above V_{TP}, and they will be incremented as long as a valid V_{BAK} power source is provided. To read, set the RC bit (register 0Ch, bit 3) to 1. This takes a snapshot of all four counter bytes allowing a stable value even if a count occurs during the read. The registers can be written by software allowing the counters to be cleared or initialized by the system. Counts are blocked during a write operation. The two counters can be cascaded to create a single 32-bit counter by setting the CC control bit (register 0Ch, bit 2). When cascaded, the CNT1 input will cause the counter to increment. CNT2 is not used in this mode and should be tied to ground.

Figure 6. Event Counter



The control bits for event counting are located in register 0Ch. Counter 1 Polarity is bit C1P, bit 0; Counter 2 Polarity is C2P, bit 1; the Cascade Control is CC, bit 2; and the Read Counter bit is RC, bit 3.

The polarity bits must be set prior to setting the counter value(s). If a polarity bit is changed, the counter may inadvertently increment. If the counter pins are not being used, tie them to ground.

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writeable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via the device ID for the Processor Companion. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. However, once the lock bit is set, the values cannot be altered and the lock cannot be removed. Once locked the serial number registers can still be read by the system.

The serial number is located in registers 11h to 18h. The lock bit is SNL (register 0Bh, bit 7). Setting the SNL bit to a '1' disables writes to the serial number registers, and the SNL bit cannot be cleared.

Real-time Clock Operation

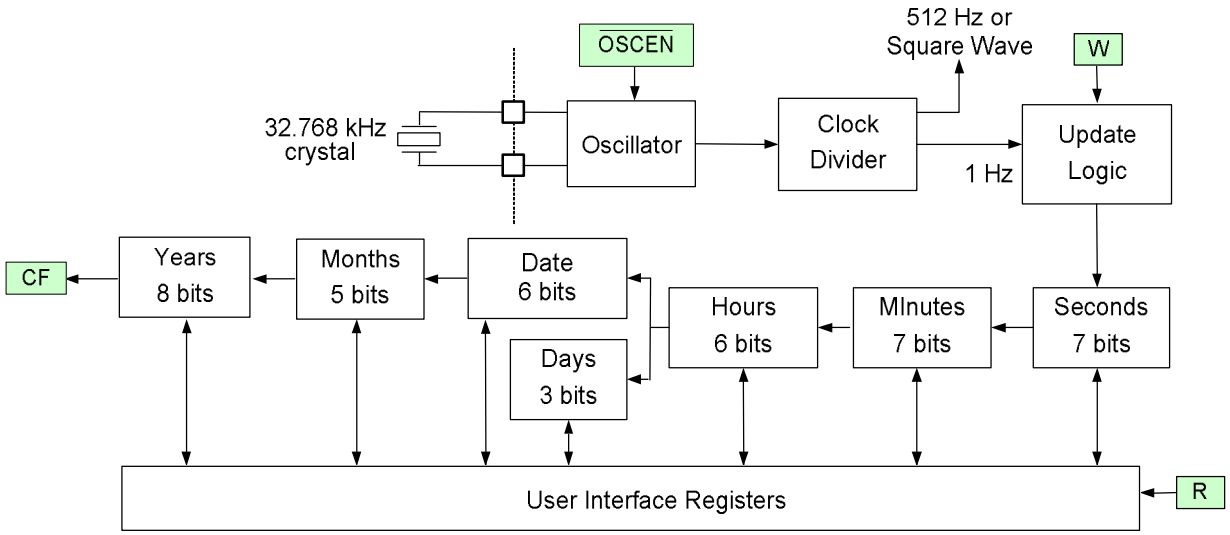
The real-time clock (RTC) is a timekeeping device that can be battery or capacitor backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1 Hz). Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram (Figure 7 on page 8) illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h described below. Changing the R bit from '0' to '1' transfers timekeeping information from the core into holding registers that can be read by the user. If a timekeeper update is pending when R is set, then the core will be updated prior to loading the user registers. The registers are frozen and will not be updated again until the R bit is cleared to '0'. R is used for reading the time.

Setting the W bit to '1' locks the user registers. Clearing it to '0' causes the values in the user registers to be loaded into the timekeeper core. W bit is used for writing new time values. Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

Figure 7. Real-time Clock Core Block Diagram

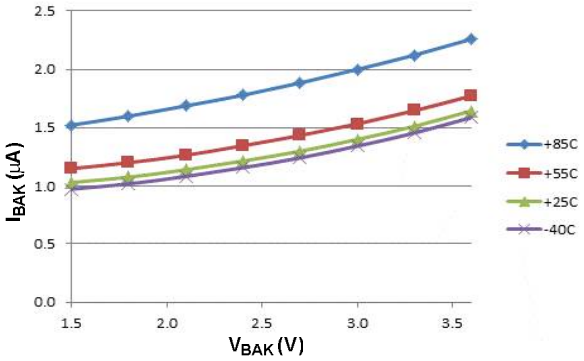


Backup Power

The real-time clock/calendar is intended to be permanently powered. When the primary system power fails, the voltage on the V_{DD} pin will drop. When V_{DD} is less than 2.5 V, the RTC (and event counters) will switch to the backup power supply on V_{BAK}. The clock operates at extremely low current in order to maximize battery or capacitor life. However, an advantage of combining a clock function with F-RAM memory is that data is not lost regardless of the backup power source.

The I_{BAK} current varies with temperature and voltage (see DC Electrical Characteristics on page 26). The following graph shows I_{BAK} as a function of V_{BAK}. These curves are useful for calculating backup time when a capacitor is used as the V_{BAK} source.

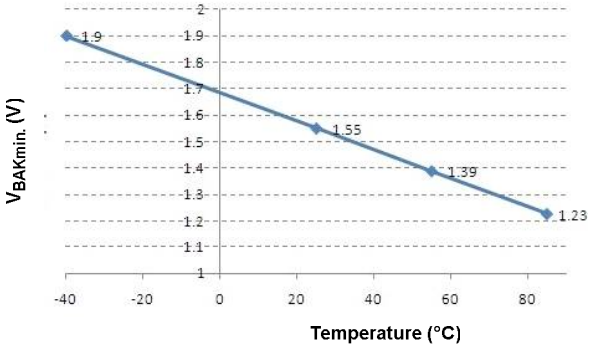
Figure 8. I_{BAK} vs. V_{BAK} Voltage



The minimum V_{BAK} voltage varies linearly with temperature. The user can expect the minimum V_{BAK} voltage to be 1.23 V at +85 °C and 1.90 V at -40 °C. The tested limit is 1.55 V at +25 °C.

Note The minimum V_{BAK} voltage has been characterized at -40 °C and +85 °C but is not 100% tested.

Figure 9. V_{BAK}(min.) vs Temperature



Trickle Charger

To facilitate capacitor backup the V_{BAK} pin can optionally provide a trickle charge current. When the VBC bit (register 0Bh, bit 2) is set to '1', the V_{BAK} pin will source approximately 15 µA until V_{BAK} reaches V_{DD} or 3.75 V, whichever is less. In 3 V systems, this charges the capacitor to V_{DD} without an external diode and resistor charger. In 5 V systems, it provides the same convenience and also prevents the user from exceeding the V_{BAK} maximum voltage specification.

In the case where no battery is used, the V_{BAK} pin should be tied according to the following conditions:

- For 3.3 V systems, V_{BAK} should be tied to V_{DD}. This assumes V_{DD} does not exceed 3.75 V.
- For 5 V systems, attach a 1 µF capacitor to V_{BAK} and turn the trickle charger on. The V_{BAK} pin will charge to the internal backup voltage which regulates itself to about 3.6 V. V_{BAK} should not be tied to 5 V since the V_{BAK}(max) specification will be exceeded. A 1 µF capacitor will keep the companion functions working for about 1.5 second.

Although V_{BAK} may be connected to V_{SS}, this is not recommended if the companion is used. None of the companion functions will operate below about 2.5 V

Note Systems using lithium batteries should clear the VBC bit to '0' to prevent battery charging. The V_{BAK} circuitry includes an internal 1 KΩ series resistor as a safety element.

Calibration

When the CAL bit in the register 00h is set to '1', the clock enters calibration mode. In calibration mode, the CAL/PFO output pin is dedicated to the calibration function and the power fail output is temporarily unavailable. Calibration operates by applying a digital correction to the counter based on the frequency error. In this mode, the CAL/PFO pin is driven with a 512 Hz (nominal) square wave. Any measured deviation from 512 Hz translates into a timekeeping error. The user converts the measured error in ppm and writes the appropriate correction value to the calibration register. The correction factors are listed in the table below. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to '1', whereas negative ppm adjustments have CALS = '0'. After calibration, the clock will have a maximum error of ±2.17 ppm or ±0.09 minutes per month at the calibrated temperature.

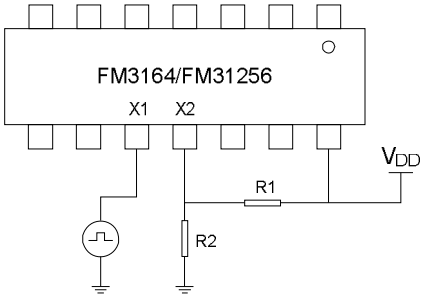
The calibration setting is stored in F-RAM so it is not lost should the backup source fail. It is accessed with bits CAL(4:0) in register 01h. This value can be written only when the CAL bit is set to a '1'. To exit the calibration mode, the user must clear the CAL bit to a '0'. When the CAL bit is '0', the CAL/PFO pin will revert to the power fail output function.

Crystal Oscillator

The crystal oscillator is designed to use a 6 pF crystal without the need for external components, such as loading capacitors. The FM3164/FM31256 device has built-in loading capacitors that are optimized for use with 6 pF crystals.

If a 32.768 kHz crystal is not used, an external oscillator may be connected to the FM3164/FM31256. Apply the oscillator to the X1 pin. Its high and low voltage levels can be driven rail-to-rail or amplitudes as low as approximately 500 mV p-p. To ensure proper operation, a DC bias must be applied to the X2 pin. It should be centered between the high and low levels on the X1 pin. This can be accomplished with a voltage divider.

Figure 10. External Oscillator

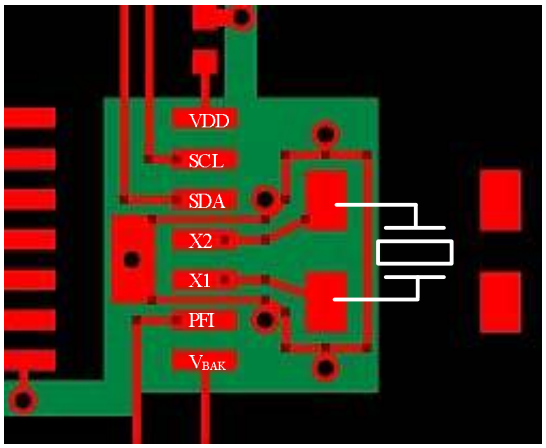


In the example, R1 and R2 are chosen such that the X2 voltage is centered around the X1 oscillator drive levels. If you wish to avoid the DC current, you may choose to drive X1 with an external clock and X2 with an inverted clock using a CMOS inverter.

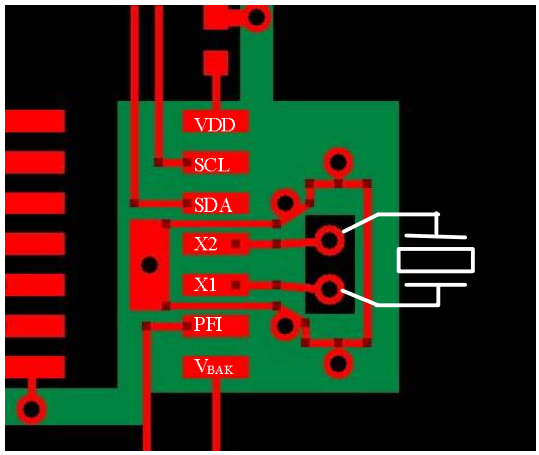
Layout Recommendations

The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring must be placed around these pads and the guard ring grounded. SDA and SCL traces should be routed away from the X1 / X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.

Figure 11. Layout Recommendations



Layout for Surface Mount Crystal
(red = top layer, green = bottom layer)



Layout for Through Hole Crystal
(red = top layer, green = bottom layer)

Table 3. Digital Calibration Adjustments

Positive Calibration for slow clocks: Calibration will achieve ±2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

Table 3. Digital Calibration Adjustments (continued)

Positive Calibration for slow clocks: Calibration will achieve ±2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001
2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

Register Map

The RTC and processor companion functions are accessed via 25 special function registers, which are mapped to a separate I^2C device ID. The interface protocol is described on I2C Interface on page 20. The registers contain timekeeping data, control bits, and information flags. A description of each register follows the summary table.

Table 4. Register Map Summary Table

Nonvolatile = ☐ Battery-backed = ☐

Address	Data								Function	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
18h	Serial Number Byte 7								Serial Number 7	FFh
17h	Serial Number Byte 6								Serial Number 6	FFh
16h	Serial Number Byte 5								Serial Number 5	FFh
15h	Serial Number Byte 4								Serial Number 4	FFh
14h	Serial Number Byte 3								Serial Number 3	FFh
13h	Serial Number Byte 2								Serial Number 2	FFh
12h	Serial Number Byte 1								Serial Number 1	FFh
11h	Serial Number Byte 0								Serial Number 0	FFh
10h	Counter 2 MSB								Event Counter 2 MSB	FFh
0Fh	Counter 2 LSB								Event Counter 2 LSB	FFh
0Eh	Counter 1 MSB								Event Counter 1 MSB	FFh
0Dh	Counter 1 LSB								Event Counter 1 LSB	FFh
0Ch					RC	CC	C2P	C1P	Event Count Control	
0Bh	SNL	–	–	WP1	WP0	VBC	VTP1	VTP0	Companion Control	
0Ah	WDE	–	–	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog Control	
09h	WTR	POR	LB	–	WR3	WR2	WR1	WR0	Watchdog Restart/Flags	
08h	10 years				years				Years	00–99
07h	0	0	0	10 months	months				Month	01–12
06h	0	0	10 date		date				Date	01–31
05h	0	0	0	0	0	day			Day	01–07
04h	0	0	10 hours		hours				Hours	00–23
03h	0	10 minutes			minutes				Minutes	00–59
02h	0	10 seconds			seconds				Seconds	00–59
01h	$\overline{\text{OSCEN}}$	reserved	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL Control	
00h	reserved	CF	reserved	reserved	reserved	CAL	W	R	RTC Control	

Note When the device is first powered up and programmed, all timekeeping registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers. All other register values should be treated as unknown.

Table 5. Default Register Values

Address	Hex Value
18h	0x00
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00
12h	0x00
11h	0x00
0Bh	0x00

Address	Hex Value
0Ah	0x1F
08h	0x00
07h	0x01
06h	0x01
05h	0x01
04h	0x00
03h	0x01
02h	0x00
01h	0x80

Table 6. Register Description

Address	Description							
18h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
	Upper byte of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
17h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
	Byte 6 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
16h	**Serial Number Byte 5**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
	Byte 5 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
15h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
	Byte 4 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
14h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24
	Byte 3 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
13h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
	Byte 2 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
12h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
	Byte 1 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							

Table 6. Register Description (continued)

Address	Description							
11h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	LSB of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
10h	**Counter 2 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.15	C2.14	C2.13	C2.12	C2.11	C2.10	C2.9	C2.8
	Event Counter 2 MSB. Increments on overflows from Counter 2 LSB. Battery-backed, read/write.							
0Fh	**Counter 2 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
	Event Counter 2 LSB. Increments on programmed edge event on CNT2 input or overflows from Counter 1 MSB when CC = '1'. Battery-backed, read/write.							
0Eh	**Counter 1 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.15	C1.14	C1.13	C1.12	C1.11	C1.10	C1.9	C1.8
	Event Counter 1MSB. Increments on overflows from Counter 1 LSB. Battery-backed, read/write.							
0Dh	**Counter 1 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Event Counter 1 LSB. Increments on programmed edge event on CNT1 input. Battery-backed, read/write.							
0Ch	**Event Counter Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	–	–	–	–	RC	CC	C2P	C1P
RC	Read Counter. Setting this bit to '1' takes a snapshot of the four counters bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.							
CC	Counter Cascade. When CC = '0', the event counters operate independently according to the edge programmed by C1P and C2P respectively. When CC = '1', the counters are cascaded to create one 32-bit counter. The registers of Counter 2 represent the most significant 16-bits of the counter and CNT1 is the controlling input. Bit C2P is don't care when CC = '1'. Battery-backed, read/write.							
C2P	CNT2 detects falling edges when C2P = '0', rising edges when C2P = '1'. C2P is "don't care" when CC = '1'. The value of Event Counter 2 may inadvertently increment if C2P is changed. Battery-backed, read/write.							
C1P	CNT1 detects falling edges when C1P = '0', rising edges when C1P = '1'. The value of Event Counter 1 may inadvertently increment if C1P is changed. Battery-backed, read/write.							
0Bh	**Companion Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SNL	–	–	WP1	WP0	VBC	VTP1	VTP0
SNL	Serial Number Lock: Setting to a '1' makes registers 11h to 18h and SNL permanently read-only. SNL cannot be cleared once set to '1'. Nonvolatile, read/write.							

Table 6. Register Description (continued)

Address	Description
WP(1:0)	Write Protect. These bits control the write protection of the memory array. Nonvolatile, read/write. Write protect address: WP1 = 0, WP0 = 0 → None WP1 = 0, WP0 = 1 → Bottom 1/4 WP1 = 1, WP0 = 0 → Bottom 1/2 WP1 = 1, WP0 = 1 → Full array
VBC	V_{BAK} Charger Control. Setting VBC to '1' causes a 15 µA trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.
VTP(1:0)	VTP Select. These bits control the reset trip point for the low V_{DD} reset function. Nonvolatile, read/write. VTP = 2.60 V: VTP1 = 0, VTP0 = 0 VTP = 2.90 V: VTP1 = 0, VTP0 = 1 VTP = 3.90 V: VTP1 = 1, VTP0 = 0 VTP = 4.40 V: VTP1 = 1, VTP0 = 1

0Ah	Watchdog Control							
	D7	D6	D5	D4	D3	D2	D1	D0
	WDE	–	–	WDT4	WDT3	WDT2	WDT1	WDT0

WDE	Watchdog Enable. When WDE = '1', a watchdog timer fault will cause the $\overline{RST}$ signal to go active. When WDE = '0' the timer runs but has no effect on $\overline{RST}$, however the WTR flag will be set when a fault occurs. Note as the timer is free-running, users should restart the timer using WR(3:0) prior to setting WDE = '1'. This assures a full watchdog timeout interval occurs. Nonvolatile, read/write.
WDT(4:0)	Watchdog Timeout. Indicates the minimum watchdog timeout interval with 100 ms resolution. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). Nonvolatile, read/write. Invalid - default 100 ms: WDT4 = 0, WDT3 = 0, WDT2 = 0, WDT1 = 0, WDT0 = 0 100 ms: 0, 0, 0, 0, 1 200 ms: 0, 0, 0, 1, 0 300 ms: 0, 0, 0, 1, 1 . . 2000 ms: 1, 0, 1, 0, 0 2100 ms: 1, 0, 1, 0, 1 2200 ms: 1, 0, 1, 1, 0 . . 2900 ms: 1, 1, 1, 0, 1 3000 ms: 1, 1, 1, 1, 0 Disable Counter: 1, 1, 1, 1, 1

09h	Watchdog Restart and Flags							
	D7	D6	D5	D4	D3	D2	D1	D0
	WTR	POR	LB	–	WR3	WR2	WR1	WR0

Table 6. Register Description (continued)

Address	Description							
WTR	Watchdog Timer Reset Flag: When a watchdog timer fault occurs, the WTR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).							
POR	Power-on Reset Flag: When the $\overline{RST}$ pin is activated by $V_{DD} < V_{TP}$ the POR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).							
LB	Low Backup Flag: On power up, if the V_{BAK} source is below the minimum voltage to operate the RTC and event counters, this bit will be set to '1'. The user should clear it to '0' when initializing the system. Battery-backed. Read/Write (internally set, user can clear bit).							
WR(3:0)	Watchdog Restart: Writing a pattern 1010b to WR(3:0) restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR(3:0) has no effect on the timer. This allows users to clear the WTR, POR, and LB flags without affecting the watchdog timer. Battery-backed, Write-only.							
08h	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99. Battery-backed, read/write.							
07h	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12. Battery-backed, read/write.							
06h	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1–31. Battery-backed, read/write.							
05h	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.							
04h	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours.2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23. Battery-backed, read/write.							

Table 6. Register Description (continued)

Address	Description							
03h	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59. Battery-backed, read/write.							
02h	**Timekeeping – Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0–59. Battery-backed, read/write.							
01h	**CAL/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{\text{OSCEN}}$	Reserved	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0
$\overline{\text{OSCEN}}$	Oscillator Enable. When set to '1', the oscillator is halted. When set to '0', the oscillator starts running after t_{OSC} time. Disabling the oscillator can save battery power during storage. On a power-up without battery, this bit is set to '1'. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to '0'.							
CALS	Calibration Sign: Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit can be written only when CAL = '1'. Nonvolatile, read/write.							
CAL(4:0)	Calibration Setting: These five bits control the calibration of the clock. These bits can be written only when CAL = '1'. Nonvolatile, read/write.							
00h	**RTC Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	Reserved	CF	Reserved	Reserved	Reserved	CAL	W	R
CF	Century Overflow Flag. This bit is set to a '1' when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to '0' when the Flag register is read. It is read-only for the user. Battery-backed.							
CAL	Calibration Setting. When set to '1', the clock enters calibration mode. When CAL is set to '0', the clock operates normally, and the CAL/PFO pin is controlled by the power fail comparator. Battery-backed, read/write.							
W	Write Time. Setting the W bit to '1' freezes the clock. The user can then write the timekeeping registers with updated values. Resetting the W bit to '0' causes the contents of the time registers to be transferred to the timekeeping counters and restarts the clock. Battery-backed, read/write.							
R	Read Time. Setting the R bit to '1' copies a static image of the timekeeping core and place it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from '0' to '1' causes the timekeeping capture, so the bit must be returned to '0' prior to reading again. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to '0'.							

I²C Interface

The FM3164/FM31256 employs an industry standard I²C bus that is familiar to many users. This product is unique since it incorporates two logical devices in one chip. Each logical device can be accessed individually. Although monolithic, it appears to the system software to be two separate products. One is a memory device. It has a Slave Address (Slave ID = 1010b) that operates the same as a stand-alone memory device. The second device is a real-time clock and processor companion which have a unique Slave Address (Slave ID = 1101b).

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM3164/FM31256 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 12 and Figure 13 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM3164/FM31256 should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM3164/FM31256 for a new operation.

If during operation the power supply drops below the specified V_{TP} minimum, any I²C transaction in progress will be aborted and the system should issue a START condition prior to performing another operation.

Figure 12. START and STOP Conditions

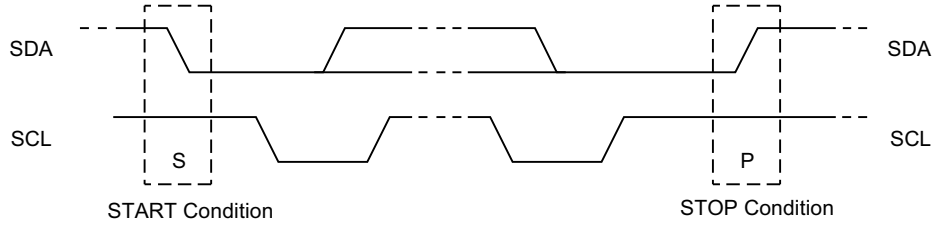
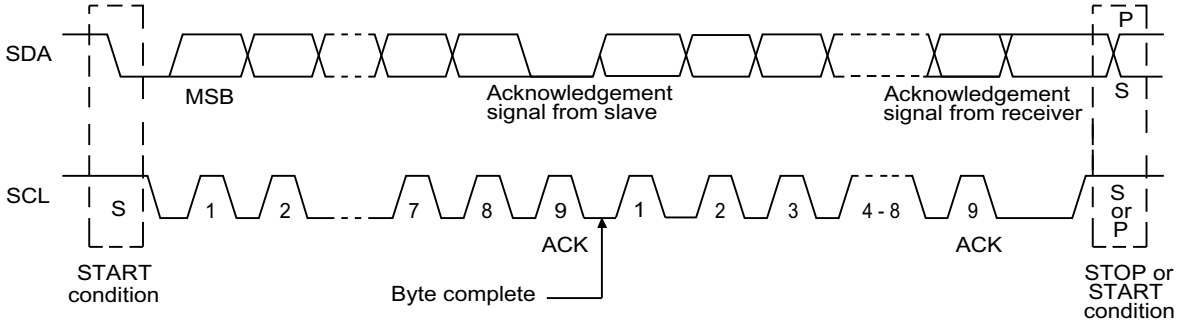


Figure 13. Data Transfer on the I²C Bus



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

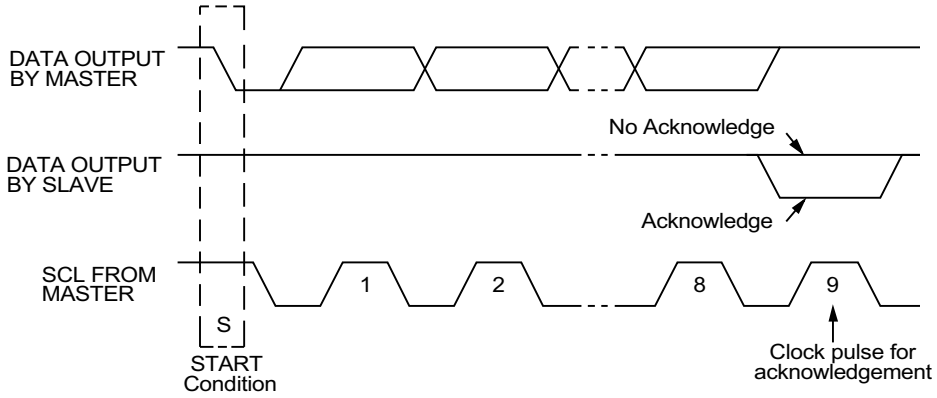
Acknowledge/No-acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the device can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM3164/FM31256 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM3164/FM31256 to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 14. Acknowledge on the I²C Bus



Slave Address

The first byte that the FM3164/FM31256 expects after a START condition is the slave address. As shown in Figure 15 and Figure 16, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

The FM3164/FM31256 has two Slave Addresses (Slave IDs) associated with two logical devices. Bits 7-4 are the device type (slave ID) and should be set to 1010b for the memory device. The other logical device within the FM3164/FM31256 is the real-time clock and companion. Bits 7-4 are the device type (slave ID) and should be set to 1101b for the RTC and companion. A bus transaction with this slave address will not affect the memory in any way. The figures below illustrate the two Slave Addresses.

Bits 2–1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to four FM3164/FM31256 devices can reside on the same I^2C bus by assigning a different address to each. Bit 0 is the read/write bit (R/$\overline{W}$). R/$\overline{W}$ = '1' indicates a read operation and R/$\overline{W}$ = '0' indicates a write operation.

Figure 15. Memory Slave Device Address

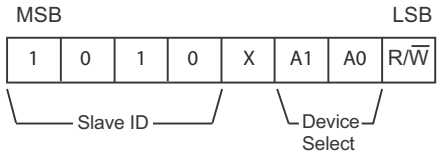
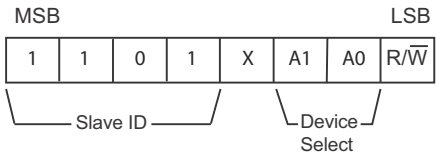


Figure 16. Companion Slave Device Address



Addressing Overview - Memory

After the FM3164/FM31256 (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 15-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as $V_{DD} > V_{TP}$ or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM3164/FM31256 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Addressing Overview - RTC & Companion

The RTC and Processor Companion operate in a similar manner to the memory, except that it uses only one byte of address. Addresses 00h to 18h correspond to special function registers. Attempting to load addresses above 18h is an illegal condition; the FM3164/FM31256 will return a NACK and abort the I^2C transaction.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM3164/FM31256 can begin. For a read operation the FM3164/FM31256 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM3164/FM31256 will transfer the next sequential byte. If the acknowledge is not sent, the FM3164/FM31256 will end the read operation. For a write operation, the FM3164/FM31256 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM3164/FM31256 is designed to operate in a manner very similar to other I^2C interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM3164/FM31256 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

The memory address for FM3164 range from 0x0000 to 0x1FFFF, and for FM31256, they range from 0x0000 to 0x7FFF. Memory functionality is described with respect to FM31256 in the following sections.

Memory Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/$\overline{W}$ bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM3164/FM31256 uses no page buffering.

Figure 17 and Figure 18 below illustrate a single-byte and multiple-byte write cycles.

Figure 17. Single-Byte Write

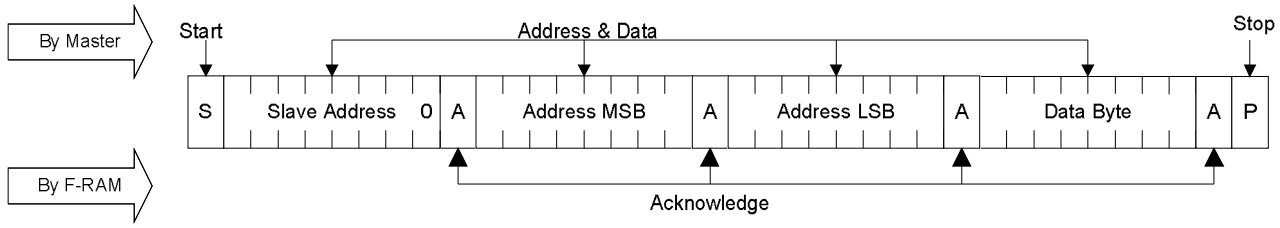
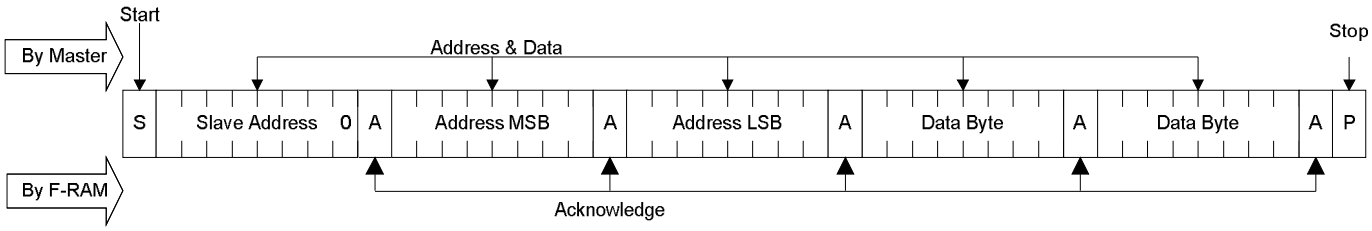


Figure 18. Multi-Byte Write



Memory Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM3164/FM31256 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM3164/FM31256 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM3164/FM31256 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM3164/FM31256 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM3164/FM31256 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. Figure 19 and Figure 20 below show the proper operation for current address reads.

Figure 19. Current Address Read

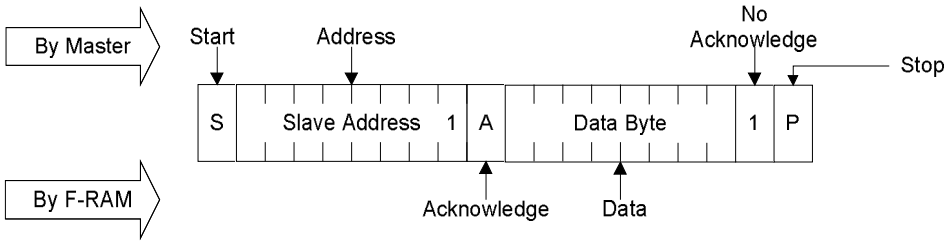
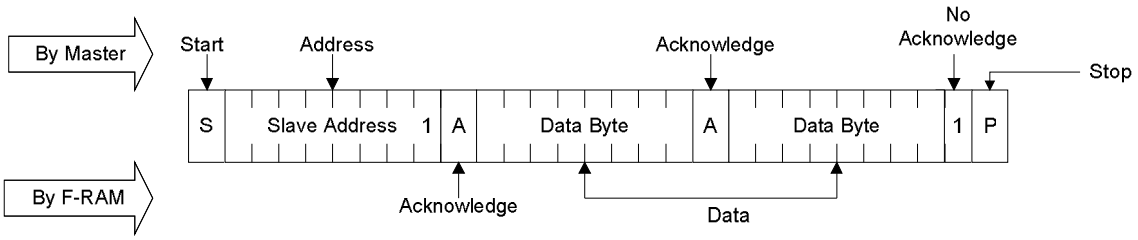


Figure 20. Sequential Read

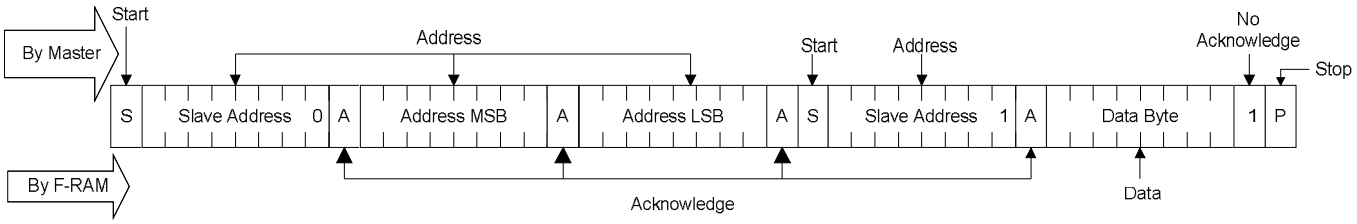


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB ($R/\overline{W}$) set to '0'. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM3164/FM31256 acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 21. Selective (Random) Read

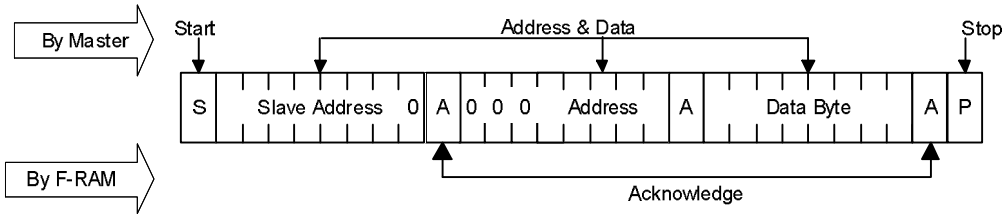


RTC/Companion Write Operation

All RTC and Companion writes operate in a similar manner to memory writes. The distinction is that a different device ID is used and only one byte address is needed instead of two byte address. Figure 22 illustrates a single byte write to this device.

Note Although not required, it is recommended that A5-A7 in the register address byte are zeros in order to preserve compatibility with future devices.

Figure 22. Single Byte Write



RTC/Companion Read Operation

As with writes, a read operation begins with the Slave Address. To perform a register read, the bus master supplies a Slave Address with the LSB set to '1'. This indicates that a read operation is requested. After receiving the complete Slave Address, the FM3164/FM31256 will begin shifting data out from the current register address on the next clock. Auto-increment operates for the special function registers as with the memory address. A current address read for the registers look exactly like the memory except that the device ID is different.

The FM3164/FM31256 contains two separate address registers, one for the memory address and the other for the register address. This allows the contents of one address register to be modified without affecting the current address of the other register. For example, this would allow an interrupted read to the memory while still providing fast access to an RTC register. A subsequent memory read will then continue from the memory address where it previously left off, without requiring the load of a new memory address. However, a write sequence always requires an address to be supplied.

Addressing FRAM Array in the FM3164/FM31256 Family

The FM3164/FM31256 family includes 64-Kbit and 256-Kbit memory densities. The following 2-byte address field is shown for each density.

Part Number	1st Address Byte								2nd Address Byte							
FM3164	X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
FM31256	X	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Maximum junction temperature ..... 95 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +7.0 V

Input voltage ..... –1.0 V to +7.0 V and $V_{IN} < V_{DD} + 1.0$ V

Backup supply voltage .....–1.0 V to +4.5 V

DC voltage applied to outputs in High-Z state ..... –0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ..... –2.0 V to V_{DD} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration) ..... 15 mA

Electrostatic Discharge Voltage

Human Body Model (JEDEC Std JESD22-A114-E) ..... 2 kV

Charged Device Model (JEDEC Std JESD22-C101-C) ..... 1.25 kV

Machine Model (JEDEC Std JESD22-A115-A) ..... 100 V

Latch-up current ..... > ±100 mA

Note PFI input voltage must not exceed 4.5 V. The "$V_{IN} < V_{DD}+1.0$ V" restriction does not apply to the SCL and SDA inputs which do not employ a diode to V_{DD}.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.7 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{DD}[2]	Power supply			2.7	–	5.5	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.3 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.3 V.	f_{SCL} = 100 kHz	–	–	500	µA
			f_{SCL} = 400 kHz	–	–	900	µA
			f_{SCL} = 1 MHz	–	–	1500	µA
I_{SB}	V_{DD} standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.	V_{DD} < 5.5 V	–	–	150	µA
			V_{DD} < 3.6 V	–	–	120	µA
V_{BAK}[3]	RTC backup voltage		T_A = +25 °C to +85 °C	1.55	–	3.75	V
			T_A = –40 °C to +25 °C	1.90	–	3.75	V
I_{BAK}	RTC backup current	V_{DD} < 2.4 V, oscillator running, CNT1, CNT 2 at V_{BAK}.	T_A = +25 °C, V_{BAK} = 3.0 V	–	–	1.4	µA
			T_A = +85 °C, V_{BAK} = 3.0 V	–	–	2.1	µA
			T_A = +25 °C, V_{BAK} = 2.0 V	–	–	1.15	µA
			T_A = +85 °C, V_{BAK} = 2.0 V	–	–	1.75	µA
I_{BAKTC}[4]	Trickle charge current			5	–	25	µA

Notes
1. Typical values are at 25 °C, V_{DD} = V_{DD}(typ). Not 100% tested.
2. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
3. The V_{BAK} trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
4. V_{BAK} will source current when trickle charge is enabled (VBC bit = '1'), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$ max.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{TP0}	V_{DD} trip point voltage, VTP(1:0) = 00b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$		2.50	2.6	2.70	V
V_{TP1}	V_{DD} trip point voltage, VTP(1:0) = 01b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$		2.80	2.90	3.00	V
V_{TP2}	V_{DD} trip point voltage, VTP(1:0) = 10b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$		3.75	3.90	4.00	V
V_{TP3}	V_{DD} trip point voltage, VTP(1:0) = 11b	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$		4.20	4.40	4.50	V
V_{RST}[5]	V_{DD} for valid $\overline{RST}$	I_{OL} = 80 µA at V_{OL}	$V_{BAK} > V_{BAK}$ min	0	–	–	V
			$V_{BAK} < V_{BAK}$ min	1.6	–	–	V
I_{LI}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$. Does not apply to A0, A1, PFI, $\overline{RST}$, X1, or X2		–	–	±1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$. Does not apply to $\overline{RST}$, X1, or X2		–	–	±1	µA
V_{IL}[6]	Input LOW voltage		All inputs except as listed below	– 0.3	–	0.3 × V_{DD}	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	– 0.3	–	0.5	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	– 0.3	–	0.8	V
V_{IH}	Input HIGH voltage		All inputs except as listed below	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	V_{BAK} – 0.5	–	V_{BAK} + 0.3	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			PFI (comparator input)	–	–	3.75	V
V_{OH}	Output HIGH voltage	I_{OH} = –2 mA		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		–	–	0.4	V
R_{RST}	Pull-up resistance for $\overline{RST}$ inactive			50	–	400	kΩ
R_{in}	Input resistance (A1–A0)	For $V_{IN} = V_{IL}$(Max)		20	–	–	kΩ
		For $V_{IN} = V_{IH}$(Min)		1	–	–	MΩ
V_{PFI}	Power fail input reference voltage			1.140	1.20	1.225	V
V_{HYS}	Power fail input (PFI) hysteresis (rising)			–	–	100	mV

Notes
5. The minimum V_{DD} to guarantee the level of $\overline{RST}$ remains a valid V_{OL} level.
6. Includes $\overline{RST}$ input detection of external reset condition to trigger driving of $\overline{RST}$ signal by FM3164/FM31256.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

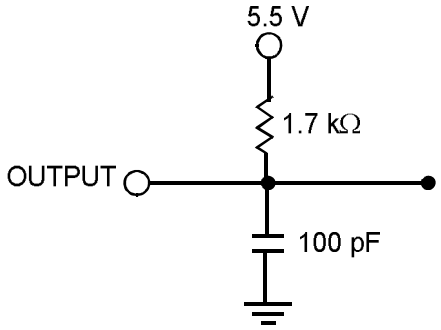
Parameter [7]	Description	Test Conditions	Typ	Max	Unit
C_{IO}	Input/Output pin capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	–	8	pF
C_{XTL} [8]	X1, X2 crystal pin capacitance		12	–	pF

Thermal Resistance

Parameter	Description	Test Conditions	14-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	80	°C/W
Θ_{JC}	Thermal resistance (junction to case)		29	°C/W

AC Test Loads and Waveforms

Figure 23. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels ..... 10% and 90% of V_{DD}

Input rise and fall times ..... 10 ns

Input and output timing reference levels ..... 0.5 × V_{DD}

Output load capacitance ..... 100 pF

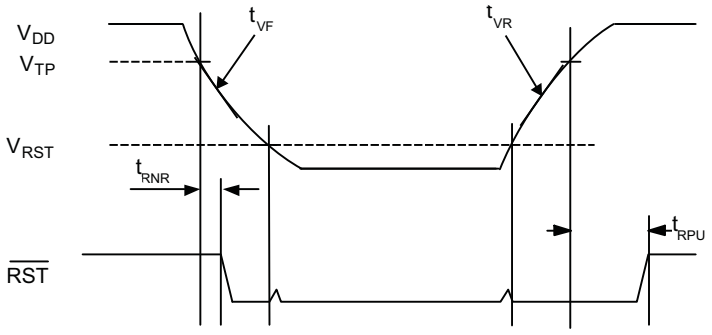
Notes
7. This parameter is characterized and not 100% tested.
8. The crystal attached to the X1/X2 pins must be rated as 6 pF.

Supervisor Timing

Over the Operating Range

Parameter	Description	Min	Max	Units
t_{RPU}	$\overline{RST}$ active (LOW) after $V_{DD} > V_{TP}$	100	200	ms
t_{RNR}[9]	$\overline{RST}$ response time to $V_{DD} < V_{TP}$ (noise filter)	10	25	µs
t_{VR}[9, 10]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF}[9, 10]	V_{DD} power-down ramp rate	100	–	µs/V
t_{WDP}[11]	Pulse width of $\overline{RST}$ for watchdog reset	100	200	ms
t_{WDOG}[11]	Timeout of watchdog	t_{DOG}	2 × t_{DOG}	ms
f_{CNT}	Frequency of event counters	0	10	MHz
t_{OSC}	RTC Oscillator time to start	–	2	s

Figure 24. $\overline{RST}$ Timing



Notes
9. This parameter is characterized and not 100% tested.
10. Slope measured at any point on V_{DD} waveform.
11. t_{DOG} is the programmed time in register in register 0Ah, $V_{DD} > V_{TP}$, and t_{RPU} satisfied.

AC Switching Characteristics

Over the Operating Range

Parameter [12]	Alt. Parameter	Description	Min	Max	Min	Max	Min	Max	Unit
f_{SCL}		SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{SU;STA}$		Start condition setup for repeated Start	4.7	–	0.6	–	0.25	–	µs
$t_{HD;STA}$		Start condition hold time	4.0	–	0.6	–	0.25	–	µs
t_{LOW}		Clock LOW period	4.7	–	1.3	–	0.6	–	µs
t_{HIGH}		Clock HIGH period	4.0	–	0.6	–	0.4	–	µs
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	250	–	100	–	100	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	–	0	–	ns
t_{DH}		Data output hold (from SCL @ V_{IL})	0	–	0	–	0	–	ns
t_R[13]	t_r	Input rise time	–	1000	–	300	–	300	ns
t_F[13]	t_f	Input fall time	–	300	–	300	–	100	ns
$t_{SU;STO}$		STOP condition setup	4	–	0.6		0.25	–	µs
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	3		0.9	–	0.55	µs
t_{BUF}		Bus free before new transmission	4.7	–	1.3	–	0.5	–	µs
t_{SP}		Noise suppression time constant on SCL, SDA	–	50		50	–	50	ns

Figure 25. Read Bus Timing Diagram

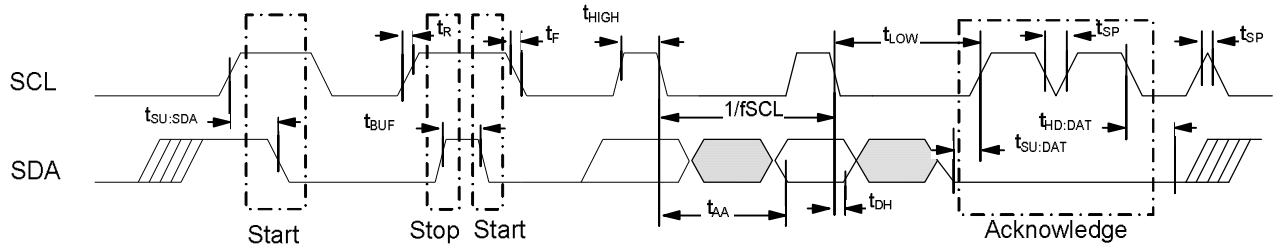
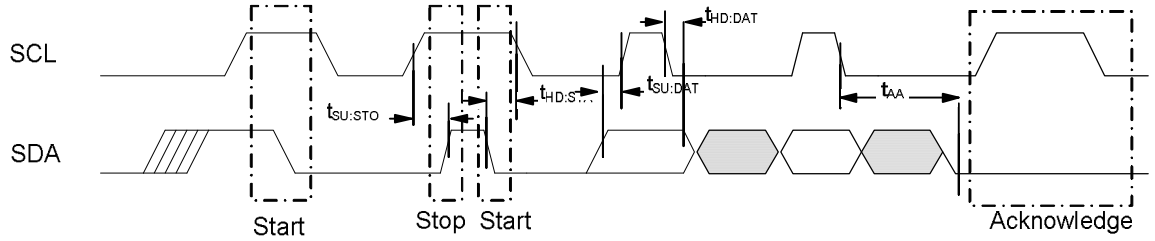


Figure 26. Write Bus Timing Diagram



Notes

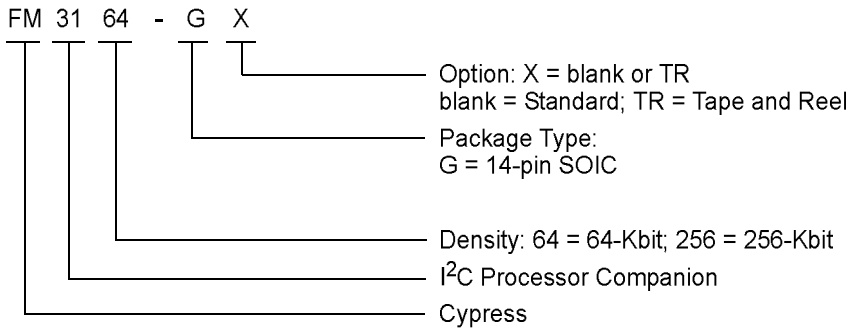
12. Test conditions assume a signal transition time of 10 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 100 pF load capacitance shown in page 28.
13. This parameter is characterized and not 100% tested.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM3164/FM31256-G	51-85067	14-pin SOIC	Industrial
FM3164/FM31256-GTR	51-85067	14-pin SOIC	

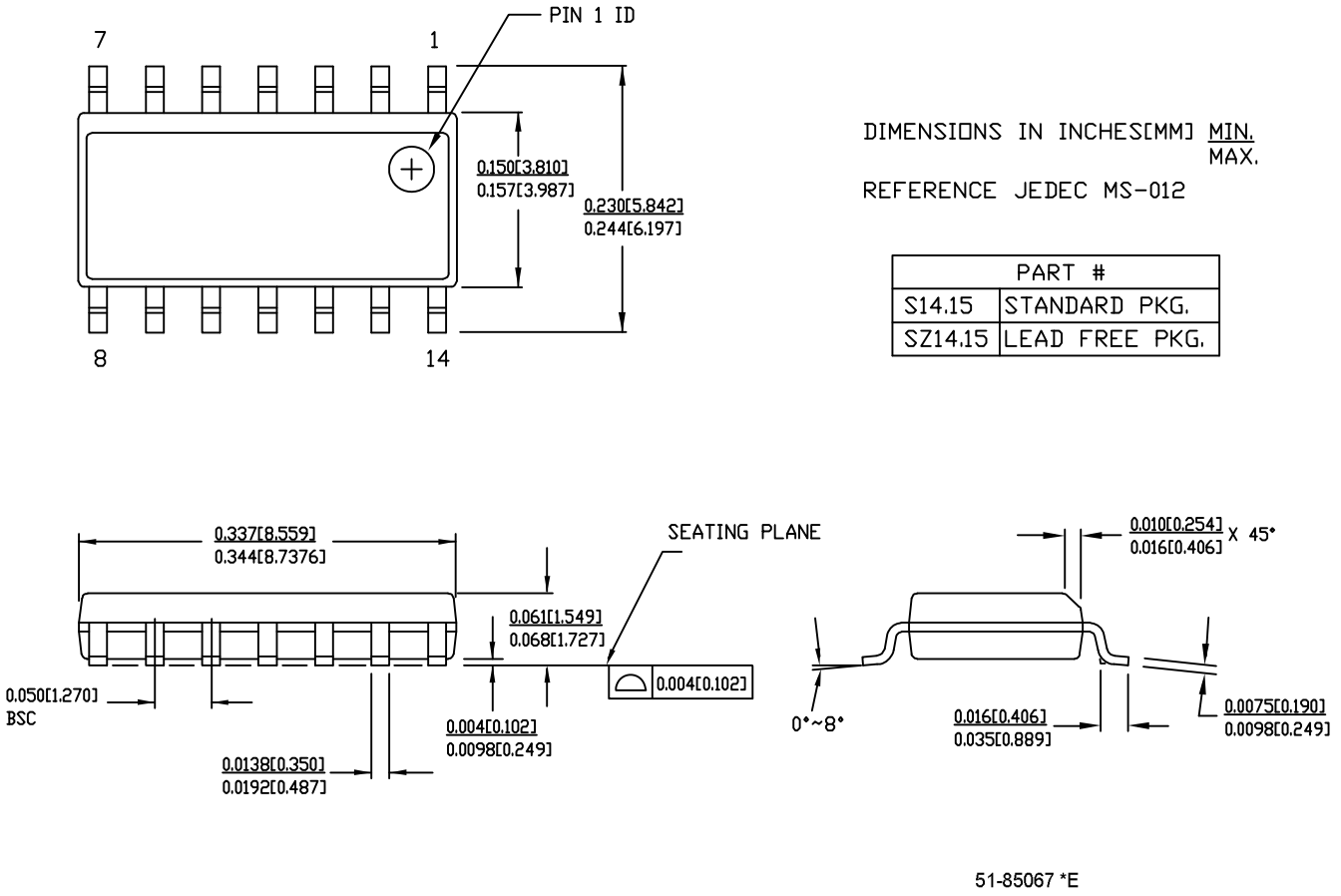
All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 27. 14-pin SOIC (150 Mils) Package Outline, 51-85067



Acronyms

Acronym	Description
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
NMI	Non Maskable interrupt
RoHS	Restriction of Hazardous Substances
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM3164/FM31256, 64-Kbit/256-Kbit Integrated Processor Companion with F-RAM Document Number: 001-86391				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3916896	GVCH	02/28/2013	New spec.
*A	3924836	GVCH	03/07/2013	Changed status to Production. Removed FM3116 and FM3104 part details in all instances across the document. Removed 4Kb and 8Kb versions details in all instances across the document. Modified formatting
*B	3985209	GVCH	05/02/2013	Updated DC Electrical Characteristics: Changed minimum value of V_{TP0} parameter from 2.55 V to 2.50 V. Changed minimum value of V_{TP1} parameter from 2.85V to 2.80 V. Changed minimum value of V_{TP2} parameter from 3.80 V to 3.75 V. Changed minimum value of V_{TP3} parameter from 4.25 V to 4.20 V. Changed minimum value of V_{PFI} parameter from 1.175 V to 1.140 V.
*C	4333096	GVCH	05/059/2014	Updated Maximum Ratings: Removed “Package Moisture Sensitivity Level” and its corresponding details. Added “Maximum junction temperature” and its corresponding details. Added “DC voltage applied to outputs in High-Z state” and its corresponding details. Added “Transient voltage (< 20 ns) on any pin to ground potential” and its corresponding details. Added “Package power dissipation capability (T_A = 25 °C)” and its corresponding details. Added “DC output current (1 output at a time, 1s duration)” and its corresponding details. Added “Latch-up current” and its corresponding details. Updated Data Retention and Endurance: Updated details corresponding to T_{DR} parameter. Added NV_C parameter and its details. Added Thermal Resistance. Updated Package Diagram: Removed “SOIC Package Marking Scheme”. Updated to Cypress template.
*D	4562106	GVCH	11/05/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*E	6062038	NILE / GVCH	02/07/2018	Updated Register Map: Updated Table 6: Updated details in “Description” column corresponding to $\overline{\text{OSCEN}}$ bit (Added reference to t_{OSC}). Updated Supervisor Timing: Added t_{OSC} parameter and its details. Updated Package Diagram: spec 51-85067 – Changed revision from *D to *E. Updated to new template.

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FM31256-G1

256-Kbit Integrated Processor Companion with F-RAM

Features

- 256-Kbit ferroelectric random access memory (F-RAM)
  - Logically organized as 32 K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- High Integration Device Replaces Multiple Parts
  - Serial nonvolatile memory
  - Real time clock (RTC)
  - Low voltage reset
  - Watchdog timer
  - Early power-fail warning/NMI
  - Two 16-bit event counter
  - Serial number with write-lock for security
- Real-time Clock/Calendar
  - Backup current at 2V: 1.15 µA at +25 °C
  - Seconds through centuries in BCD format
  - Tracks leap years through 2099
  - Uses standard 32.768 kHz crystal (12.5 pF)
  - Software calibration
  - Supports battery or capacitor backup
- Processor Companion
  - Active-low reset output for V_{DD} and watchdog
  - Programmable low-V_{DD} reset trip point
  - Manual reset filtered and debounced
  - Programmable watchdog timer
  - Dual Battery-backed event counter tracks system intrusions or other events
  - Comparator for power-fail interrupt
  - 64-bit programmable serial number with lock
- Fast 2-wire serial interface (I^2C)
  - Up to 1-MHz frequency
  - Supports legacy timings for 100 kHz and 400 kHz
  - RTC, Supervisor controlled via I^2C interface
  - Device select pins for up to 4 memory devices
- Low power consumption
  - 1.5 mA active current at 1 MHz
  - 150 µA standby current
- Operating voltage: V_{DD} = 4.0 V to 5.5 V
- Industrial temperature: –40 °C to +85 °C
- 14-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant
- Underwriters laboratory (UL) recognized

Functional Overview

The FM31256-G1 device integrates F-RAM memory with the most commonly needed functions for processor-based systems. Major features include nonvolatile memory, real time clock, low-V_{DD} reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or any other purpose.

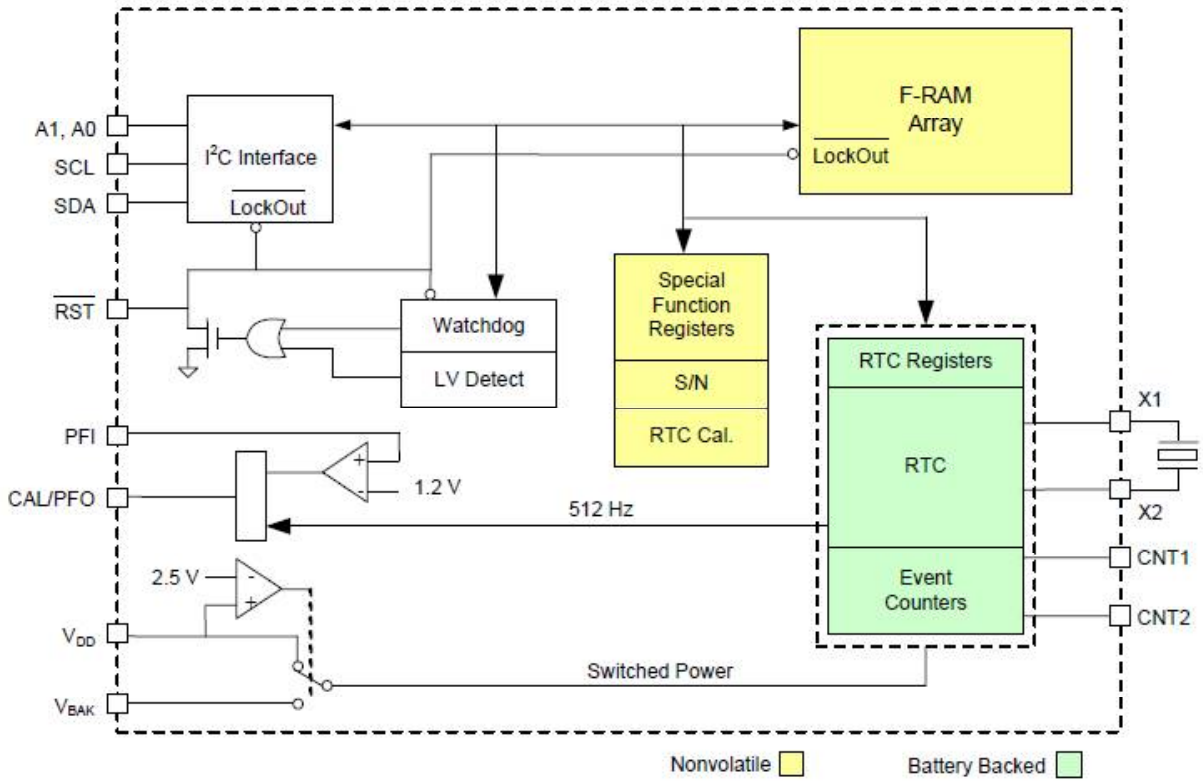
The FM31256-G1 is a 256-Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. This memory is truly nonvolatile rather than battery backed. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by other nonvolatile memories. The FM31256-G1 is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

The real time clock (RTC) provides time and date information in BCD format. It can be permanently powered from an external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low V_{DD} condition or a watchdog timeout. $\overline{RST}$ goes active when V_{DD} drops below a programmable threshold and remains active for 100 ms after V_{DD} rises above the trip point. A programmable watchdog timer runs from 100 ms to 3 seconds. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host before the timeout. A flag-bit indicates the source of the reset.

A comparator on PFI compares an external input pin to the onboard 1.2 V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers a dual battery-backed event counter that tracks the number of rising or falling edges detected on a dedicated input pin.

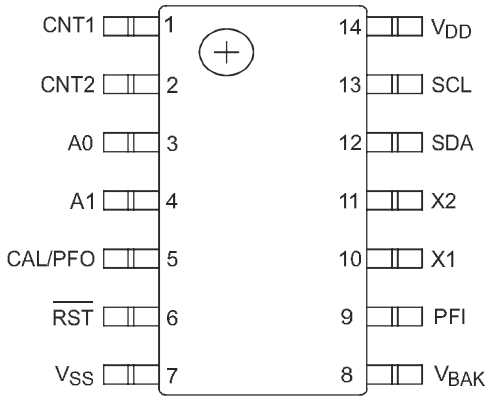
Logic Block Diagram



Contents

Pinout

Figure 1. 14-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A1-A0	Input	**Device Select Address 1-0**. These pins are used to select one of up to 4 devices of the same type on the same I^2C bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data/Address**. This is a bi-directional pin for the I^2C interface. It is open-drain and is intended to be wire-OR'd with other devices on the I^2C bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the I^2C interface. Data is clocked out of the device on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
CNT1, CNT2	Input	**Event Counter Inputs**. These battery-backed inputs increment counters when an edge is detected on the corresponding CNT pin. The polarity is programmable. These pins should not be left floating. Tie to ground if these pins are not used.
X1, X2	Input/Output	32.768 kHz crystal connection. When using an external oscillator, apply the clock to X1 and a DC mid-level to X2. These pins should be left unconnected if RTC is not used.
$\overline{RST}$	Input/Output	**Reset**. This active-low output is open drain with weak pull-up. It is also an input when used as a manual reset. This pin should be left floating if unused.
PFI	Input	**Early Power-fail Input**. Typically connected to an unregulated power supply to detect an early power failure. This pin must be tied to ground if unused.
CAL/PFO	Output	**Calibration/Early Power-fail Output**. In calibration mode, this pin supplies a 512 Hz square-wave output for clock calibration. In normal operation, this is the early power-fail output.
V_{BAK}	Power supply	**Backup supply voltage**. Connected to a 3 V battery or a large value capacitor. If no backup supply is used, this pin should be tied to ground and the VBC bit should be cleared in the RTC register 0Bh. The trickle charger is UL recognized and ensures no excessive current when using a lithium battery.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Overview

The FM31256-G1 device combines a serial nonvolatile RAM with a real time clock (RTC) and a processor companion. The companion is a highly integrated peripheral including a processor supervisor, a comparator used for early power-fail warning, nonvolatile event counters, and a 64-bit serial number. The FM31256-G1 integrates these complementary but distinct functions under a common interface in a single package. The product is organized as two logical devices. The first is a memory and the second is the companion which includes all the remaining functions. From the system perspective they appear to be two separate devices with unique IDs on the serial bus.

The memory is organized as a standalone nonvolatile I^2C memory using standard device ID value. The real time clock and supervisor functions are accessed with a separate I^2C device ID. This allows clock/calendar data to be read while maintaining the most recently used memory address. The clock and supervisor functions are controlled by 25 special function registers. The RTC and event counter circuits are maintained by the power source on the V_{BAK} pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Architecture

The FM31256-G1 device is available in memory size 256-Kbit. The device uses two-byte addressing for the memory portion of the chip. This makes the device software compatible with its standalone memory counterparts, but makes them compatible within the entire family.

The memory array is logically organized as 32,768 × 8 bits and is accessed using an industry-standard I^2C interface. The memory is based on F-RAM technology. Therefore it can be treated as RAM and is read or written at the speed of the I^2C bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The I^2C protocol is described on page 19.

The memory array can be write-protected by software. Two bits in the processor companion area (WP1, WP0 in register 0Bh) control the protection setting. Based on the setting, the protected addresses cannot be written and the I^2C interface will not acknowledge any data to protected addresses. The special function registers containing these bits are described in detail below.

Table 1. Block Memory Write Protection

WP1	WP0	Protected Address Range
0	0	None
0	1	Bottom 1/4
1	0	Bottom 1/2
1	1	Full array

Processor Companion

In addition to nonvolatile RAM, the FM31256-G1 incorporates a real time clock and highly integrated processor companion. The companion includes a low-V_{DD} reset, a programmable watchdog timer, a battery-backed event counters, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

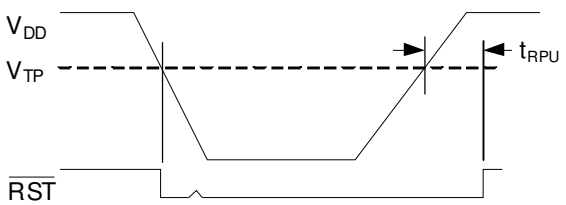
Supervisors provide a host processor two basic functions: detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. The FM31256-G1 has a reset pin ($\overline{RST}$) to drive a processor reset input during power faults, power-up, and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the $\overline{RST}$ pin. When V_{DD} is above the programmed trip point, $\overline{RST}$ output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}), the $\overline{RST}$ pin will be driven LOW. It will remain LOW until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, $\overline{RST}$ continues to drive LOW for at least 100 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the $\overline{RST}$ pin will return to the weak HIGH state. While $\overline{RST}$ is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

Table 1 below shows how bit VTP controls the trip point of the low-V_{DD} reset. They are located in register 0Bh, bits 1 and 0. The reset pin will drive LOW when V_{DD} is below the selected V_{TP} voltage, and the I^2C interface and F-RAM array will be locked out. Note that the bit 1 location is a don't care. Figure 2 illustrates the reset operation in response to a low V_{DD}.

Table 2. VTP setting

VTP Setting	VTP
3.9 V	0
4.4 V	1

Figure 2. Low V_{DD} Reset



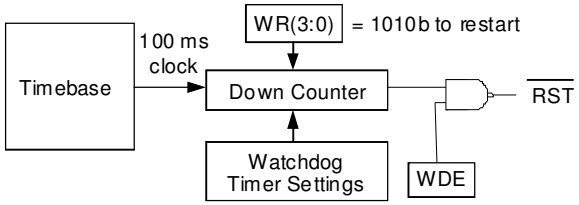
A watchdog timer can also be used to drive an active reset signal. The watchdog is a free-running programmable timer. The timeout period can be software programmed from 100 ms to 3 seconds in 100 ms increments via a 5-bit nonvolatile register. All programmed settings are minimum values and vary with temperature according to the operating specifications. The watchdog has two additional controls associated with its operation, a watchdog enable bit (WDE) and timer restart bits (WR). Both the enable bit must be set and the watchdog must

timeout in order to drive $\overline{RST}$ active. If a reset event occurs, the timer will automatically restart on the rising edge of the reset pulse. If WDE = '0', the watchdog timer runs but a watchdog fault will not cause $\overline{RST}$ to be asserted LOW. The WTR flag will be set, indicating a watchdog fault. This setting is useful during software development if the developer does not want $\overline{RST}$ to drive. Note that setting the maximum timeout setting (11111b) disables the counter to save power. The second control is a nibble that restarts the timer preventing a reset. The timer should be restarted after changing the timeout value.

The watchdog timeout value is located in register 0Ah, bits 4:0, and the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 09h. Writing this pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout period will be set immediately after enabling. The watchdog is disabled when V_{DD} is below V_{TP}. The following table summarizes the watchdog bits. A block diagram follows.

Watchdog Timeout	WDT(4:0)	0Ah, bits 4:0
Watchdog Enable	WDE	0Ah, bit 7
Watchdog Restart	WR(3:0)	09h, bits 3:0

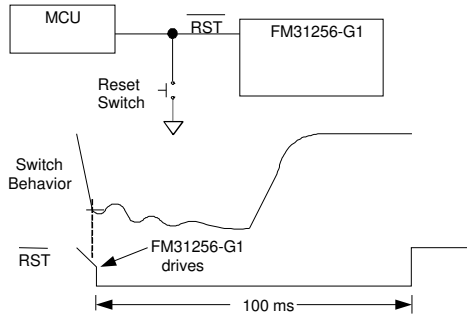
Figure 3. Watchdog Timer



Manual Reset

The $\overline{RST}$ is a bi-directional signal allowing the FM31256-G1 to filter and de-bounce a manual reset switch. The $\overline{RST}$ input detects an external low condition and responds by driving the $\overline{RST}$ signal LOW for 100 ms.

Figure 4. Manual Reset



Note The internal weak pull-up eliminates the need for additional external components.

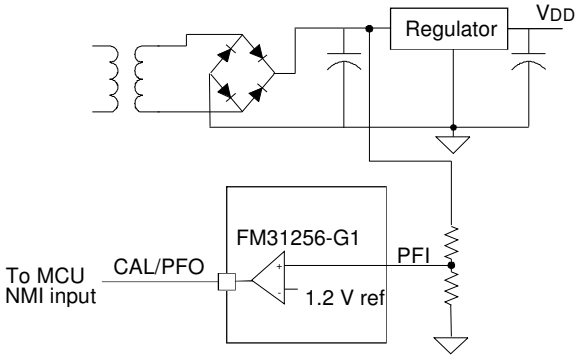
Reset Flags

In case of a reset condition, a flag bit will be set to indicate the source of the reset. A low-V_{DD} reset is indicated by the POR flag, register 09h bit 6. A watchdog reset is indicated by the WTR flag, register 09h bit 7. Note that the flags are internally set in response to reset sources, but they must be cleared by the user. When the register is read, it is possible that both flags are set if both have occurred since the user last cleared them.

Early Power Fail Comparator

An early power fail warning can be provided to the processor well before V_{DD} drops out of spec. The comparator is used to create a power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to the unregulated power supply via a resistor divider. An application circuit is shown below.

Figure 5. Comparator as a Power-Fail Warning



The voltage on the PFI input pin is compared to an onboard 1.2 V reference. When the PFI input voltage drops below this threshold, the comparator will drive the CAL/PFO pin to a LOW state. The comparator has 100 mV (max) of hysteresis to reduce noise sensitivity, only for a rising PFI signal. For a falling PFI edge, there is no hysteresis.

The comparator is a general purpose device and its application is not limited to the NMI function.

The comparator is not integrated into the special function registers except as it shares its output pin with the CAL output. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the CAL/PFO output pin will be driven with a 512 Hz square wave and the comparator will be ignored. Since most users only invoke the calibration mode during production, this should have no impact on system operations using the comparator.

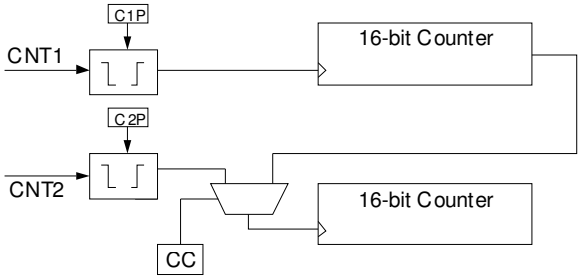
Note The maximum voltage on the comparator input PFI is limited to 3.75 V under normal operating conditions.

Event Counter

The FM31256-G1 offers the user two battery-backed event counters. Input pins CNT1 and CNT2 are programmable edge detectors. Each clocks a 16-bit counter. When an edge occurs, the counters will increment their respective registers. Counter 1

is located in registers 0Dh and 0Eh, Counter 2 is located in registers 0Fh and 10h. These register values can be read anytime V_{DD} is above V_{TP}, and they will be incremented as long as a valid V_{BAK} power source is provided. To read, set the RC bit, register 0Ch bit 3 to 1. This takes a snapshot of all four counter bytes allowing a stable value even if a count occurs during the read. The registers can be written by software allowing the counters to be cleared or initialized by the system. Counts are blocked during a write operation. The two counters can be cascaded to create a single 32-bit counter by setting the CC control bit (register 0Ch, bit 2). When cascaded, the CNT1 input will cause the counter to increment. CNT2 is not used in this mode and should be tied to ground.

Figure 6. Event Counter



The control bits for event counting are located in register 0Ch. Counter 1 Polarity is bit C1P, bit 0; Counter 2 Polarity is C2P, bit 1; the Cascade Control is CC, bit 2; and the Read Counter bit is RC, bit 3.

The polarity bits must be set prior to setting the counter value(s). If a polarity bit is changed, the counter may inadvertently increment. If the counter pins are not being used, tie them to ground.

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via the device ID for the Processor Companion. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. However, once the lock bit is set, the values cannot be altered and the lock cannot be removed. Once locked the serial number registers can still be read by the system.

The serial number is located in registers 11h to 18h. The lock bit is SNL (register 0Bh, bit 7). Setting the SNL bit to a ‘1’ disables writes to the serial number registers, and the SNL bit cannot be cleared.

Real-time Clock Operation

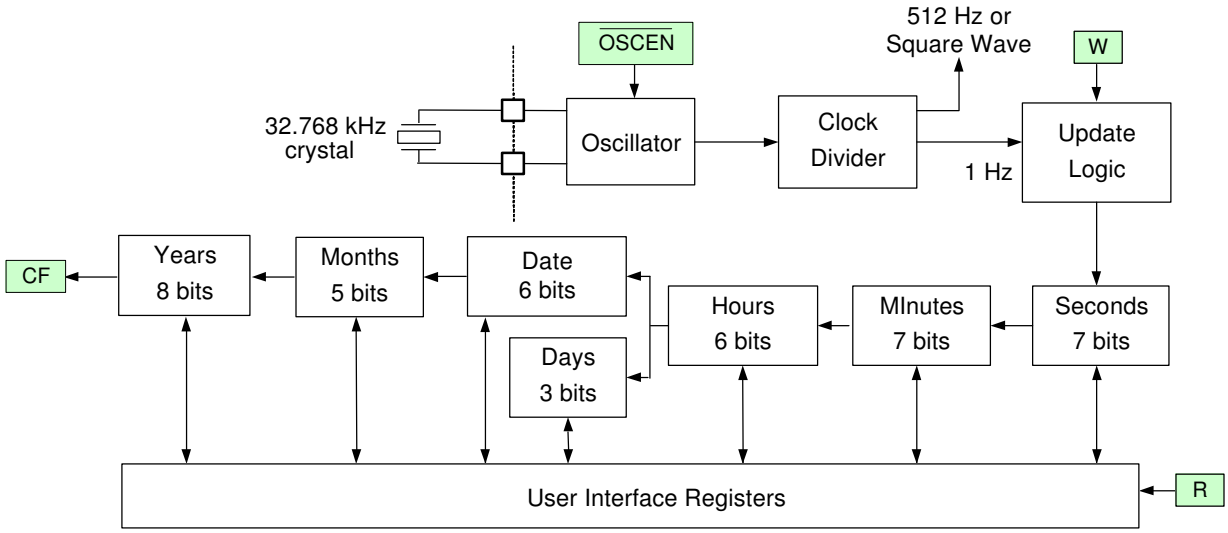
The real-time clock (RTC) is a timekeeping device that can be battery or capacitor backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1 Hz). Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram (Figure 7) illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h described below. Changing the R bit from ‘0’ to ‘1’ transfers timekeeping information from the core into holding registers that can be read by the user. If a timekeeper update is pending when R is set, then the core will be updated prior to loading the user registers. The registers are frozen and will not be updated again until the R bit is cleared to ‘0’. R is used for reading the time.

Setting the W bit to ‘1’ locks the user registers. Clearing it to ‘0’ causes the values in the user registers to be loaded into the timekeeper core. W bit is used for writing new time values. Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

Figure 7. Real-time Clock Core Block Diagram

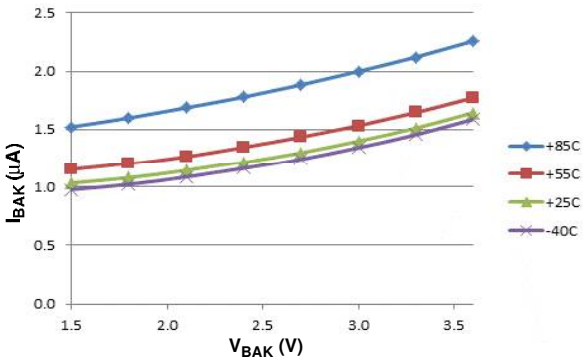


Backup Power

The real-time clock/calendar is intended to be permanently powered. When the primary system power fails, the voltage on the V_{DD} pin will drop. When V_{DD} is less than 2.5 V, the RTC (and event counters) will switch to the backup power supply on V_{BAK}. The clock operates at extremely low current in order to maximize battery or capacitor life. However, an advantage of combining a clock function with F-RAM memory is that data is not lost regardless of the backup power source.

The I_{BAK} current varies with temperature and voltage (see DC Electrical Characteristics table). The following graph shows I_{BAK} as a function of V_{BAK}. These curves are useful for calculating backup time when a capacitor is used as the V_{BAK} source.

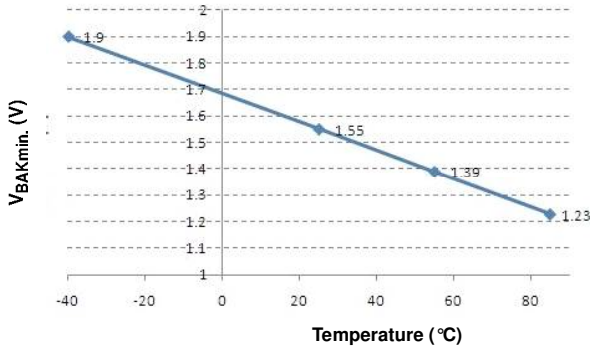
Figure 8. I_{BAK} vs. V_{BAK} Voltage



The minimum V_{BAK} voltage varies linearly with temperature. The user can expect the minimum V_{BAK} voltage to be 1.23 V at +85 °C and 1.90 V at -40 °C. The tested limit is 1.55 V at +25 °C.

Note The minimum V_{BAK} voltage has been characterized at -40 °C and +85 °C but is not 100% tested.

Figure 9. V_{BAK}(min.) vs Temperature



Trickle Charger

To facilitate capacitor backup the V_{BAK} pin can optionally provide a trickle charge current. When the VBC bit (register 0Bh, bit 2) is set to '1', the V_{BAK} pin will source approximately 15 µA until V_{BAK} reaches 3.75 V. In 5 V systems, this charges the capacitor to V_{DD} without an external diode and resistor charger and also prevents the user from exceeding the V_{BAK} maximum voltage specification. There is a Fast Charge mode which is enabled by the FC bit (register 0Bh, bit 5). In this mode the trickle charger current is set to approximately 1 mA, allowing a large backup capacitor to charge more quickly.

In the case where no battery is used, the V_{BAK} pin should be tied to V_{SS}. V_{BAK} should not be tied to 5 V since the V_{BAK} (max) specification will be exceeded. Be sure to turn off the trickle charger (VBC = '0'), otherwise charger current will be shunted to ground from V_{DD}.

Note Systems using lithium batteries should clear the VBC bit to '0' to prevent battery charging. The V_{BAK} circuitry includes an internal 1 KΩ series resistor as a safety element. The trickle charger is UL Recognized.

Calibration

When the CAL bit in the register 00h is set to '1', the clock enters calibration mode. In calibration mode, the CAL/PFO output pin is dedicated to the calibration function and the power fail output is temporarily unavailable. Calibration operates by applying a digital correction to the counter based on the frequency error. In this mode, the CAL/PFO pin is driven with a 512 Hz (nominal) square wave. Any measured deviation from 512 Hz translates into a timekeeping error. The user converts the measured error in ppm and writes the appropriate correction value to the calibration register. The correction factors are listed in the table below. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to '1', whereas negative ppm adjustments have CALS = '0'. After calibration, the clock will have a maximum error of ±2.17 ppm or ±0.09 minutes per month at the calibrated temperature.

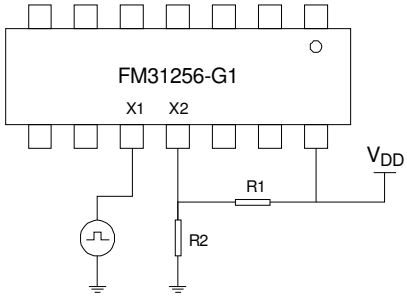
The calibration setting is stored in F-RAM so it is not lost should the backup source fail. It is accessed with bits CAL(4:0) in register 01h. This value can be written only when the CAL bit is set to a '1'. To exit the calibration mode, the user must clear the CAL bit to a '0'. When the CAL bit is '0', the CAL/PFO pin will revert to the power fail output function.

Crystal Oscillator

The crystal oscillator is designed to use a 12.5 pF crystal without the need for external components, such as loading capacitors. The FM31256-G1 device has built-in loading capacitors that are optimized for use with 12.5 pF crystals and no additional external loading capacitors are required nor suggested.

If a 32.768 kHz crystal is not used, an external oscillator may be connected to the FM31256-G1. Apply the oscillator to the X1 pin. Its high and low voltage levels can be driven rail-to-rail or amplitudes as low as approximately 500 mV p-p. To ensure proper operation, a DC bias must be applied to the X2 pin. It should be centered between the high and low levels on the X1 pin. This can be accomplished with a voltage divider.

Figure 10. External Oscillator

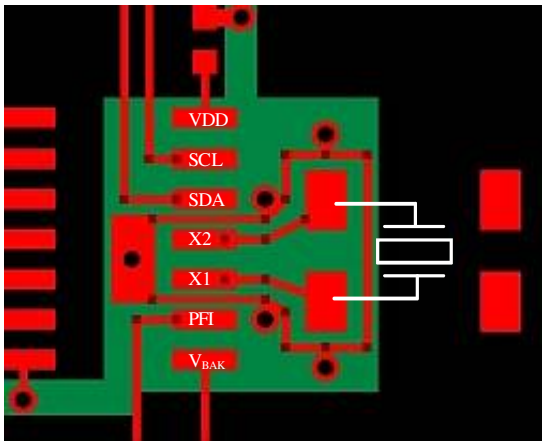


In the example, R1 and R2 are chosen such that the X2 voltage is centered around the X1 oscillator drive levels. If you wish to avoid the DC current, you may choose to drive X1 with an external clock and X2 with an inverted clock using a CMOS inverter.

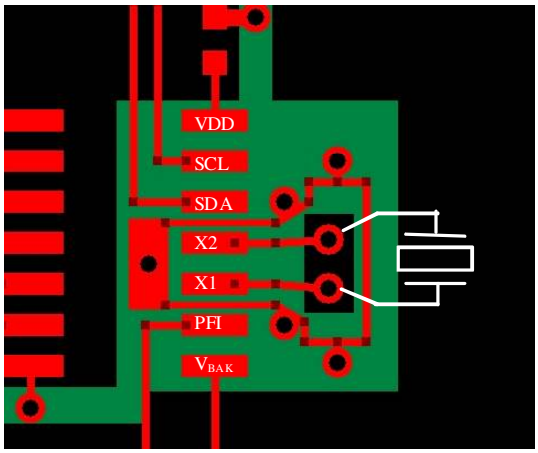
Layout Recommendations

The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring must be placed around these pads and the guard ring grounded. SDA and SCL traces should be routed away from the X1 / X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.

Figure 11. Layout Recommendations



Layout for Surface Mount Crystal
(red = top layer, green = bottom layer)



Layout for Through Hole Crystal
(red = top layer, green = bottom layer)

Table 3. Digital Calibration Adjustments

Positive Calibration for slow clocks: Calibration will achieve ±2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

Table 3. Digital Calibration Adjustments (continued)

Negative Calibration for fast clocks: Calibration will achieve ±2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001
2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

Register Map

The RTC and processor companion functions are accessed via 25 special function registers, which are mapped to a separate I^2C device ID. The interface protocol is described on page 19. The registers contain timekeeping data, control bits, and information flags. A description of each register follows the summary table.

Table 4. Register Map Summary Table

Nonvolatile = ☐ Battery-backed = ☐

Address	Data								Function	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
18h	Serial Number Byte 7								Serial Number 7	FFh
17h	Serial Number Byte 6								Serial Number 6	FFh
16h	Serial Number Byte 5								Serial Number 5	FFh
15h	Serial Number Byte 4								Serial Number 4	FFh
14h	Serial Number Byte 3								Serial Number 3	FFh
13h	Serial Number Byte 2								Serial Number 2	FFh
12h	Serial Number Byte 1								Serial Number 1	FFh
11h	Serial Number Byte 0								Serial Number 0	FFh
10h	Counter 2 MSB								Event Counter 2 MSB	FFh
0Fh	Counter 2 LSB								Event Counter 2 LSB	FFh
0Eh	Counter 1 MSB								Event Counter 1 MSB	FFh
0Dh	Counter 1 LSB								Event Counter 1 LSB	FFh
0Ch					RC	CC	C2P	C1P	Event Count Control	
0Bh	SNL	-	FC	WP1	WP0	VBC	-	VTP	Companion Control	
0Ah	WDE	-	-	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog Control	
09h	WTR	POR	LB	-	WR3	WR2	WR1	WR0	Watchdog Restart/Flags	
08h	10 years				years				Years	00-99
07h	0	0	0	10 months	months				Month	01-12
06h	0	0	10 date		date				Date	01-31
05h	0	0	0	0	0	day			Day	01-07
04h	0	0	10 hours		hours				Hours	00-23
03h	0	10 minutes			minutes				Minutes	00-59
02h	0	10 seconds			seconds				Seconds	00-59
01h	$\overline{\text{OSCEN}}$	reserved	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL Control	
00h	reserved	CF	reserved	reserved	reserved	CAL	W	R	RTC Control	

Note When the device is first powered up and programmed, all timekeeping registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers. All other register values should be treated as unknown.

Table 5. Default Register Values

Address	Hex Value
18h	0x00
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00
12h	0x00
11h	0x00
0Bh	0x00

Address	Hex Value
0Ah	0x1F
08h	0x00
07h	0x01
06h	0x01
05h	0x01
04h	0x00
03h	0x01
02h	0x00
01h	0x80

Table 6. Register Description

Address	Description							
18h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
	Upper byte of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
17h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
16h	Byte 6 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
	Serial Number Byte 5							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
	Byte 5 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
15h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
	Byte 4 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
14h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24
	Byte 3 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
13h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
	Byte 2 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
12h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
	Byte 1 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
11h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	LSB of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
10h	**Counter 2 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.15	C2.14	C2.13	C2.12	C2.11	C2.10	C2.9	C2.8
	Event Counter 2 MSB. Increments on overflows from Counter 2 LSB. Battery-backed, read/write.							

Table 6. Register Description (continued)

Address	Description							
0Fh	**Counter 2 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
	Event Counter 2 LSB. Increments on programmed edge event on CNT2 input or overflows from Counter 1 MSB when CC = '1'. Battery-backed, read/write.							
0Eh	**Counter 1 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.15	C1.14	C1.13	C1.12	C1.11	C1.10	C1.9	C1.8
	Event Counter 1MSB. Increments on overflows from Counter 1 LSB. Battery-backed, read/write.							
0Dh	**Counter 1 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Event Counter 1 LSB. Increments on programmed edge event on CNT1 input. Battery-backed, read/write.							
0Ch	**Event Counter Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	-	-	-	-	RC	CC	C2P	C1P
RC	Read Counter. Setting this bit to '1' takes a snapshot of the four counters bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.							
CC	Counter Cascade. When CC = '0', the event counters operate independently according to the edge programmed by C1P and C2P respectively. When CC = '1', the counters are cascaded to create one 32-bit counter. The registers of Counter 2 represent the most significant 16-bits of the counter and CNT1 is the controlling input. Bit C2P is don't care when CC = '1'. Battery-backed, read/write.							
C2P	CNT2 detects falling edges when C2P = '0', rising edges when C2P = '1'. C2P is "don't care" when CC = '1'. The value of Event Counter 2 may inadvertently increment if C2P is changed. Battery-backed, read/write.							
C1P	CNT1 detects falling edges when C1P = '0', rising edges when C1P = '1'. The value of Event Counter 1 may inadvertently increment if C1P is changed. Battery-backed, read/write.							
0Bh	**Companion Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SNL	-	FC	WP1	WP0	VBC	-	VTP
SNL	Serial Number Lock: Setting to a '1' makes registers 11h to 18h and SNL permanently read-only. SNL cannot be cleared once set to '1'. Nonvolatile, read/write.							
FC	Fast Charge: Setting FC to '1' (and VBC = '1') causes a ~1 mA trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.							
WP(1:0)	Write Protect. These bits control the write protection of the memory array. Nonvolatile, read/write. Write protect address — WP1 — WP0 None — 0 — 0 Bottom 1/4 — 0 — 1 Bottom 1/2 — 1 — 0 Full array — 1 — 1							
VBC	V_{BAK} Charger Control. Setting VBC to '1' (and FC = '0') causes a 80 µA (1 mA if FC = '1') trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.							

Table 6. Register Description (continued)

Address	Description
VTP	VTP Select. This bit control the reset trip point for the low V_{DD} reset function. Nonvolatile, read/write. Trip Voltage — VTP 3.9 V — 0 4.4 V — 1
0Ah	**Watchdog Control**
	D7 | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** WDE | - | - | WDT4 | WDT3 | WDT2 | WDT1 | WDT0
WDE	Watchdog Enable. When WDE = '1', a watchdog timer fault will cause the $\overline{RST}$ signal to go active. When WDE = '0' the timer runs but has no effect on $\overline{RST}$, however the WTR flag will be set when a fault occurs. Note as the timer is free-running, users should restart the timer using WR(3:0) prior to setting WDE = '1'. This assures a full watchdog timeout interval occurs. Nonvolatile, read/write.
WDT(4:0)	Watchdog Timeout. Indicates the minimum watchdog timeout interval with 100 ms resolution. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). Nonvolatile, read/write. Watchdog Timeout — WDT4 — WDT3 — WDT2 — WDT1 — WDT0 Invalid - default 100 ms — 0 — 0 — 0 — 0 — 0 100 ms — 0 — 0 — 0 — 0 — 1 200 ms — 0 — 0 — 0 — 1 — 0 300 ms — 0 — 0 — 0 — 1 — 1 . . 2000 ms — 1 — 0 — 1 — 0 — 0 2100 ms — 1 — 0 — 1 — 0 — 1 2200 ms — 1 — 0 — 1 — 1 — 0 . . 2900 ms — 1 — 1 — 1 — 0 — 1 3000 ms — 1 — 1 — 1 — 1 — 0 Disable Counter — 1 — 1 — 1 — 1 — 1
09h	**Watchdog Restart and Flags**
	D7 | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** WTR | POR | LB | - | WR3 | WR2 | WR1 | WR0
WTR	Watchdog Timer Reset Flag: When a watchdog timer fault occurs, the WTR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
POR	Power-on Reset Flag: When the $\overline{RST}$ pin is activated by $V_{DD} < V_{TP}$, the POR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
LB	Low Backup Flag: On power up, if the V_{BAK} source is below the minimum voltage to operate the RTC and event counters, this bit will be set to '1'. The user should clear it to '0' when initializing the system. Battery-backed. Read/Write (internally set, user can clear bit).

Table 6. Register Description (continued)

Address	Description							
WR(3:0)	Watchdog Restart: Writing a pattern 1010b to WR(3:0) restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR(3:0) has no effect on the timer. This allows users to clear the WTR, POR, and LB flags without affecting the watchdog timer. Battery-backed, Write-only.							
08h	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99. Battery-backed, read/write.							
07h	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12. Battery-backed, read/write.							
06h	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Battery-backed, read/write.							
05h	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.							
04h	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours.2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23. Battery-backed, read/write.							
03h	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							

Table 6. Register Description (continued)

Address	Description							
02h	**Timekeeping - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							
01h	**CAL/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{\text{OSCEN}}$	Reserved	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0
$\overline{\text{OSCEN}}$	Oscillator Enable. When set to ‘1’, the oscillator is halted. When set to ‘0’, the oscillator runs after t_{OSC} time. Disabling the oscillator can save battery power during storage. On a power-up without battery, this bit is set to ‘1’. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to ‘0’.							
CALS	Calibration Sign: Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit can be written only when CAL = ‘1’. Nonvolatile, read/write.							
CAL(4:0)	Calibration Setting: These five bits control the calibration of the clock. These bits can be written only when CAL = ‘1’. Nonvolatile, read/write.							
00h	**RTC Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	Reserved	CF	Reserved	Reserved	Reserved	CAL	W	R
CF	Century Overflow Flag. This bit is set to a ‘1’ when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to ‘0’ when the Flag register is read. It is read-only for the user. Battery-backed.							
CAL	Calibration Setting. When set to ‘1’, the clock enters calibration mode. When CAL is set to ‘0’, the clock operates normally, and the CAL/PFO pin is controlled by the power fail comparator. Battery-backed, read/write.							
W	Write Time. Setting the W bit to ‘1’ freezes the clock. The user can then write the timekeeping registers with updated values. Resetting the W bit to ‘0’ causes the contents of the time registers to be transferred to the timekeeping counters and restarts the clock. Battery-backed, read/write.							
R	Read Time. Setting the R bit to ‘1’ copies a static image of the timekeeping core and place it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from ‘0’ to ‘1’ causes the timekeeping capture, so the bit must be returned to ‘0’ prior to reading again. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to ‘0’.							

I²C Interface

The FM31256-G1 employs an industry standard I²C bus that is familiar to many users. This product is unique since it incorporates two logical devices in one chip. Each logical device can be accessed individually. Although monolithic, it appears to the system software to be two separate products. One is a memory device. It has a Slave Address (Slave ID = 1010b) that operates the same as a stand-alone memory device. The second device is a real-time clock and processor companion which have a unique Slave Address (Slave ID = 1101b).

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM31256-G1 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 12 and Figure 13 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM31256-G1 should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM31256-G1 for a new operation.

If during operation the power supply drops below the specified V_{TP} minimum, any I²C transaction in progress will be aborted and the system should issue a START condition prior to performing another operation.

Figure 12. START and STOP Conditions

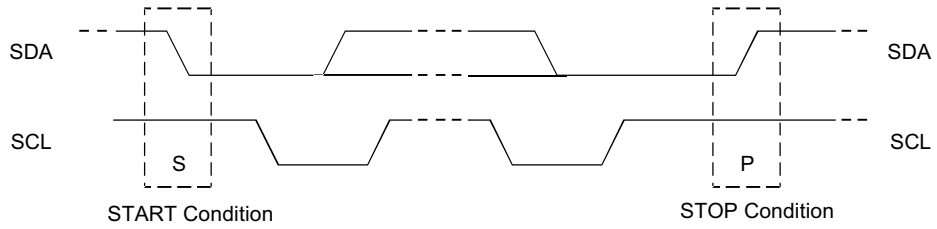
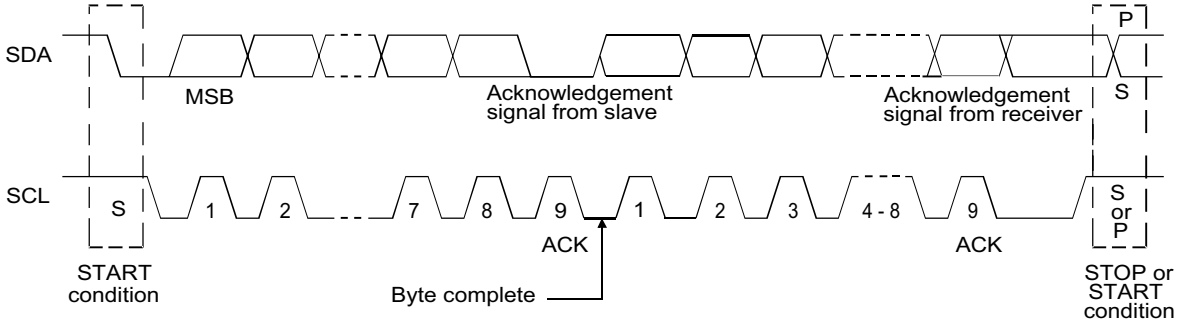


Figure 13. Data Transfer on the I²C Bus



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

Acknowledge / No-acknowledge

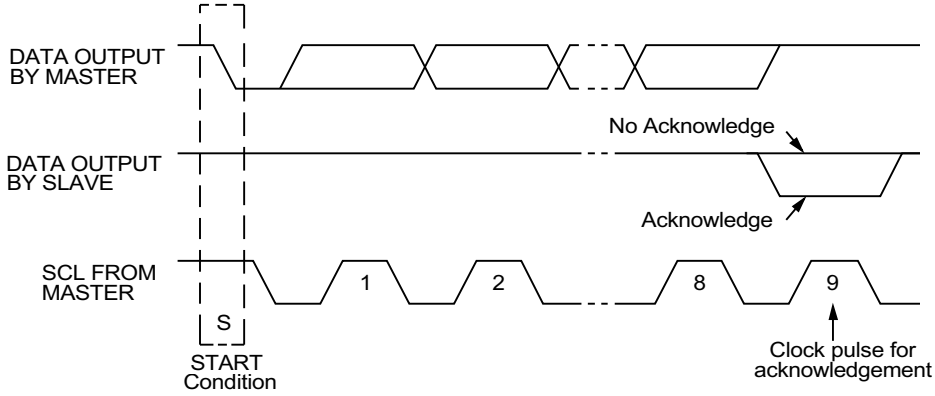
The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the device can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read

operation, the FM31256-G1 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM31256-G1 to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 14. Acknowledge on the I^2C Bus



Slave Address

The first byte that the FM31256-G1 expects after a START condition is the slave address. As shown in Figure 15 and Figure 16, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

The FM31256-G1 has two Slave Addresses (Slave IDs) associated with two logical devices. Bits 7-4 are the device type (slave ID) and should be set to 1010b for the memory device. The other logical device within the FM31256-G1 is the real-time clock and companion. Bits 7-4 are the device type (slave ID) and should be set to 1101b for the RTC and companion. A bus transaction with this slave address will not affect the memory in any way. The figures below illustrate the two Slave Addresses.

Bits 2-1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to four FM31256-G1 devices can reside on the same I^2C bus by assigning a different address to each. Bit 0 is the read/write bit (R/$\overline{W}$). R/$\overline{W}$ = '1' indicates a read operation and R/$\overline{W}$ = '0' indicates a write operation.

Figure 15. Memory Slave Device Address

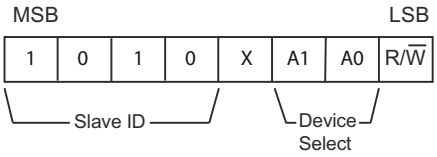
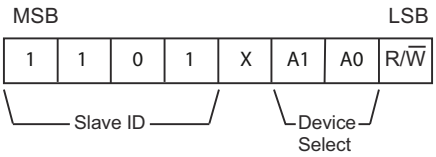


Figure 16. Companion Slave Device Address



Addressing Overview - Memory

After the FM31256-G1 (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 15-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as $V_{DD} > V_{TP}$ or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM31256-G1 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Addressing Overview - RTC & Companion

The RTC and Processor Companion operate in a similar manner to the memory, except that it uses only one byte of address. Addresses 00h to 18h correspond to special function registers. Attempting to load addresses above 18h is an illegal condition; the FM31256-G1 will return a NACK and abort the I^2C transaction.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM31256-G1 can begin. For a read operation the FM31256-G1 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM31256-G1 will transfer the next sequential byte. If the acknowledge is not sent, the FM31256-G1 will end the read operation. For a write operation, the

FM31256-G1 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM31256-G1 is designed to operate in a manner very similar to other I^2C interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM31256-G1 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

The memory address for FM31256-G1 range from 0x0000 to 0x7FFF.

Memory Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/$\overline{W}$ bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM31256-G1 uses no page buffering.

Figure 17 and Figure 18 below illustrate a single-byte and multiple-byte write cycles.

Figure 17. Single-Byte Write

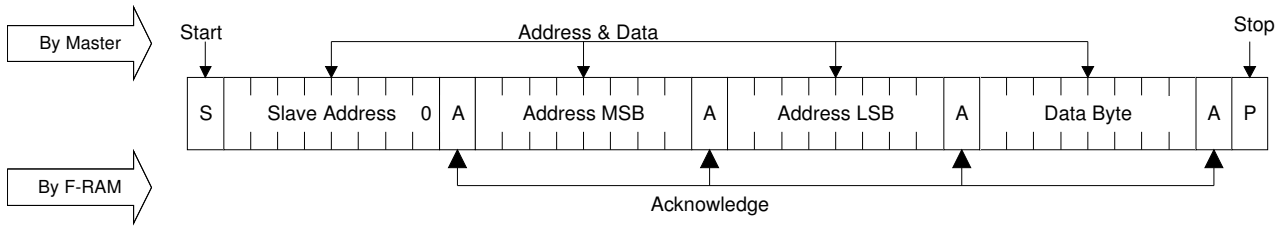
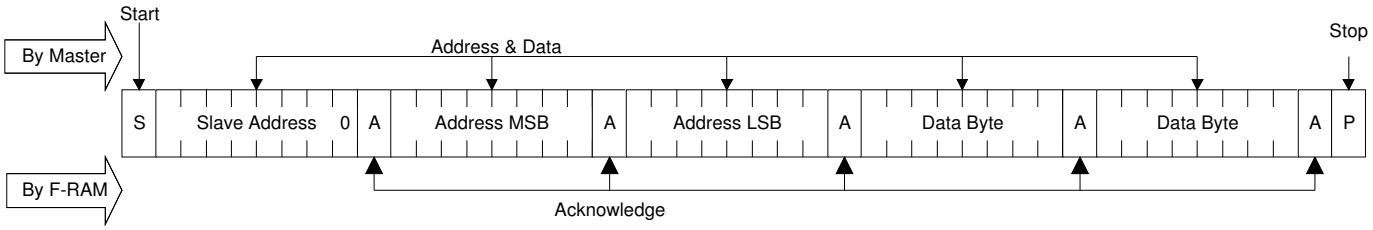


Figure 18. Multi-Byte Write



Memory Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM31256-G1 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM31256-G1 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM31256-G1 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM31256-G1 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM31256-G1 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. Figure 19 and Figure 20 below show the proper operation for current address reads.

Figure 19. Current Address Read

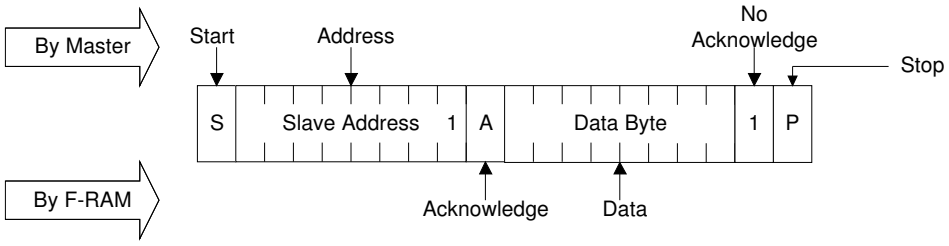
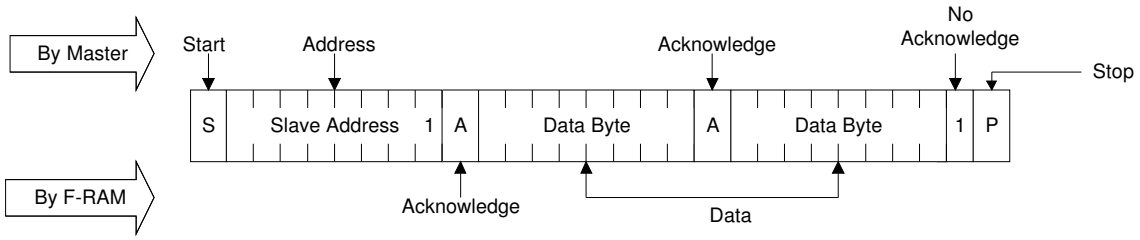


Figure 20. Sequential Read

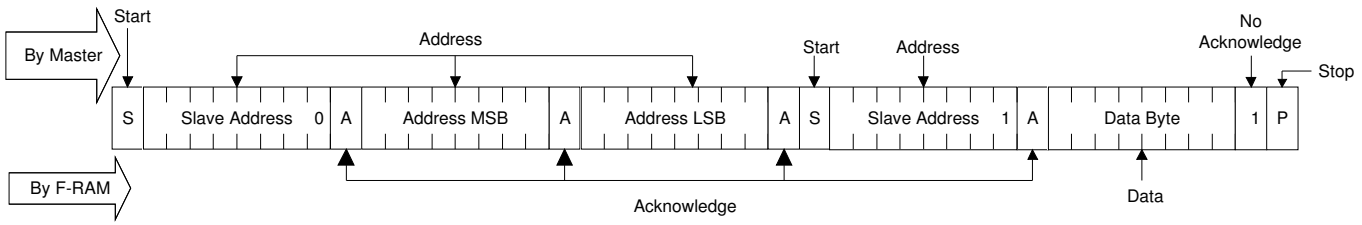


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB ($R/\overline{W}$) set to '0'. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM31256-G1 acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 21. Selective (Random) Read

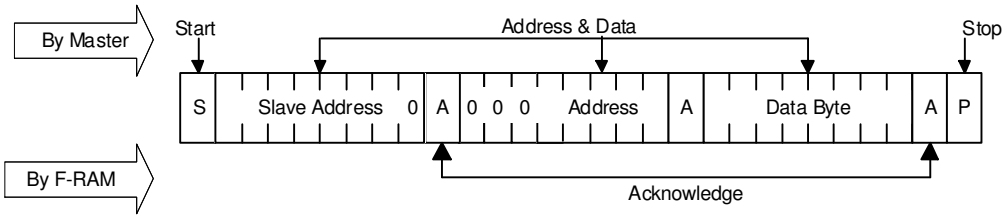


RTC/Companion Write Operation

All RTC and Companion writes operate in a similar manner to memory writes. The distinction is that a different device ID is used and only one byte address is needed instead of two byte address. Figure 22 illustrates a single byte write to this device.

Note Although not required, it is recommended that A5-A7 in the register address byte are zeros in order to preserve compatibility with future devices.

Figure 22. Single Byte Write



RTC/Companion Read Operation

As with writes, a read operation begins with the Slave Address. To perform a register read, the bus master supplies a Slave Address with the LSB set to '1'. This indicates that a read operation is requested. After receiving the complete Slave Address, the FM31256-G1 will begin shifting data out from the current register address on the next clock. Auto-increment operates for the special function registers as with the memory address. A current address read for the registers look exactly like the memory except that the device ID is different.

The FM31256-G1 contains two separate address registers, one for the memory address and the other for the register address. This allows the contents of one address register to be modified without affecting the current address of the other register. For example, this would allow an interrupted read to the memory while still providing fast access to an RTC register. A subsequent memory read will then continue from the memory address where it previously left off, without requiring the load of a new memory address. However, a write sequence always requires an address to be supplied.

Addressing FRAM Array in the FM31256-G1 Family

The FM31256-G1 family includes 256-Kbit memory density. The following 2-byte address field is shown for 256-kbit density.

Part Number	1st Address Byte								2nd Address Byte							
FM31256-G1	X	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Ambient Temperature

with power applied..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +7.0 V

Input voltage ..... –1.0 V to +7.0 V and $V_{IN} < V_{DD} + 1.0$ V

Backup supply voltage.....–1.0 V to +4.5 V

DC voltage applied to outputs
in High-Z state .....–0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on
any pin to ground potential .....–2.0 V to V_{DD} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering
temperature (3 seconds) ..... +260 °C

DC output current
(1 output at a time, 1s duration) ..... 15 mA

Electrostatic Discharge Voltage
Human Body Model (AEC-Q100-002 Rev. D) ..... 2 kV

Charged Device Model (AEC-Q100-011 Rev. B) ..... 1.25 kV

Machine Model (AEC-Q100-003 Rev. E) ..... 100 V

Latch-up current ..... > ±100 mA

Note PFI input voltage must not exceed 4.5 V. The "$V_{IN} < V_{DD}$+1.0 V" restriction does not apply to the SCL and SDA inputs which do not employ a diode to V_{DD}.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	4.0 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{DD}[2]	Power supply			4.0	–	5.5	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.3 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.3 V.	f_{SCL} = 100 kHz	–	–	500	µA
			f_{SCL} = 400 kHz	–	–	900	µA
			f_{SCL} = 1 MHz	–	–	1500	µA
I_{SB}	V_{DD} standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	–	150	µA
V_{BAK}[3]	RTC backup voltage		T_A = +25 °C to +85 °C	1.55	–	3.75	V
			T_A = –40 °C to +25 °C	1.90	–	3.75	V
I_{BAK}	RTC backup current	V_{BAK} = 3.0 V, V_{DD} < 2.4 V, oscillator running, CNT1, CNT2 at V_{BAK}.	T_A = +25 °C, V_{BAK} = 3.0 V	–	–	1.4	µA
			T_A = +85 °C, V_{BAK} = 3.0 V	–	–	2.1	µA
			T_A = +25 °C, V_{BAK} = 2.0 V	–	–	1.15	µA
			T_A = +85 °C, V_{BAK} = 2.0 V	–	–	1.75	µA
I_{BAKTC}[4]	Trickle charge current with V_{BAK} = 0 V		Fast Charge Off (FC = '0')	50	–	120	µA
			Fast Charge On (FC = '1')	200	–	2500	µA

Notes
1. Typical values are at 25 °C, $V_{DD} = V_{DD}$(typ). Not 100% tested.
2. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
3. The V_{BAK} trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
4. V_{BAK} will source current when trickle charge is enabled (VBC bit = '1'), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$ max.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{TP1}	V_{DD} trip point voltage, VTP = 0	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		3.75	3.90	4.00	V
V_{TP2}	V_{DD} trip point voltage, VTP = 1	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		4.20	4.40	4.50	V
V_{RST}[5]	V_{DD} for valid $\overline{RST}$	I_{OL} = 80 µA at V_{OL}	$V_{BAK} > V_{BAK}$ min	0	–	–	V
			$V_{BAK} < V_{BAK}$ min	1.6	–	–	V
I_{LI}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$. Does not apply to A0, A1, X1, PFI, $\overline{RST}$, or X2		–	–	±1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$. Does not apply to $\overline{RST}$, X1, or X2		–	–	±1	µA
V_{IL}[6]	Input LOW voltage		All inputs except as listed below	– 0.3	–	0.3 × V_{DD}	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	– 0.3	–	0.5	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	– 0.3	–	0.8	V
V_{IH}	Input HIGH voltage		All inputs except as listed below	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	V_{BAK} – 0.5	–	V_{BAK} + 0.3	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			PFI (comparator input)	–	–	3.75	V
V_{OH}	Output HIGH voltage	I_{OH} = –2 mA		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		–	–	0.4	V
R_{RST}	Pull-up resistance for $\overline{RST}$ inactive			50	–	400	kΩ
R_{in}	Input resistance (A1-A0)	For $V_{IN} = V_{IL}(Max_)$		20	–	–	kΩ
		For $V_{IN} = V_{IH}$(Min)		1	–	–	MΩ
V_{PFI}	Power fail input reference voltage			1.140	1.20	1.225	V
V_{HYS}	Power fail input (PFI) hysteresis (rising)			–	–	100	mV

Notes
5. The minimum V_{DD} to guarantee the level of $\overline{RST}$ remains a valid V_{OL} level.
6. Includes $\overline{RST}$ input detection of external reset condition to trigger driving of $\overline{RST}$ signal by FM31256-G1.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

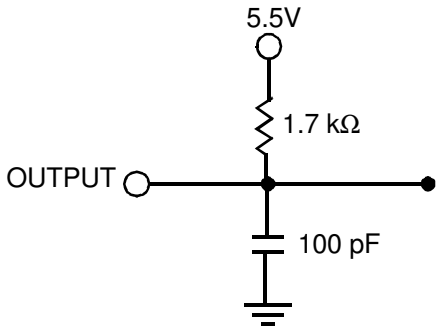
Parameter [7]	Description	Test Conditions	Typ	Max	Unit
C_{IO}	Input/Output pin capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	–	8	pF
C_{XTL} [8]	X1, X2 crystal pin capacitance		12	–	pF

Thermal Resistance

Parameter	Description	Test Conditions	14-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	80	°C/W
Θ_{JC}	Thermal resistance (junction to case)		29	°C/W

AC Test Loads and Waveforms

Figure 23. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....10 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 100 pF

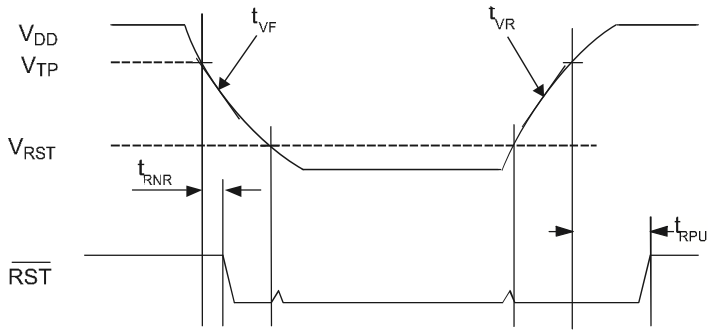
Notes
7. This parameter is characterized and not 100% tested.
8. The crystal attached to the X1/X2 pins must be rated as 12.5 pF.

Supervisor Timing

Over the Operating Range

Parameter	Description	Min	Max	Units
t_{RPU}	$\overline{RST}$ active (LOW) after $V_{DD} > V_{TP}$	100	200	ms
t_{RNR}[9]	$\overline{RST}$ response time to $V_{DD} < V_{TP}$ (noise filter)	10	25	µs
t_{VR}[9, 10]	V_{DD} power-up ramp rate	50	-	µs/V
t_{VF}[9, 10]	V_{DD} power-down ramp rate	100	-	µs/V
t_{WDP}[11]	Pulse width of $\overline{RST}$ for watchdog reset	100	200	ms
t_{WDOG}[11]	Timeout of watchdog	t_{DOG}	$2 \times t_{DOG}$	ms
f_{CNT}	Frequency of event counters	0	10	MHz
t_{OSC}	RTC Oscillator time to start	-	2	s

Figure 24. $\overline{RST}$ Timing



Notes
9. This parameter is characterized and not 100% tested.
10. Slope measured at any point on V_{DD} waveform.
11. t_{DOG} is the programmed time in register in register 0Ah, $V_{DD} > V_{TP}$, and t_{RPU} satisfied.

AC Switching Characteristics

Over the Operating Range

Parameter[12]	Alt. Parameter	Description	Min	Max	Min	Max	Min	Max	Unit
f_{SCL}		SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{SU;\ STA}$		Start condition setup for repeated Start	4.7	–	0.6	–	0.25	–	µs
$t_{HD;STA}$		Start condition hold time	4.0	–	0.6	–	0.25	–	µs
t_{LOW}		Clock LOW period	4.7	–	1.3	–	0.6	–	µs
t_{HIGH}		Clock HIGH period	4.0	–	0.6	–	0.4	–	µs
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	250	–	100	–	100	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	–	0	–	ns
t_{DH}		Data output hold (from SCL @ V_{IL})	0	–	0	–	0	–	ns
t_R[13]	t_r	Input rise time	–	1000	–	300	–	300	ns
t_F[13]	t_f	Input fall time	–	300	–	300	–	100	ns
$t_{SU;STO}$		STOP condition setup	4	–	0.6		0.25	–	µs
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	3		0.9	–	0.55	µs
t_{BUF}		Bus free before new transmission	4.7	–	1.3	–	0.5	–	µs
t_{SP}		Noise suppression time constant on SCL, SDA	–	50		50	–	50	ns

Figure 25. Read Bus Timing Diagram

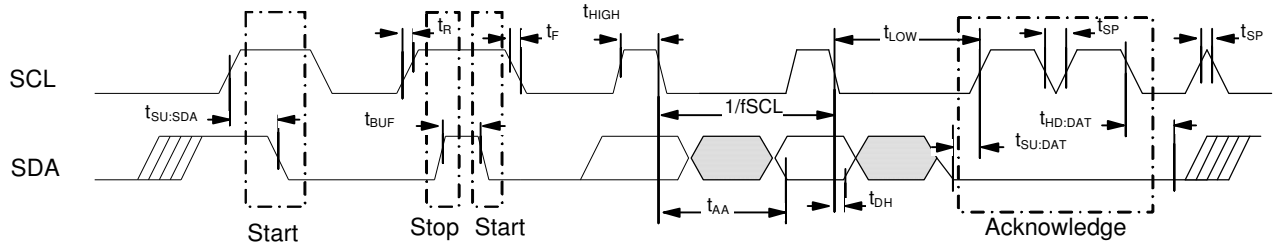
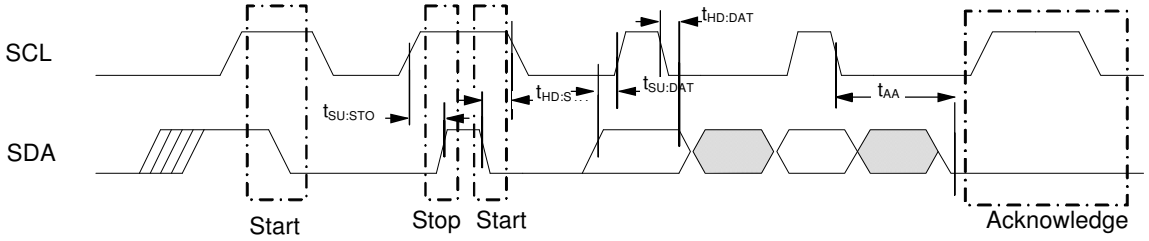


Figure 26. Write Bus Timing Diagram



Notes

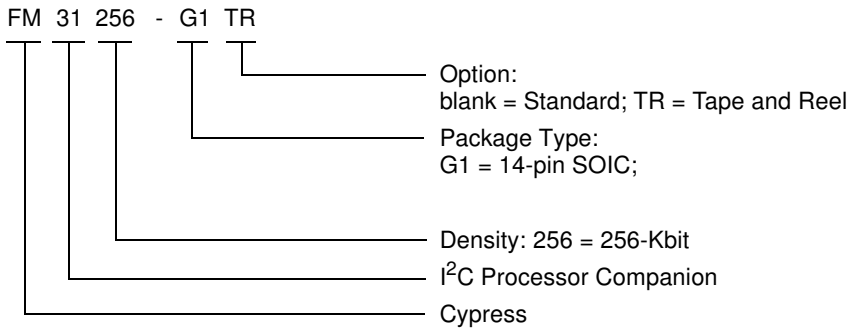
12. Test conditions assume a signal transition time of 10 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 100 pF load capacitance shown in page 26.
13. This parameter is characterized and not 100% tested.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM31256-G1	51-85067	14-pin SOIC	Industrial
FM31256-G1TR	51-85067	14-pin SOIC	

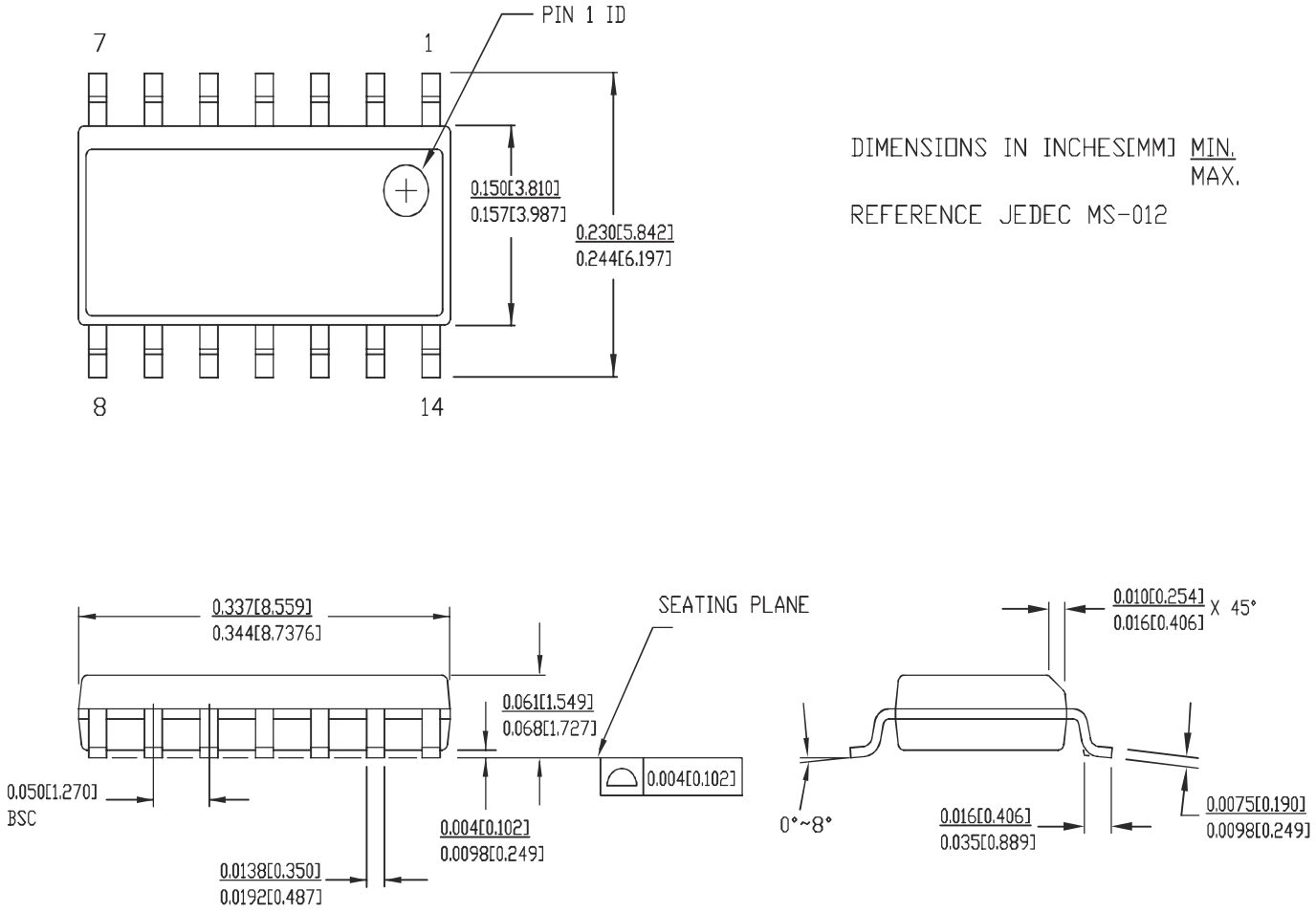
All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 27. 14-pin SOIC (150 Mils) Package Outline, 51-85067



51-85067 *D

Acronyms

Acronym	Description
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
NMI	Non Maskable interrupt
RoHS	Restriction of Hazardous Substances
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
℃	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM31256-G1, 256-Kbit Integrated Processor Companion with F-RAM Document Number: 002-23029				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**		GVCH	04/06/2018	New spec

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FM31276/FM31278

64-Kbit/256-Kbit Integrated Processor Companion with F-RAM

Features

- 64-Kbit/256-Kbit ferroelectric random access memory (F-RAM)
  - Logically organized as 8 K × 8 (FM31276) / 32 K × 8 (FM31278)
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See the Data Retention and Endurance table)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- High Integration Device Replaces Multiple Parts
  - Serial nonvolatile memory
  - Real time clock (RTC)
  - Low voltage reset
  - Watchdog timer
  - Early power-fail warning/NMI
  - Two 16-bit event counter
  - Serial number with write-lock for security
- Real-time Clock/Calendar
  - Backup current at 2 V: 1.15 µA at +25 °C
  - Seconds through centuries in BCD format
  - Tracks leap years through 2099
  - Uses standard 32.768 kHz crystal (6 pF/12.5 pF)
  - Software calibration
  - Supports battery or capacitor backup
- Processor Companion
  - Active-low reset output for V_{DD} and watchdog
  - Programmable low-V_{DD} reset trip point
  - Manual reset filtered and debounced
  - Programmable watchdog timer
  - Dual Battery-backed event counter tracks system intrusions or other events
  - Comparator for power-fail interrupt
  - 64-bit programmable serial number with lock
- Fast 2-wire serial interface (I^2C)
  - Up to 1-MHz frequency
  - Supports legacy timings for 100 kHz and 400 kHz
  - RTC, Supervisor controlled via I^2C interface
  - Device select pins for up to 4 memory devices
- Low power consumption
  - 1.5 mA active current at 1 MHz
  - 150 µA standby current
- Operating voltage: V_{DD} = 4.0 V to 5.5 V
- Industrial temperature: –40 °C to +85 °C
- 14-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant
- Underwriters laboratory (UL) recognized

Functional Overview

The FM31276/FM31278 device integrates F-RAM memory with the most commonly needed functions for processor-based systems. Major features include nonvolatile memory, real time clock, low-V_{DD} reset, watchdog timer, nonvolatile event counter, lockable 64-bit serial number area, and general purpose comparator that can be used for a power-fail (NMI) interrupt or any other purpose.

The FM31276/FM31278 is a 64-Kbit/256-Kbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. This memory is truly nonvolatile rather than battery backed. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by other nonvolatile memories. The FM31276/FM31278 is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

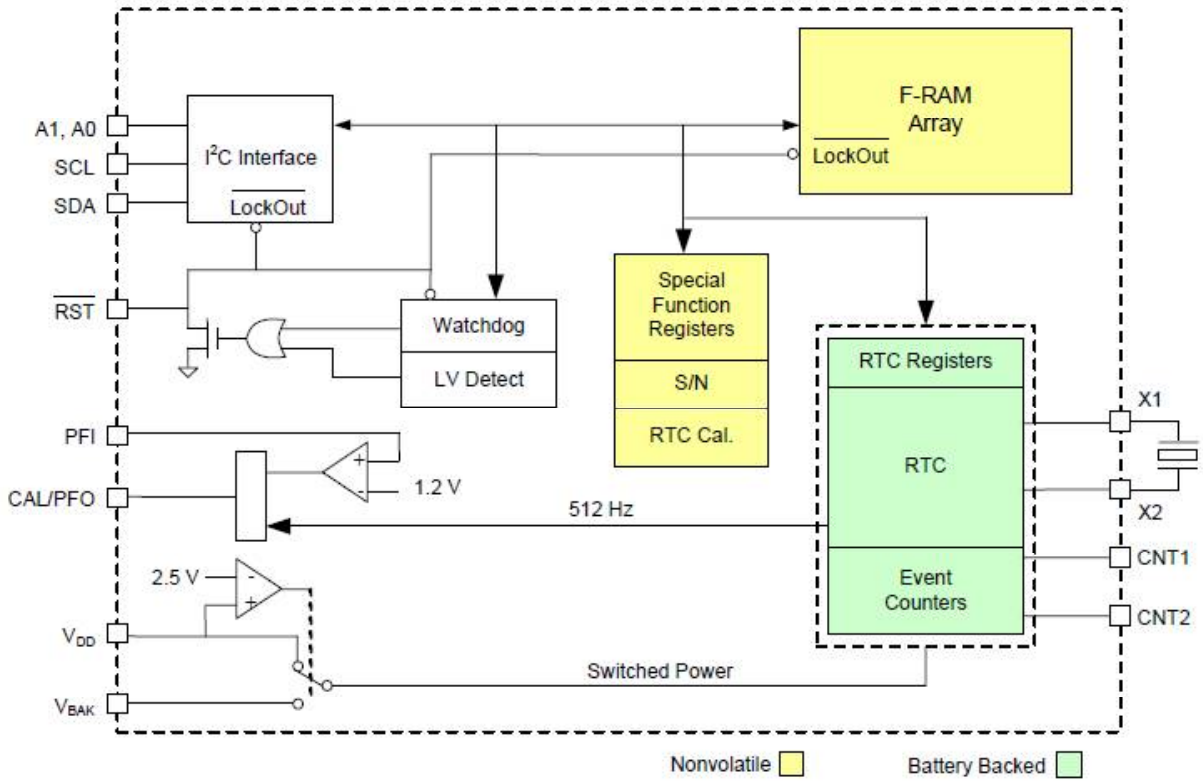
The real time clock (RTC) provides time and date information in BCD format. It can be permanently powered from an external backup voltage source, either a battery or a capacitor. The timekeeper uses a common external 32.768 kHz crystal and provides a calibration mode that allows software adjustment of timekeeping accuracy.

The processor companion includes commonly needed CPU support functions. Supervisory functions include a reset output signal controlled by either a low V_{DD} condition or a watchdog timeout. $\overline{RST}$ goes active when V_{DD} drops below a programmable threshold and remains active for 100 ms after V_{DD} rises above the trip point. A programmable watchdog timer runs from 100 ms to 3 seconds. The watchdog timer is optional, but if enabled it will assert the reset signal for 100 ms if not restarted by the host before the timeout. A flag-bit indicates the source of the reset.

A comparator on PFI compares an external input pin to the onboard 1.2 V reference. This is useful for generating a power-fail interrupt (NMI) but can be used for any purpose. The family also includes a programmable 64-bit serial number that can be locked making it unalterable. Additionally it offers a dual battery-backed event counter that tracks the number of rising or falling edges detected on a dedicated input pin.

For a complete list of related documentation, click here.

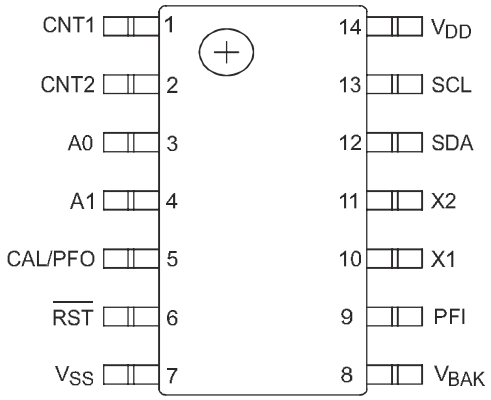
Logic Block Diagram



Contents

Pinout

Figure 1. 14-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A1-A0	Input	**Device Select Address 1-0**. These pins are used to select one of up to 4 devices of the same type on the same I^2C bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data/Address**. This is a bi-directional pin for the I^2C interface. It is open-drain and is intended to be wire-OR'd with other devices on the I^2C bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the I^2C interface. Data is clocked out of the device on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
CNT1, CNT2	Input	**Event Counter Inputs**. These battery-backed inputs increment counters when an edge is detected on the corresponding CNT pin. The polarity is programmable. These pins should not be left floating. Tie to ground if these pins are not used.
X1, X2	Input/Output	32.768 kHz crystal connection. When using an external oscillator, apply the clock to X1 and a DC mid-level to X2. These pins should be left unconnected if RTC is not used.
$\overline{RST}$	Input/Output	**Reset**. This active-low output is open drain with weak pull-up. It is also an input when used as a manual reset. This pin should be left floating if unused.
PFI	Input	**Early Power-fail Input**. Typically connected to an unregulated power supply to detect an early power failure. This pin must be tied to ground if unused.
CAL/PFO	Output	**Calibration/Early Power-fail Output**. In calibration mode, this pin supplies a 512 Hz square-wave output for clock calibration. In normal operation, this is the early power-fail output.
V_{BAK}	Power supply	**Backup supply voltage**. Connected to a 3 V battery or a large value capacitor. If no backup supply is used, this pin should be tied to ground and the VBC bit should be cleared in the RTC register 0Bh. The trickle charger is UL recognized and ensures no excessive current when using a lithium battery.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.

Overview

The FM31276/FM31278 device combines a serial nonvolatile RAM with a real time clock (RTC) and a processor companion. The companion is a highly integrated peripheral including a processor supervisor, a comparator used for early power-fail warning, nonvolatile event counters, and a 64-bit serial number. The FM31276/FM31278 integrates these complementary but distinct functions under a common interface in a single package. The product is organized as two logical devices. The first is a memory and the second is the companion which includes all the remaining functions. From the system perspective they appear to be two separate devices with unique IDs on the serial bus.

The memory is organized as a standalone nonvolatile I^2C memory using standard device ID value. The real time clock and supervisor functions are accessed with a separate I^2C device ID. This allows clock/calendar data to be read while maintaining the most recently used memory address. The clock and supervisor functions are controlled by 25 special function registers. The RTC and event counter circuits are maintained by the power source on the V_{BAK} pin, allowing them to operate from battery or backup capacitor power when V_{DD} drops below a set threshold. Each functional block is described below.

Memory Architecture

The FM31276/FM31278 device is available in memory size 64-Kbit/256-Kbit. The device uses two-byte addressing for the memory portion of the chip. This makes the device software compatible with its standalone memory counterparts, but makes them compatible within the entire family.

The memory array is logically organized as 8,192 × 8 bits / 32,768 × 8 bits and is accessed using an industry-standard I^2C interface. The memory is based on F-RAM technology. Therefore it can be treated as RAM and is read or written at the speed of the I^2C bus with no delays for write operations. It also offers effectively unlimited write endurance unlike other nonvolatile memory technologies. The I^2C protocol is described on page 19.

The memory array can be write-protected by software. Two bits in the processor companion area (WP1, WP0 in register 0Bh) control the protection setting. Based on the setting, the protected addresses cannot be written and the I^2C interface will not acknowledge any data to protected addresses. The special function registers containing these bits are described in detail below.

Table 1. Block Memory Write Protection

WP1	WP0	Protected Address Range
0	0	None
0	1	Bottom 1/4
1	0	Bottom 1/2
1	1	Full array

Processor Companion

In addition to nonvolatile RAM, the FM31276/FM31278 incorporates a real time clock and highly integrated processor companion. The companion includes a low-V_{DD} reset, a programmable watchdog timer, a battery-backed event counters, a comparator for early power-fail detection or other purposes, and a 64-bit serial number.

Processor Supervisor

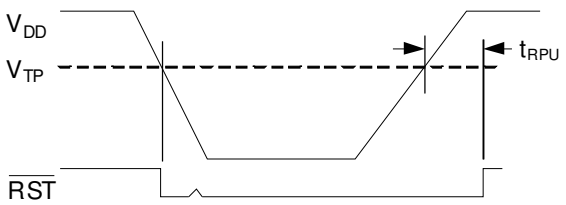
Supervisors provide a host processor two basic functions: detection of power supply fault conditions and a watchdog timer to escape a software lockup condition. The FM31276/FM31278 has a reset pin ($\overline{RST}$) to drive a processor reset input during power faults, power-up, and software lockups. It is an open drain output with a weak internal pull-up to V_{DD}. This allows other reset sources to be wire-OR'd to the $\overline{RST}$ pin. When V_{DD} is above the programmed trip point, $\overline{RST}$ output is pulled weakly to V_{DD}. If V_{DD} drops below the reset trip point voltage level (V_{TP}), the $\overline{RST}$ pin will be driven LOW. It will remain LOW until V_{DD} falls too low for circuit operation which is the V_{RST} level. When V_{DD} rises again above V_{TP}, $\overline{RST}$ continues to drive LOW for at least 100 ms (t_{RPU}) to ensure a robust system reset at a reliable V_{DD} level. After t_{RPU} has been met, the $\overline{RST}$ pin will return to the weak HIGH state. While $\overline{RST}$ is asserted, serial bus activity is locked out even if a transaction occurred as V_{DD} dropped below V_{TP}. A memory operation started while V_{DD} is above V_{TP} will be completed internally.

Table 1 below shows how bit VTP controls the trip point of the low-V_{DD} reset. They are located in register 0Bh, bits 1 and 0. The reset pin will drive LOW when V_{DD} is below the selected V_{TP} voltage, and the I^2C interface and F-RAM array will be locked out. Note that the bit 1 location is a don't care. Figure 2 illustrates the reset operation in response to a low V_{DD}.

Table 2. VTP setting

VTP Setting	VTP
3.9 V	0
4.4 V	1

Figure 2. Low V_{DD} Reset



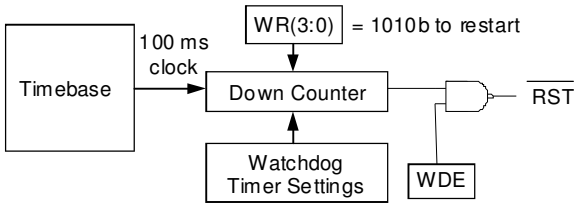
A watchdog timer can also be used to drive an active reset signal. The watchdog is a free-running programmable timer. The timeout period can be software programmed from 100 ms to 3 seconds in 100 ms increments via a 5-bit nonvolatile register. All programmed settings are minimum values and vary with

temperature according to the operating specifications. The watchdog has two additional controls associated with its operation, a watchdog enable bit (WDE) and timer restart bits (WR). Both the enable bit must be set and the watchdog must timeout in order to drive $\overline{RST}$ active. If a reset event occurs, the timer will automatically restart on the rising edge of the reset pulse. If WDE = '0', the watchdog timer runs but a watchdog fault will not cause $\overline{RST}$ to be asserted LOW. The WTR flag will be set, indicating a watchdog fault. This setting is useful during software development if the developer does not want $\overline{RST}$ to drive. Note that setting the maximum timeout setting (11111b) disables the counter to save power. The second control is a nibble that restarts the timer preventing a reset. The timer should be restarted after changing the timeout value.

The watchdog timeout value is located in register 0Ah, bits 4:0, and the watchdog enable is bit 7. The watchdog is restarted by writing the pattern 1010b to the lower nibble of register 09h. Writing this pattern will also cause the timer to load new timeout values. Writing other patterns to this address will not affect its operation. Note the watchdog timer is free-running. Prior to enabling it, users should restart the timer as described above. This assures that the full timeout period will be set immediately after enabling. The watchdog is disabled when V_{DD} is below V_{TP}. The following table summarizes the watchdog bits. A block diagram follows.

Watchdog Timeout	WDT(4:0)	0Ah, bits 4:0
Watchdog Enable	WDE	0Ah, bit 7
Watchdog Restart	WR(3:0)	09h, bits 3:0

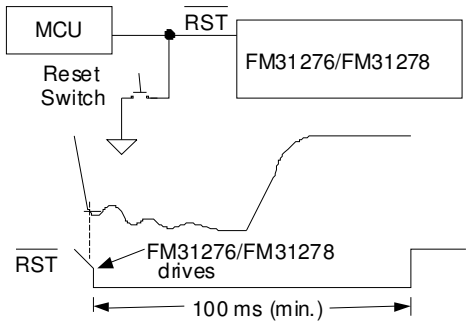
Figure 3. Watchdog Timer



Manual Reset

The $\overline{RST}$ is a bi-directional signal allowing the FM31276/FM31278 to filter and de-bounce a manual reset switch. The $\overline{RST}$ input detects an external low condition and responds by driving the $\overline{RST}$ signal LOW for 100 ms.

Figure 4. Manual Reset



Note The internal weak pull-up eliminates the need for additional external components.

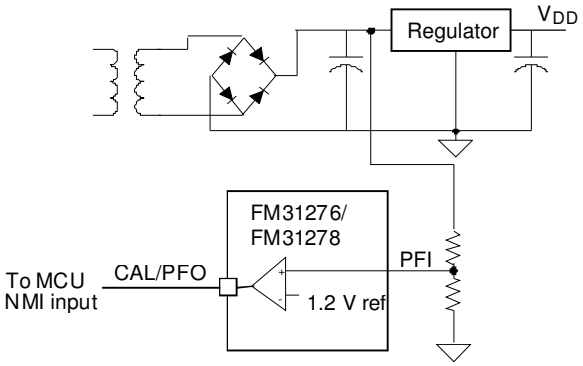
Reset Flags

In case of a reset condition, a flag bit will be set to indicate the source of the reset. A low-V_{DD} reset is indicated by the POR flag, register 09h bit 6. A watchdog reset is indicated by the WTR flag, register 09h bit 7. Note that the flags are internally set in response to reset sources, but they must be cleared by the user. When the register is read, it is possible that both flags are set if both have occurred since the user last cleared them.

Early Power Fail Comparator

An early power fail warning can be provided to the processor well before V_{DD} drops out of spec. The comparator is used to create a power fail interrupt (NMI). This can be accomplished by connecting the PFI pin to the unregulated power supply via a resistor divider. An application circuit is shown below.

Figure 5. Comparator as a Power-Fail Warning



The voltage on the PFI input pin is compared to an onboard 1.2 V reference. When the PFI input voltage drops below this threshold, the comparator will drive the CAL/PFO pin to a lLOW state. The comparator has 100 mV (max) of hysteresis to reduce noise sensitivity, only for a rising PFI signal. For a falling PFI edge, there is no hysteresis.

The comparator is a general purpose device and its application is not limited to the NMI function.

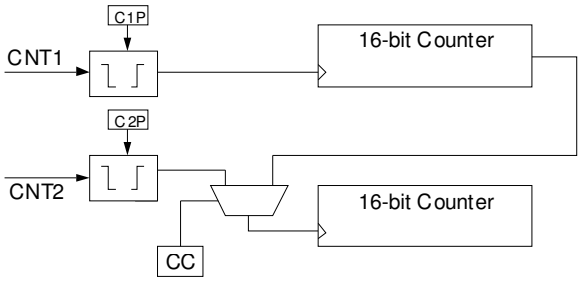
The comparator is not integrated into the special function registers except as it shares its output pin with the CAL output. When the RTC calibration mode is invoked by setting the CAL bit (register 00h, bit 2), the CAL/PFO output pin will be driven with a 512 Hz square wave and the comparator will be ignored. Since most users only invoke the calibration mode during production, this should have no impact on system operations using the comparator.

Note The maximum voltage on the comparator input PFI is limited to 3.75 V under normal operating conditions.

Event Counter

The FM31276/FM31278 offers the user two battery-backed event counters. Input pins CNT1 and CNT2 are programmable edge detectors. Each clocks a 16-bit counter. When an edge occurs, the counters will increment their respective registers. Counter 1 is located in registers 0Dh and 0Eh, Counter 2 is located in registers 0Fh and 10h. These register values can be read anytime V_{DD} is above V_{TP}, and they will be incremented as long as a valid V_{BAK} power source is provided. To read, set the RC bit, register 0Ch bit 3 to 1. This takes a snapshot of all four counter bytes allowing a stable value even if a count occurs during the read. The registers can be written by software allowing the counters to be cleared or initialized by the system. Counts are blocked during a write operation. The two counters can be cascaded to create a single 32-bit counter by setting the CC control bit (register 0Ch, bit 2). When cascaded, the CNT1 input will cause the counter to increment. CNT2 is not used in this mode and should be tied to ground.

Figure 6. Event Counter



The control bits for event counting are located in register 0Ch. Counter 1 Polarity is bit C1P, bit 0; Counter 2 Polarity is C2P, bit 1; the Cascade Control is CC, bit 2; and the Read Counter bit is RC, bit 3.

The polarity bits must be set prior to setting the counter value(s). If a polarity bit is changed, the counter may inadvertently increment. If the counter pins are not being used, tie them to ground.

Serial Number

A memory location to write a 64-bit serial number is provided. It is a writeable nonvolatile memory block that can be locked by the user once the serial number is set. The 8 bytes of data and the lock bit are all accessed via the device ID for the Processor Companion. Therefore the serial number area is separate and distinct from the memory array. The serial number registers can be written an unlimited number of times, so these locations are general purpose memory. However, once the lock bit is set, the values cannot be altered and the lock cannot be removed. Once locked the serial number registers can still be read by the system.

The serial number is located in registers 11h to 18h. The lock bit is SNL (register 0Bh, bit 7). Setting the SNL bit to a '1' disables writes to the serial number registers, and the SNL bit cannot be cleared.

Real-time Clock Operation

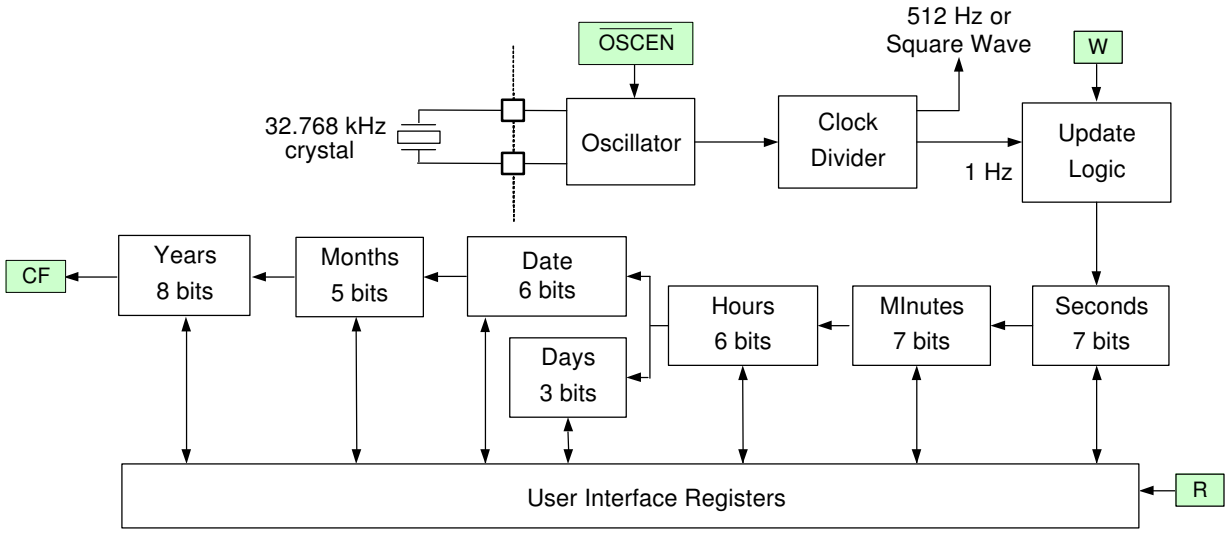
The real-time clock (RTC) is a timekeeping device that can be battery or capacitor backed for permanently-powered operation. It offers a software calibration feature that allows high accuracy.

The RTC consists of an oscillator, clock divider, and a register system for user access. It divides down the 32.768 kHz time-base and provides a minimum resolution of seconds (1 Hz). Static registers provide the user with read/write access to the time values. It includes registers for seconds, minutes, hours, day-of-the-week, date, months, and years. A block diagram (Figure 7) illustrates the RTC function.

The user registers are synchronized with the timekeeper core using R and W bits in register 00h described below. Changing the R bit from '0' to '1' transfers timekeeping information from the core into holding registers that can be read by the user. If a timekeeper update is pending when R is set, then the core will be updated prior to loading the user registers. The registers are frozen and will not be updated again until the R bit is cleared to '0'. R is used for reading the time.

Setting the W bit to '1' locks the user registers. Clearing it to '0' causes the values in the user registers to be loaded into the timekeeper core. W bit is used for writing new time values. Users should be certain not to load invalid values, such as FFh, to the timekeeping registers. Updates to the timekeeping core occur continuously except when locked.

Figure 7. Real-time Clock Core Block Diagram

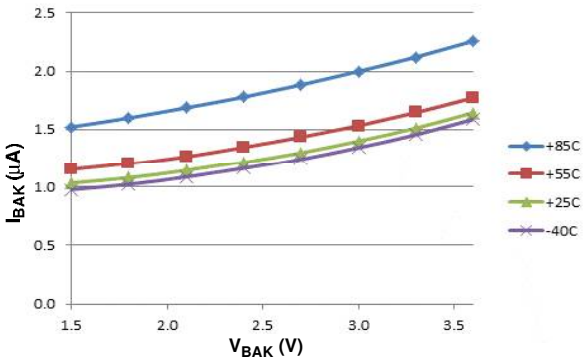


Backup Power

The real-time clock/calendar is intended to be permanently powered. When the primary system power fails, the voltage on the V_{DD} pin will drop. When V_{DD} is less than 2.5 V, the RTC (and event counters) will switch to the backup power supply on V_{BAK}. The clock operates at extremely low current in order to maximize battery or capacitor life. However, an advantage of combining a clock function with F-RAM memory is that data is not lost regardless of the backup power source.

The I_{BAK} current varies with temperature and voltage (see DC Electrical Characteristics table). The following graph shows I_{BAK} as a function of V_{BAK}. These curves are useful for calculating backup time when a capacitor is used as the V_{BAK} source.

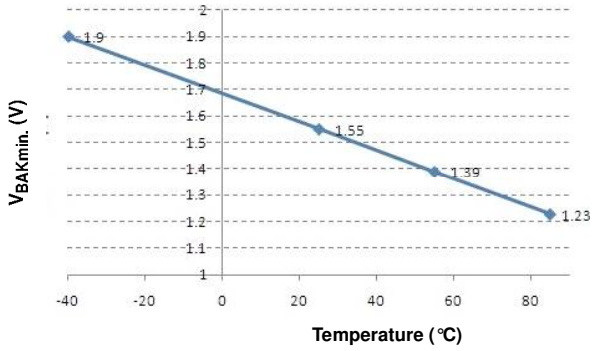
Figure 8. I_{BAK} vs. V_{BAK} Voltage



The minimum V_{BAK} voltage varies linearly with temperature. The user can expect the minimum V_{BAK} voltage to be 1.23 V at +85 °C and 1.90 V at -40 °C. The tested limit is 1.55 V at +25 °C.

Note The minimum V_{BAK} voltage has been characterized at -40 °C and +85 °C but is not 100% tested.

Figure 9. V_{BAK}(min.) vs Temperature



Trickle Charger

To facilitate capacitor backup the V_{BAK} pin can optionally provide a trickle charge current. When the VBC bit (register 0Bh, bit 2) is set to '1', the V_{BAK} pin will source approximately 80 µA until V_{BAK} reaches 3.75 V. In 5 V systems, this charges the capacitor to V_{DD} without an external diode and resistor charger and also prevents the user from exceeding the V_{BAK} maximum voltage specification. There is a Fast Charge mode which is enabled by the FC bit (register 0Bh, bit 5). In this mode the trickle charger current is set to approximately 1 mA, allowing a large backup capacitor to charge more quickly.

In the case where no battery is used, the V_{BAK} pin should be tied to V_{SS}. V_{BAK} should not be tied to 5 V since the V_{BAK} (max) specification will be exceeded. Be sure to turn off the trickle charger (VBC = '0'), otherwise charger current will be shunted to ground from V_{DD}.

Note Systems using lithium batteries should clear the VBC bit to '0' to prevent battery charging. The V_{BAK} circuitry includes an internal 1 KΩ series resistor as a safety element. The trickle charger is UL Recognized.

Calibration

When the CAL bit in the register 00h is set to '1', the clock enters calibration mode. In calibration mode, the CAL/PFO output pin is dedicated to the calibration function and the power fail output is temporarily unavailable. Calibration operates by applying a digital correction to the counter based on the frequency error. In this mode, the CAL/PFO pin is driven with a 512 Hz (nominal) square wave. Any measured deviation from 512 Hz translates into a timekeeping error. The user converts the measured error in ppm and writes the appropriate correction value to the calibration register. The correction factors are listed in the table below. Positive ppm errors require a negative adjustment that removes pulses. Negative ppm errors require a positive correction that adds pulses. Positive ppm adjustments have the CALS (sign) bit set to '1', whereas negative ppm adjustments have CALS = '0'. After calibration, the clock will have a maximum error of ±2.17 ppm or ±0.09 minutes per month at the calibrated temperature.

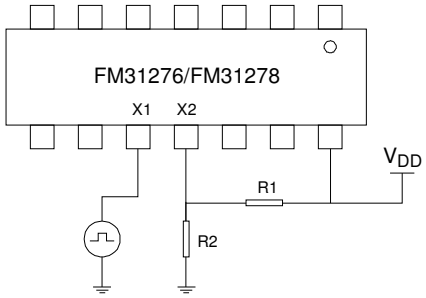
The calibration setting is stored in F-RAM so it is not lost should the backup source fail. It is accessed with bits CAL(4:0) in register 01h. This value can be written only when the CAL bit is set to a '1'. To exit the calibration mode, the user must clear the CAL bit to a '0'. When the CAL bit is '0', the CAL/PFO pin will revert to the power fail output function.

Crystal Oscillator

The crystal oscillator is designed to use a 6 pF/12.5 pF crystal without the need for external components, such as loading capacitors. The FM31276/FM31278 device has built-in loading capacitors that are optimized for use with 6 pF crystals, but which work well with 12.5 pF crystals. For either crystal, no additional external loading capacitors are required nor suggested.

If a 32.768 kHz crystal is not used, an external oscillator may be connected to the FM31276/FM31278. Apply the oscillator to the X1 pin. Its high and low voltage levels can be driven rail-to-rail or amplitudes as low as approximately 500 mV p-p. To ensure proper operation, a DC bias must be applied to the X2 pin. It should be centered between the high and low levels on the X1 pin. This can be accomplished with a voltage divider.

Figure 10. External Oscillator

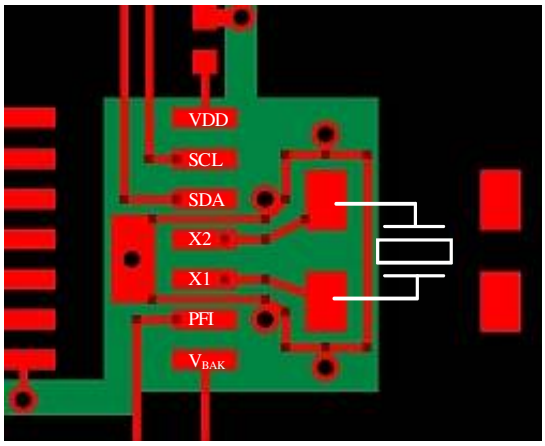


In the example, R1 and R2 are chosen such that the X2 voltage is centered around the X1 oscillator drive levels. If you wish to avoid the DC current, you may choose to drive X1 with an external clock and X2 with an inverted clock using a CMOS inverter.

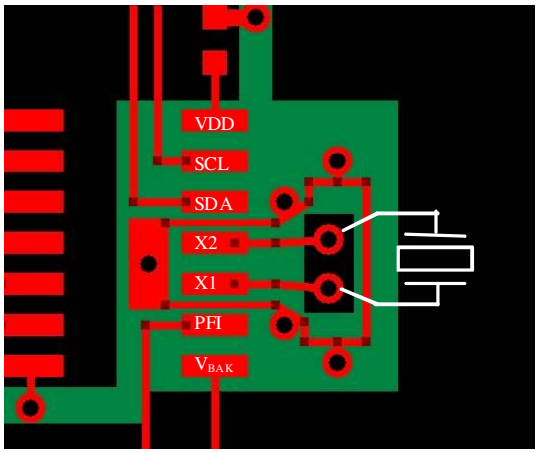
Layout Recommendations

The X1 and X2 crystal pins employ very high impedance circuits and the oscillator connected to these pins can be upset by noise or extra loading. To reduce RTC clock errors from signal switching noise, a guard ring must be placed around these pads and the guard ring grounded. SDA and SCL traces should be routed away from the X1 / X2 pads. The X1 and X2 trace lengths should be less than 5 mm. The use of a ground plane on the backside or inner board layer is preferred. See layout example. Red is the top layer, green is the bottom layer.

Figure 11. Layout Recommendations



Layout for Surface Mount Crystal
(red = top layer, green = bottom layer)



Layout for Through Hole Crystal
(red = top layer, green = bottom layer)

Table 3. Digital Calibration Adjustments

Positive Calibration for slow clocks: Calibration will achieve ±2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	511.9989	0	2.17	000000
1	511.9989	511.9967	2.18	6.51	100001
2	511.9967	511.9944	6.52	10.85	100010
3	511.9944	511.9922	10.86	15.19	100011
4	511.9922	511.9900	15.20	19.53	100100
5	511.9900	511.9878	19.54	23.87	100101
6	511.9878	511.9856	23.88	28.21	100110
7	511.9856	511.9833	28.22	32.55	100111
8	511.9833	511.9811	32.56	36.89	101000
9	511.9811	511.9789	36.90	41.23	101001
10	511.9789	511.9767	41.24	45.57	101010
11	511.9767	511.9744	45.58	49.91	101011
12	511.9744	511.9722	49.92	54.25	101100
13	511.9722	511.9700	54.26	58.59	101101
14	511.9700	511.9678	58.60	62.93	101110
15	511.9678	511.9656	62.94	67.27	101111
16	511.9656	511.9633	67.28	71.61	110000
17	511.9633	511.9611	71.62	75.95	110001
18	511.9611	511.9589	75.96	80.29	110010
19	511.9589	511.9567	80.30	84.63	110011
20	511.9567	511.9544	84.64	88.97	110100
21	511.9544	511.9522	88.98	93.31	110101
22	511.9522	511.9500	93.32	97.65	110110
23	511.9500	511.9478	97.66	101.99	110111
24	511.9478	511.9456	102.00	106.33	111000
25	511.9456	511.9433	106.34	110.67	111001
26	511.9433	511.9411	110.68	115.01	111010
27	511.9411	511.9389	115.02	119.35	111011
28	511.9389	511.9367	119.36	123.69	111100
29	511.9367	511.9344	123.70	128.03	111101
30	511.9344	511.9322	128.04	132.37	111110
31	511.9322	511.9300	132.38	136.71	111111

Table 3. Digital Calibration Adjustments (continued)

Negative Calibration for fast clocks: Calibration will achieve ±2.17 PPM after calibration					
	Measured Frequency Range		Error Range (PPM)		
	Min	Max	Min	Max	Program Calibration Register to:
0	512.0000	512.0011	0	2.17	000000
1	512.0011	512.0033	2.18	6.51	000001
2	512.0033	512.0056	6.52	10.85	000010
3	512.0056	512.0078	10.86	15.19	000011
4	512.0078	512.0100	15.20	19.53	000100
5	512.0100	512.0122	19.54	23.87	000101
6	512.0122	512.0144	23.88	28.21	000110
7	512.0144	512.0167	28.22	32.55	000111
8	512.0167	512.0189	32.56	36.89	001000
9	512.0189	512.0211	36.90	41.23	001001
10	512.0211	512.0233	41.24	45.57	001010
11	512.0233	512.0256	45.58	49.91	001011
12	512.0256	512.0278	49.92	54.25	001100
13	512.0278	512.0300	54.26	58.59	001101
14	512.0300	512.0322	58.60	62.93	001110
15	512.0322	512.0344	62.94	67.27	001111
16	512.0344	512.0367	67.28	71.61	010000
17	512.0367	512.0389	71.62	75.95	010001
18	512.0389	512.0411	75.96	80.29	010010
19	512.0411	512.0433	80.30	84.63	010011
20	512.0433	512.0456	84.64	88.97	010100
21	512.0456	512.0478	88.98	93.31	010101
22	512.0478	512.0500	93.32	97.65	010110
23	512.0500	512.0522	97.66	101.99	010111
24	512.0522	512.0544	102.00	106.33	011000
25	512.0544	512.0567	106.34	110.67	011001
26	512.0567	512.0589	110.68	115.01	011010
27	512.0589	512.0611	115.02	119.35	011011
28	512.0611	512.0633	119.36	123.69	011100
29	512.0633	512.0656	123.70	128.03	011101
30	512.0656	512.0678	128.04	132.37	011110
31	512.0678	512.0700	132.38	136.71	011111

Register Map

The RTC and processor companion functions are accessed via 25 special function registers, which are mapped to a separate I^2C device ID. The interface protocol is described on page 19. The registers contain timekeeping data, control bits, and information flags. A description of each register follows the summary table.

Table 4. Register Map Summary Table

Nonvolatile = ☐ Battery-backed = ☐

Address	Data								Function	Range
	D7	D6	D5	D4	D3	D2	D1	D0		
18h	Serial Number Byte 7								Serial Number 7	FFh
17h	Serial Number Byte 6								Serial Number 6	FFh
16h	Serial Number Byte 5								Serial Number 5	FFh
15h	Serial Number Byte 4								Serial Number 4	FFh
14h	Serial Number Byte 3								Serial Number 3	FFh
13h	Serial Number Byte 2								Serial Number 2	FFh
12h	Serial Number Byte 1								Serial Number 1	FFh
11h	Serial Number Byte 0								Serial Number 0	FFh
10h	Counter 2 MSB								Event Counter 2 MSB	FFh
0Fh	Counter 2 LSB								Event Counter 2 LSB	FFh
0Eh	Counter 1 MSB								Event Counter 1 MSB	FFh
0Dh	Counter 1 LSB								Event Counter 1 LSB	FFh
0Ch					RC	CC	C2P	C1P	Event Count Control	
0Bh	SNL	-	FC	WP1	WP0	VBC	-	VTP	Companion Control	
0Ah	WDE	-	-	WDT4	WDT3	WDT2	WDT1	WDT0	Watchdog Control	
09h	WTR	POR	LB	-	WR3	WR2	WR1	WR0	Watchdog Restart/Flags	
08h	10 years				years				Years	00-99
07h	0	0	0	10 months	months				Month	01-12
06h	0	0	10 date		date				Date	01-31
05h	0	0	0	0	0	day			Day	01-07
04h	0	0	10 hours		hours				Hours	00-23
03h	0	10 minutes			minutes				Minutes	00-59
02h	0	10 seconds			seconds				Seconds	00-59
01h	$\overline{\text{OSCEN}}$	reserved	CALS	CAL4	CAL3	CAL2	CAL1	CAL0	CAL Control	
00h	reserved	CF	reserved	reserved	reserved	CAL	W	R	RTC Control	

Note When the device is first powered up and programmed, all timekeeping registers must be written because the battery-backed register values cannot be guaranteed. The table below shows the default values of the non-volatile registers. All other register values should be treated as unknown.

Table 5. Default Register Values

Address	Hex Value
18h	0x00
17h	0x00
16h	0x00
15h	0x00
14h	0x00
13h	0x00
12h	0x00
11h	0x00
0Bh	0x00

Address	Hex Value
0Ah	0x1F
08h	0x00
07h	0x01
06h	0x01
05h	0x01
04h	0x00
03h	0x01
02h	0x00
01h	0x80

Table 6. Register Description

Address	Description							
18h	**Serial Number Byte 7**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.63	SN.62	SN.61	SN.60	SN.59	SN.58	SN.57	SN.56
	Upper byte of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
17h	**Serial Number Byte 6**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.55	SN.54	SN.53	SN.52	SN.51	SN.50	SN.49	SN.48
16h	Byte 6 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
	Serial Number Byte 5							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.47	SN.46	SN.45	SN.44	SN.43	SN.42	SN.41	SN.40
	Byte 5 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
15h	**Serial Number Byte 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.39	SN.38	SN.37	SN.36	SN.35	SN.34	SN.33	SN.32
	Byte 4 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
14h	**Serial Number Byte 3**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.31	SN.30	SN.29	SN.28	SN.27	SN.26	SN.25	SN.24
	Byte 3 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
13h	**Serial Number Byte 2**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.23	SN.22	SN.21	SN.20	SN.19	SN.18	SN.17	SN.16
	Byte 2 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
12h	**Serial Number Byte 1**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.15	SN.14	SN.13	SN.12	SN.11	SN.10	SN.9	SN.8
	Byte 1 of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
11h	**Serial Number Byte 0**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SN.7	SN.6	SN.5	SN.4	SN.3	SN.2	SN.1	SN.0
	LSB of the serial number. Read/write when SNL = '0', read-only when SNL = '1'. Nonvolatile.							
10h	**Counter 2 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.15	C2.14	C2.13	C2.12	C2.11	C2.10	C2.9	C2.8
	Event Counter 2 MSB. Increments on overflows from Counter 2 LSB. Battery-backed, read/write.							

Table 6. Register Description (continued)

Address	Description							
0Fh	**Counter 2 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
	Event Counter 2 LSB. Increments on programmed edge event on CNT2 input or overflows from Counter 1 MSB when CC = '1'. Battery-backed, read/write.							
0Eh	**Counter 1 MSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.15	C1.14	C1.13	C1.12	C1.11	C1.10	C1.9	C1.8
	Event Counter 1MSB. Increments on overflows from Counter 1 LSB. Battery-backed, read/write.							
0Dh	**Counter 1 LSB**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
	Event Counter 1 LSB. Increments on programmed edge event on CNT1 input. Battery-backed, read/write.							
0Ch	**Event Counter Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	-	-	-	-	RC	CC	C2P	C1P
RC	Read Counter. Setting this bit to '1' takes a snapshot of the four counters bytes allowing the system to read the values without missing count events. The RC bit will be automatically cleared.							
CC	Counter Cascade. When CC = '0', the event counters operate independently according to the edge programmed by C1P and C2P respectively. When CC = '1', the counters are cascaded to create one 32-bit counter. The registers of Counter 2 represent the most significant 16-bits of the counter and CNT1 is the controlling input. Bit C2P is don't care when CC = '1'. Battery-backed, read/write.							
C2P	CNT2 detects falling edges when C2P = '0', rising edges when C2P = '1'. C2P is "don't care" when CC = '1'. The value of Event Counter 2 may inadvertently increment if C2P is changed. Battery-backed, read/write.							
C1P	CNT1 detects falling edges when C1P = '0', rising edges when C1P = '1'. The value of Event Counter 1 may inadvertently increment if C1P is changed. Battery-backed, read/write.							
0Bh	**Companion Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	SNL	-	FC	WP1	WP0	VBC	-	VTP
SNL	Serial Number Lock: Setting to a '1' makes registers 11h to 18h and SNL permanently read-only. SNL cannot be cleared once set to '1'. Nonvolatile, read/write.							
FC	Fast Charge: Setting FC to '1' (and VBC = '1') causes a ~1 mA trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.							
WP(1:0)	Write Protect. These bits control the write protection of the memory array. Nonvolatile, read/write.							
	Write protect address		WP1	WP0				
	None		0	0				
	Bottom 1/4		0	1				
	Bottom 1/2		1	0				
	Full array		1	1				
VBC	V_{BAK} Charger Control. Setting VBC to '1' (and FC = '0') causes a 80 µA (1 mA if FC = '1') trickle charge current to be supplied on V_{BAK}. Clearing VBC to '0' disables the charge current. Nonvolatile, read/write.							

Table 6. Register Description (continued)

Address	Description
VTP	VTP Select. This bit control the reset trip point for the low V_{DD} reset function. Nonvolatile, read/write. Trip Voltage — VTP 3.9 V — 0 4.4 V — 1
0Ah	**Watchdog Control**
	D7 | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** WDE | - | - | WDT4 | WDT3 | WDT2 | WDT1 | WDT0
WDE	Watchdog Enable. When WDE = '1', a watchdog timer fault will cause the $\overline{RST}$ signal to go active. When WDE = '0' the timer runs but has no effect on $\overline{RST}$, however the WTR flag will be set when a fault occurs. Note as the timer is free-running, users should restart the timer using WR(3:0) prior to setting WDE = '1'. This assures a full watchdog timeout interval occurs. Nonvolatile, read/write.
WDT(4:0)	Watchdog Timeout. Indicates the minimum watchdog timeout interval with 100 ms resolution. New watchdog timeouts are loaded when the timer is restarted by writing the 1010b pattern to WR(3:0). Nonvolatile, read/write. Watchdog Timeout — WDT4 — WDT3 — WDT2 — WDT1 — WDT0 Invalid - default 100 ms — 0 — 0 — 0 — 0 — 0 100 ms — 0 — 0 — 0 — 0 — 1 200 ms — 0 — 0 — 0 — 1 — 0 300 ms — 0 — 0 — 0 — 1 — 1 . . 2000 ms — 1 — 0 — 1 — 0 — 0 2100 ms — 1 — 0 — 1 — 0 — 1 2200 ms — 1 — 0 — 1 — 1 — 0 . . 2900 ms — 1 — 1 — 1 — 0 — 1 3000 ms — 1 — 1 — 1 — 1 — 0 Disable Counter — 1 — 1 — 1 — 1 — 1
09h	**Watchdog Restart and Flags**
	D7 | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** WTR | POR | LB | - | WR3 | WR2 | WR1 | WR0
WTR	Watchdog Timer Reset Flag: When a watchdog timer fault occurs, the WTR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
POR	Power-on Reset Flag: When the $\overline{RST}$ pin is activated by $V_{DD} < V_{TP}$, the POR bit will be set to '1'. It must be cleared by the user. Note that both WTR and POR could be set if both reset sources have occurred since the flags were cleared by the user. Battery-backed. Read/Write (internally set, user can clear bit).
LB	Low Backup Flag: On power up, if the V_{BAK} source is below the minimum voltage to operate the RTC and event counters, this bit will be set to '1'. The user should clear it to '0' when initializing the system. Battery-backed. Read/Write (internally set, user can clear bit).

Table 6. Register Description (continued)

Address	Description							
WR(3:0)	Watchdog Restart: Writing a pattern 1010b to WR(3:0) restarts the watchdog timer. The upper nibble contents do not affect this operation. Writing any pattern other than 1010b to WR(3:0) has no effect on the timer. This allows users to clear the WTR, POR, and LB flags without affecting the watchdog timer. Battery-backed, Write-only.							
08h	**Timekeeping – Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10 year.3	10 year.2	10 year.1	10 year.0	Year.3	Year.2	Year.1	Year.0
	Contains the lower two BCD digits of the year. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99. Battery-backed, read/write.							
07h	**Timekeeping – Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10 Month	Month.3	Month.2	Month.1	Month.0
	Contains the BCD digits for the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1-12. Battery-backed, read/write.							
06h	**Timekeeping – Date of the month**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 date.1	10 date.0	Date.3	Date.2	Date.1	Date.0
	Contains the BCD digits for the date of the month. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 3. The range for the register is 1-31. Battery-backed, read/write.							
05h	**Timekeeping – Day of the week**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day.2	Day.1	Day.0
	Lower nibble contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, as the day is not integrated with the date. Battery-backed, read/write.							
04h	**Timekeeping – Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10 hours.1	10 hours.0	Hours.3	Hours.2	Hours.1	Hours.0
	Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0-23. Battery-backed, read/write.							
03h	**Timekeeping – Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 min.2	10 min.1	10 min.0	Min.3	Min.2	Min.1	Min.0
	Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper minutes digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							

Table 6. Register Description (continued)

Address	Description							
02h	**Timekeeping - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10 sec.2	10 sec.1	10 sec.0	Seconds.3	Seconds.2	Seconds.1	Seconds.0
	Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0-59. Battery-backed, read/write.							
01h	**CAL/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	$\overline{\text{OSCEN}}$	Reserved	CALS	CAL.4	CAL.3	CAL.2	CAL.1	CAL.0
$\overline{\text{OSCEN}}$	Oscillator Enable. When set to ‘1’, the oscillator is halted. When set to ‘0’, the oscillator runs after t_{OSC} time. Disabling the oscillator can save battery power during storage. On a power-up without battery, this bit is set to ‘1’. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to ‘0’.							
CALS	Calibration Sign: Determines if the calibration adjustment is applied as an addition to or as a subtraction from the time-base. This bit can be written only when CAL = ‘1’. Nonvolatile, read/write.							
CAL(4:0)	Calibration Setting: These five bits control the calibration of the clock. These bits can be written only when CAL = ‘1’. Nonvolatile, read/write.							
00h	**RTC Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	Reserved	CF	Reserved	Reserved	Reserved	CAL	W	R
CF	Century Overflow Flag. This bit is set to a ‘1’ when the values in the years register overflows from 99 to 00. This indicates a new century, such as going from 1999 to 2000 or 2099 to 2100. The user should record the new century information as needed. This bit is cleared to ‘0’ when the Flag register is read. It is read-only for the user. Battery-backed.							
CAL	Calibration Setting. When set to ‘1’, the clock enters calibration mode. When CAL is set to ‘0’, the clock operates normally, and the CAL/PFO pin is controlled by the power fail comparator. Battery-backed, read/write.							
W	Write Time. Setting the W bit to ‘1’ freezes the clock. The user can then write the timekeeping registers with updated values. Resetting the W bit to ‘0’ causes the contents of the time registers to be transferred to the timekeeping counters and restarts the clock. Battery-backed, read/write.							
R	Read Time. Setting the R bit to ‘1’ copies a static image of the timekeeping core and place it into the user registers. The user can then read them without concerns over changing values causing system errors. The R bit going from ‘0’ to ‘1’ causes the timekeeping capture, so the bit must be returned to ‘0’ prior to reading again. Battery-backed, read/write.							
Reserved	Reserved bits. Do not use. Should remain set to ‘0’.							

I²C Interface

The FM31276/FM31278 employs an industry standard I²C bus that is familiar to many users. This product is unique since it incorporates two logical devices in one chip. Each logical device can be accessed individually. Although monolithic, it appears to the system software to be two separate products. One is a memory device. It has a Slave Address (Slave ID = 1010b) that operates the same as a stand-alone memory device. The second device is a real-time clock and processor companion which have a unique Slave Address (Slave ID = 1101b).

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM31276/FM31278 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 12 and Figure 13 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM31276/FM31278 should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM31276/FM31278 for a new operation.

If during operation the power supply drops below the specified V_{TP} minimum, any I²C transaction in progress will be aborted and the system should issue a START condition prior to performing another operation.

Figure 12. START and STOP Conditions

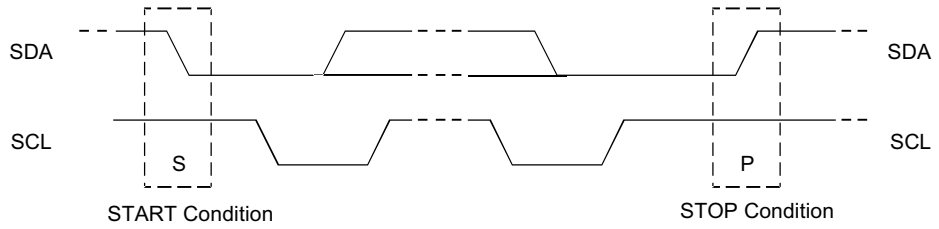
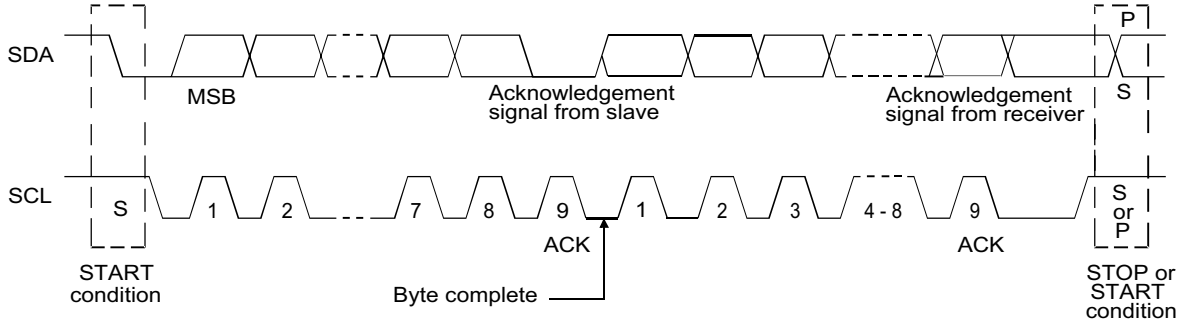


Figure 13. Data Transfer on the I²C Bus



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

Acknowledge / No-acknowledge

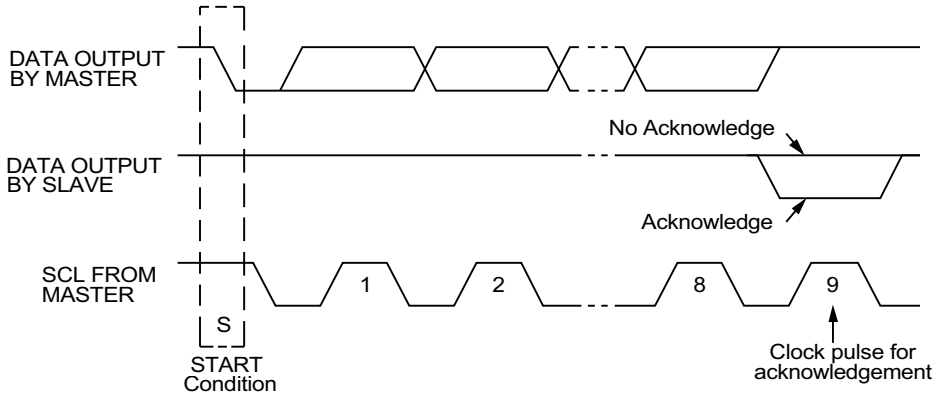
The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the device can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read

operation, the FM31276/FM31278 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM31276/FM31278 to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 14. Acknowledge on the I²C Bus



Slave Address

The first byte that the FM31276/FM31278 expects after a START condition is the slave address. As shown in Figure 15 and Figure 16, the slave address contains the device type or slave ID, the device select address bits, and a bit that specifies if the transaction is a read or a write.

The FM31276/FM31278 has two Slave Addresses (Slave IDs) associated with two logical devices. Bits 7-4 are the device type (slave ID) and should be set to 1010b for the memory device. The other logical device within the FM31276/FM31278 is the real-time clock and companion. Bits 7-4 are the device type (slave ID) and should be set to 1101b for the RTC and companion. A bus transaction with this slave address will not affect the memory in any way. The figures below illustrate the two Slave Addresses.

Bits 2-1 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to four FM31276/FM31278 devices can reside on the same I²C bus by assigning a different address to each. Bit 0 is the read/write bit (R/$\overline{W}$). R/$\overline{W}$ = '1' indicates a read operation and R/$\overline{W}$ = '0' indicates a write operation.

Figure 15. Memory Slave Device Address

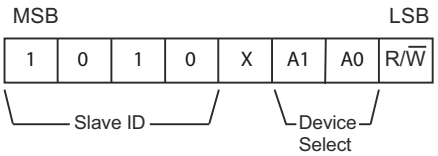
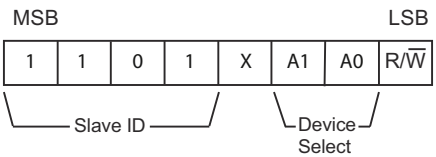


Figure 16. Companion Slave Device Address



Addressing Overview - Memory

After the FM31276/FM31278 (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires two bytes. The complete 15-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as $V_{DD} > V_{TP}$ or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM31276/FM31278 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (7FFFh) is reached, the address latch will roll over to 0000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Addressing Overview - RTC & Companion

The RTC and Processor Companion operate in a similar manner to the memory, except that it uses only one byte of address. Addresses 00h to 18h correspond to special function registers. Attempting to load addresses above 18h is an illegal condition; the FM31276/FM31278 will return a NACK and abort the I²C transaction.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM31276/FM31278 can begin. For a read operation the FM31276/FM31278 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM31276/FM31278 will transfer the next sequential byte. If the acknowledge is not sent, the FM31276/FM31278 will end the read operation. For a write

operation, the FM31276/FM31278 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM31276/FM31278 is designed to operate in a manner very similar to other I^2C interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM31276/FM31278 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

The memory address for FM31276 range from 0x0000 to 0x1FFFF, and for FM31278, they range from 0x0000 to 0x7FFF. Memory functionality is described with respect to FM31278 in the following sections.

Memory Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address (R/$\overline{W}$ bit) to a '0'. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 7FFFh to 0000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM31276/FM31278 uses no page buffering.

Figure 17 and Figure 18 below illustrate a single-byte and multiple-byte write cycles.

Figure 17. Single-Byte Write

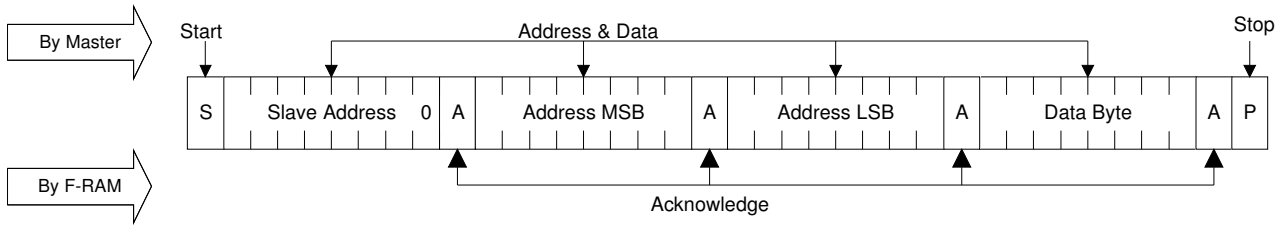
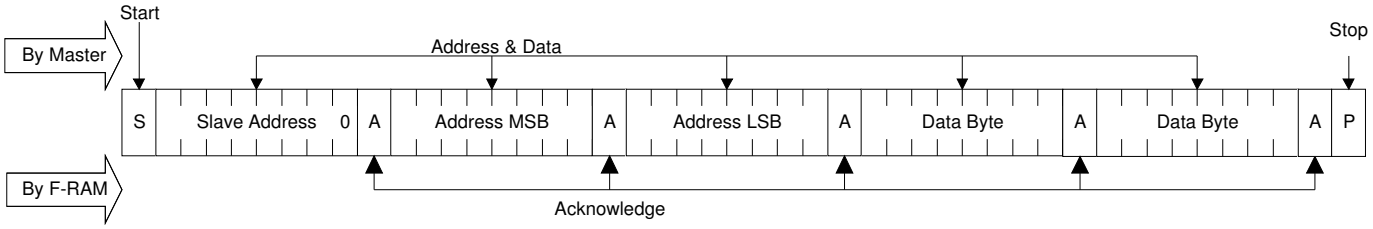


Figure 18. Multi-Byte Write



Memory Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM31276/FM31278 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM31276/FM31278 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM31276/FM31278 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current

address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM31276/FM31278 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM31276/FM31278 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 7FFFh, it will wrap around to 0000h on the next read cycle. Figure 19 and Figure 20 below show the proper operation for current address reads.

Figure 19. Current Address Read

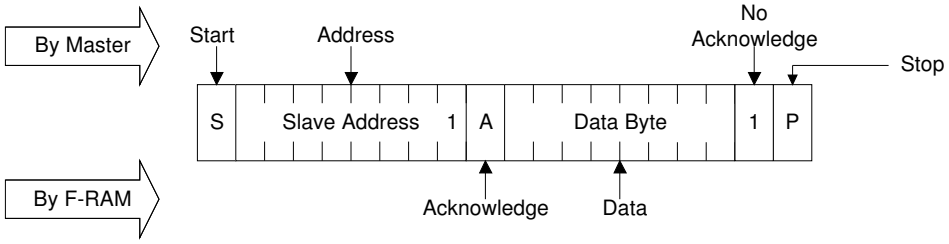
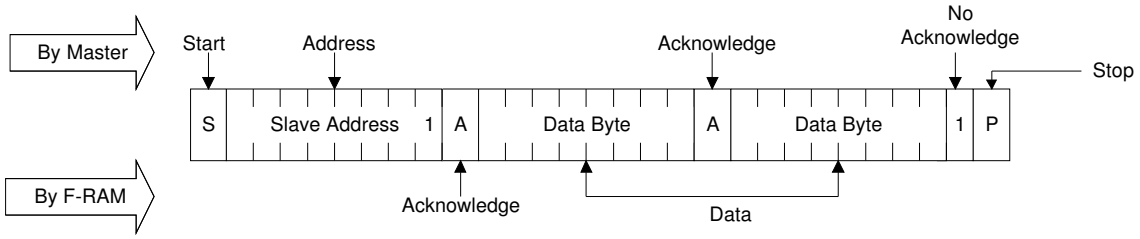


Figure 20. Sequential Read

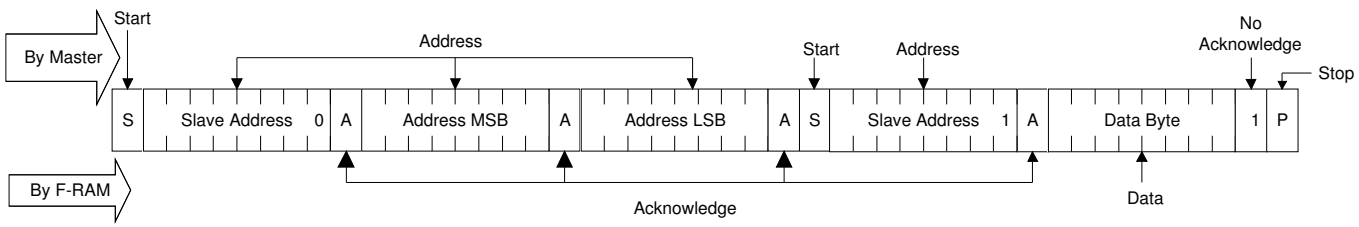


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB (R/$\overline{W}$) set to '0'. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM31276/FM31278 acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 21. Selective (Random) Read

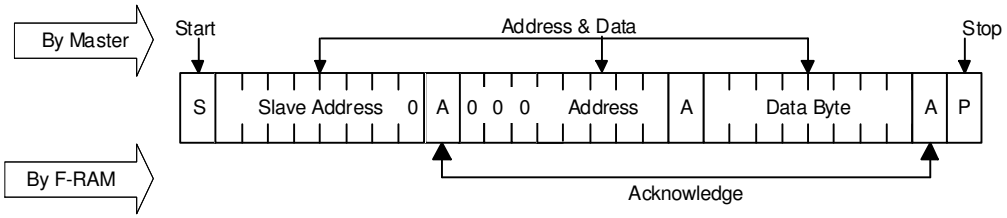


RTC/Companion Write Operation

All RTC and Companion writes operate in a similar manner to memory writes. The distinction is that a different device ID is used and only one byte address is needed instead of two byte address. Figure 22 illustrates a single byte write to this device.

Note Although not required, it is recommended that A5-A7 in the register address byte are zeros in order to preserve compatibility with future devices.

Figure 22. Single Byte Write



RTC/Companion Read Operation

As with writes, a read operation begins with the Slave Address. To perform a register read, the bus master supplies a Slave Address with the LSB set to '1'. This indicates that a read operation is requested. After receiving the complete Slave Address, the FM31276/FM31278 will begin shifting data out from the current register address on the next clock. Auto-increment operates for the special function registers as with the memory address. A current address read for the registers look exactly like the memory except that the device ID is different.

The FM31276/FM31278 contains two separate address registers, one for the memory address and the other for the register address. This allows the contents of one address register to be modified without affecting the current address of the other register. For example, this would allow an interrupted read to the memory while still providing fast access to an RTC register. A subsequent memory read will then continue from the memory address where it previously left off, without requiring the load of a new memory address. However, a write sequence always requires an address to be supplied.

Addressing FRAM Array in the FM31276/FM31278 Family

The FM31276/FM31278 family includes 64-Kbit and 256-Kbit memory densities. The following 2-byte address field is shown for each density.

Part Number	1st Address Byte								2nd Address Byte							
FM31276	X	X	X	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
FM31278	X	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –55 °C to +125 °C

Ambient Temperature

with power applied..... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} .....–1.0 V to +7.0 V

Input voltage ..... –1.0 V to +7.0 V and $V_{IN} < V_{DD} + 1.0$ V

Backup supply voltage.....–1.0 V to +4.5 V

DC voltage applied to outputs
in High-Z state .....–0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns) on
any pin to ground potential .....–2.0 V to V_{DD} + 2.0 V

Package power dissipation
capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering
temperature (3 seconds) ..... +260 °C

DC output current
(1 output at a time, 1s duration) ..... 15 mA

Electrostatic Discharge Voltage
Human Body Model (AEC-Q100-002 Rev. D) ..... 2 kV

Charged Device Model (AEC-Q100-011 Rev. B) ..... 1.25 kV

Machine Model (AEC-Q100-003 Rev. E) ..... 100 V

Latch-up current ..... > ±100 mA

Note PFI input voltage must not exceed 4.5 V. The "$V_{IN} < V_{DD}$+1.0 V" restriction does not apply to the SCL and SDA inputs which do not employ a diode to V_{DD}.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	4.0 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{DD}[2]	Power supply			4.0	–	5.5	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.3 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.3 V.	f_{SCL} = 100 kHz	–	–	500	µA
			f_{SCL} = 400 kHz	–	–	900	µA
			f_{SCL} = 1 MHz	–	–	1500	µA
I_{SB}	V_{DD} standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	–	150	µA
V_{BAK}[3]	RTC backup voltage		T_A = +25 °C to +85 °C	1.55	–	3.75	V
			T_A = –40 °C to +25 °C	1.90	–	3.75	V
I_{BAK}	RTC backup current	V_{BAK} = 3.0 V, V_{DD} < 2.4 V, oscillator running, CNT1, CNT2 at V_{BAK}.	T_A = +25 °C, V_{BAK} = 3.0 V	–	–	1.4	µA
			T_A = +85 °C, V_{BAK} = 3.0 V	–	–	2.1	µA
			T_A = +25 °C, V_{BAK} = 2.0 V	–	–	1.15	µA
			T_A = +85 °C, V_{BAK} = 2.0 V	–	–	1.75	µA
I_{BAKTC}[4]	Trickle charge current with V_{BAK} = 0 V		Fast Charge Off (FC = '0')	50	–	120	µA
			Fast Charge On (FC = '1')	200	–	2500	µA

Notes
1. Typical values are at 25 °C, $V_{DD} = V_{DD}$(typ). Not 100% tested.
2. Full complete operation. Supervisory circuits, RTC, etc operate to lower voltages as specified.
3. The V_{BAK} trickle charger automatically regulates the maximum voltage on this pin for capacitor backup applications.
4. V_{BAK} will source current when trickle charge is enabled (VBC bit = '1'), $V_{DD} > V_{BAK}$, and $V_{BAK} < V_{BAK}$ max.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{TP1}	V_{DD} trip point voltage, VTP = 0	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		3.75	3.90	4.00	V
V_{TP2}	V_{DD} trip point voltage, VTP = 1	$\overline{RST}$ is asserted active when $V_{DD} < V_{TP}$.		4.20	4.40	4.50	V
V_{RST}[5]	V_{DD} for valid $\overline{RST}$	I_{OL} = 80 µA at V_{OL}	$V_{BAK} > V_{BAK}$ min	0	–	–	V
			$V_{BAK} < V_{BAK}$ min	1.6	–	–	V
I_{LI}	Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$. Does not apply to A0, A1, X1, PFI, $\overline{RST}$, or X2		–	–	±1	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{OUT} \le V_{DD}$. Does not apply to $\overline{RST}$, X1, or X2		–	–	±1	µA
V_{IL}[6]	Input LOW voltage		All inputs except as listed below	– 0.3	–	0.3 × V_{DD}	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	– 0.3	–	0.5	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	– 0.3	–	0.8	V
V_{IH}	Input HIGH voltage		All inputs except as listed below	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			CNT1, CNT2 battery-backed (V_{DD} < 2.5 V)	V_{BAK} – 0.5	–	V_{BAK} + 0.3	V
			CNT1, CNT2 (V_{DD} > 2.5 V)	0.7 × V_{DD}	–	V_{DD} + 0.3	V
			PFI (comparator input)	–	–	3.75	V
V_{OH}	Output HIGH voltage	I_{OH} = –2 mA		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		–	–	0.4	V
R_{RST}	Pull-up resistance for $\overline{RST}$ inactive			50	–	400	kΩ
R_{in}	Input resistance (A1-A0)	For $V_{IN} = V_{IL}(Max_)$		20	–	–	kΩ
		For $V_{IN} = V_{IH}$(Min)		1	–	–	MΩ
V_{PFI}	Power fail input reference voltage			1.140	1.20	1.225	V
V_{HYS}	Power fail input (PFI) hysteresis (rising)			–	–	100	mV

Notes
5. The minimum V_{DD} to guarantee the level of $\overline{RST}$ remains a valid V_{OL} level.
6. Includes $\overline{RST}$ input detection of external reset condition to trigger driving of $\overline{RST}$ signal by FM31276/FM31278.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

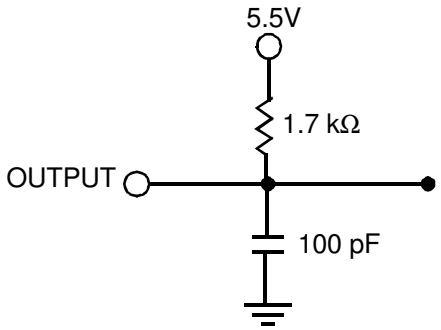
Parameter [7]	Description	Test Conditions	Typ	Max	Unit
C_{IO}	Input/Output pin capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	–	8	pF
C_{XTL} [8]	X1, X2 crystal pin capacitance		12	–	pF

Thermal Resistance

Parameter	Description	Test Conditions	14-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	80	°C/W
Θ_{JC}	Thermal resistance (junction to case)		29	°C/W

AC Test Loads and Waveforms

Figure 23. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels .....10% and 90% of V_{DD}
Input rise and fall times .....10 ns
Input and output timing reference levels .....0.5 × V_{DD}
Output load capacitance ..... 100 pF

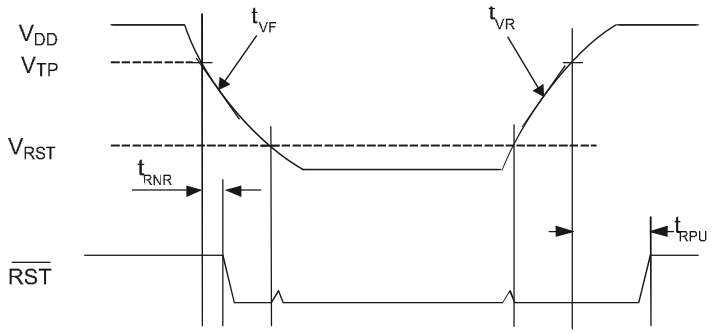
Notes
7. This parameter is characterized and not 100% tested.
8. The crystal attached to the X1/X2 pins must be rated as 6 pF/12.5 pF.

Supervisor Timing

Over the Operating Range

Parameter	Description	Min	Max	Units
t_{RPU}	$\overline{RST}$ active (LOW) after $V_{DD} > V_{TP}$	100	200	ms
t_{RNR}[9]	$\overline{RST}$ response time to $V_{DD} < V_{TP}$ (noise filter)	10	25	µs
t_{VR}[9, 10]	V_{DD} power-up ramp rate	50	-	µs/V
t_{VF}[9, 10]	V_{DD} power-down ramp rate	100	-	µs/V
t_{WDP}[11]	Pulse width of $\overline{RST}$ for watchdog reset	100	200	ms
t_{WDOG}[11]	Timeout of watchdog	t_{DOG}	$2 \times t_{DOG}$	ms
f_{CNT}	Frequency of event counters	0	10	MHz
t_{OSC}	RTC Oscillator time to start	-	2	s

Figure 24. $\overline{RST}$ Timing



Notes
9. This parameter is characterized and not 100% tested.
10. Slope measured at any point on V_{DD} waveform.
11. t_{DOG} is the programmed time in register in register 0Ah, $V_{DD} > V_{TP}$, and t_{RPU} satisfied.

AC Switching Characteristics

Over the Operating Range

Parameter[12]	Alt. Parameter	Description	Min	Max	Min	Max	Min	Max	Unit
f_{SCL}		SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{SU;STA}$		Start condition setup for repeated Start	4.7	–	0.6	–	0.25	–	µs
$t_{HD;STA}$		Start condition hold time	4.0	–	0.6	–	0.25	–	µs
t_{LOW}		Clock LOW period	4.7	–	1.3	–	0.6	–	µs
t_{HIGH}		Clock HIGH period	4.0	–	0.6	–	0.4	–	µs
$t_{SU;DAT}$	$t_{SU;DATA}$	Data in setup	250	–	100	–	100	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	–	0	–	ns
t_{DH}		Data output hold (from SCL @ V_{IL})	0	–	0	–	0	–	ns
t_R[13]	t_r	Input rise time	–	1000	–	300	–	300	ns
t_F[13]	t_f	Input fall time	–	300	–	300	–	100	ns
$t_{SU;STO}$		STOP condition setup	4	–	0.6		0.25	–	µs
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	3		0.9	–	0.55	µs
t_{BUF}		Bus free before new transmission	4.7	–	1.3	–	0.5	–	µs
t_{SP}		Noise suppression time constant on SCL, SDA	–	50		50	–	50	ns

Figure 25. Read Bus Timing Diagram

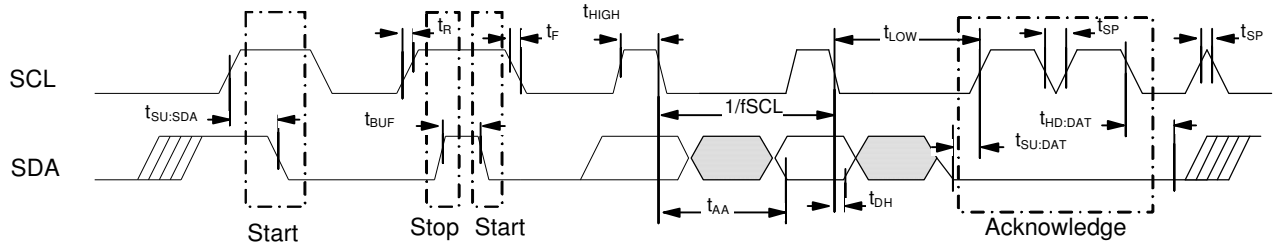
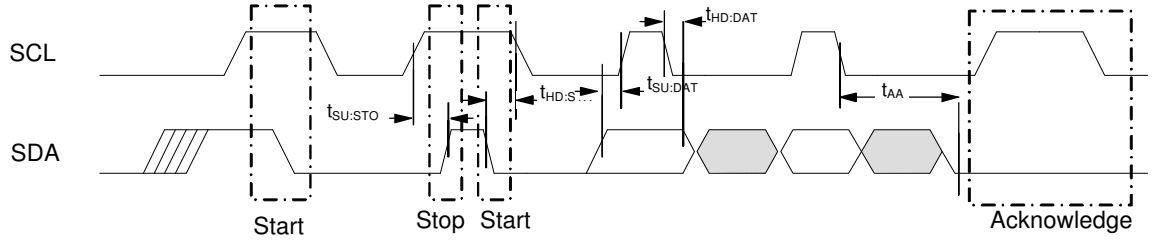


Figure 26. Write Bus Timing Diagram



Notes

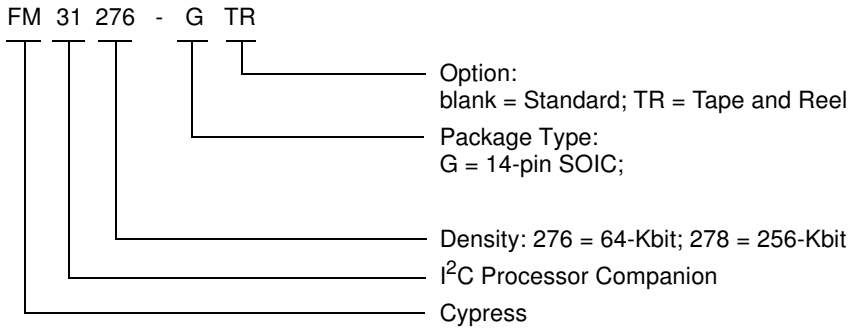
12. Test conditions assume a signal transition time of 10 ns or less, timing reference levels of 0.5 × V_{DD}, input pulse levels of 10% to 90% of V_{DD}, and output loading of the specified I_{OL}/I_{OH} and 100 pF load capacitance shown in page 26.
13. This parameter is characterized and not 100% tested.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM31276-G	51-85067	14-pin SOIC	Industrial
FM31276-GTR	51-85067	14-pin SOIC	
FM31278-G	51-85067	14-pin SOIC	
FM31278-GTR	51-85067	14-pin SOIC	

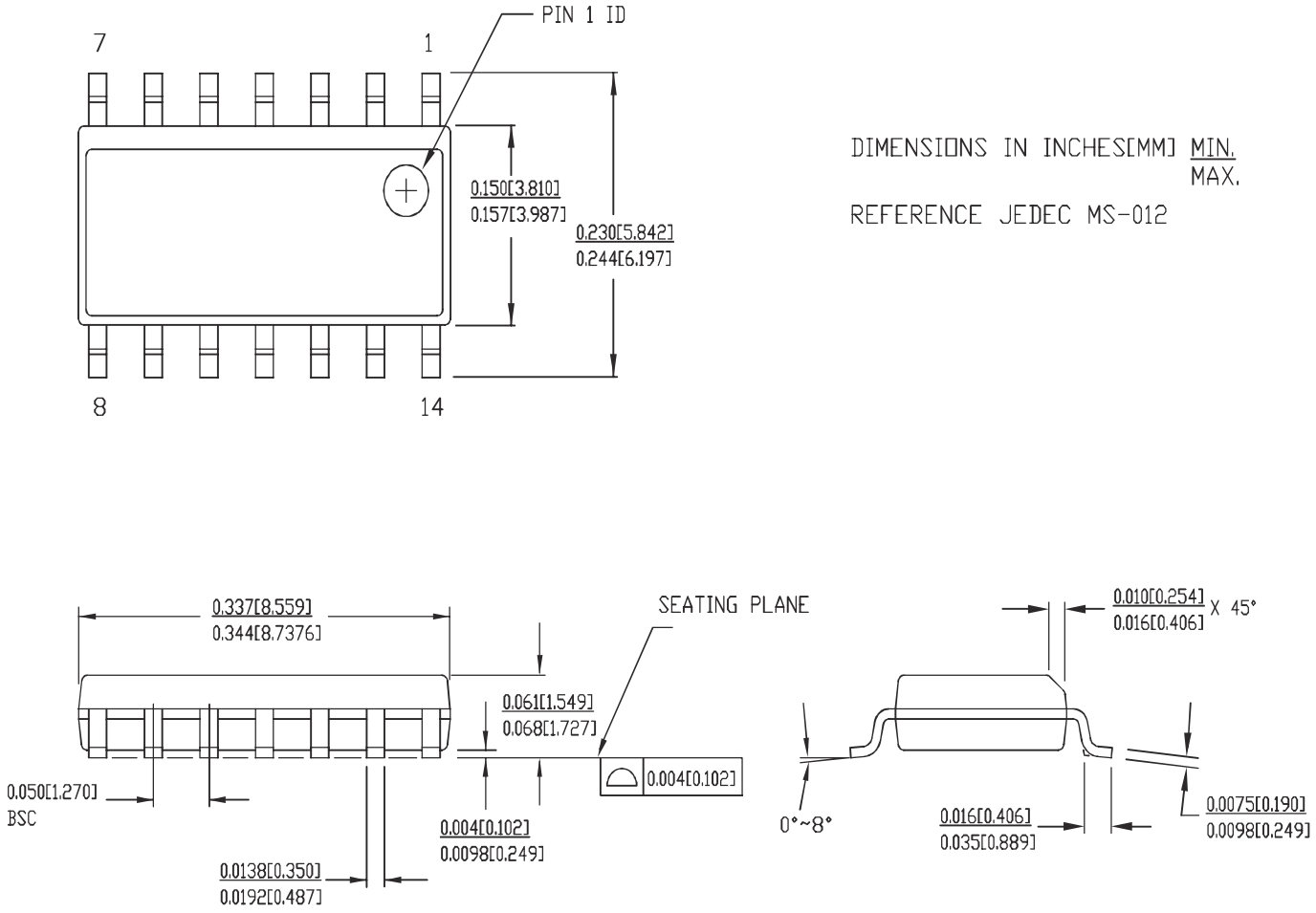
All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 27. 14-pin SOIC (150 Mils) Package Outline, 51-85067



51-85067 *D

Acronyms

Acronym	Description
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIA	Electronic Industries Alliance
F-RAM	Ferroelectric Random Access Memory
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
JESD	JEDEC Standards
LSB	Least Significant Bit
MSB	Most Significant Bit
NMI	Non Maskable interrupt
RoHS	Restriction of Hazardous Substances
SOIC	Small Outline Integrated Circuit

Document Conventions

Units of Measure

Symbol	Unit of Measure
℃	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
Mbit	megabit
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: FM31276/FM31278, 64-Kbit/256-Kbit Integrated Processor Companion with F-RAM Document Number: 001-86393				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3916896	GVCH	02/28/2013	New spec
*A	3924836	GVCH	03/07/2013	Modified formatting Deleted 4 Kb and 8 Kb versions Changed to production status
*B	3985209	GVCH	05/02/2013	Changed following values VTP1 Min value from 3.80 V to 3.75 V VTP2 Min value from 4.25 V to 4.20 V VPFI Minvalue from 1.175 V to 1.140 V
*C	4333096	GVCH	05/05/2014	Converted to Cypress standard format Crystal Oscillator: Added use of 6 pF crystal Updated Maximum Ratings table - Removed Moisture Sensitivity Level (MSL) - Added junction temperature and latch up current Updated Data Retention and Endurance table Changed C_{XTL} parameter typ value from 25 pF to 12 pF. Added Thermal Resistance table Removed Package Marking Scheme (top mark)
*D	4562106	GVCH	11/05/2014	Added related documentation hyperlink in page 1.
*E		GVCH	02/13/2018	Register Map - Table 4: Removed VTP1 bit from bit 1 and renamed VTP0 to VTP in the bit 0 of the 0Bh register Table 6: Removed VTP1 bit from bit 1 and renamed VTP0 to VTP in the bit 0 of the 0Bh register Table 6: $\overline{\text{OSCEN}}$ bit description is updated to add t_{OSC} time in the 01h register DC Electrical Characteristics: V_{TP2} typical voltage is changed from 4.00V to 4.40V Supervisor Timing: Added t_{OSC} parameter spec

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4	FM31256-G1TR
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6	FM31276-GTR
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8	FM31278-GTR
9	FM3164-G
10	FM3164-GTR
11	FM31L276-G
12	FM31L276-GTR
13	FM31L278-G
14	FM31L278-GTR