Cypress Semiconductor Corporation, 198 Champion Court, San Jose, CA 95134. Tel: (408) 943-2600

PRODUCT CHANGE NOTIFICATION

PCN: PCN170501A **Date:** December 21, 2017

Subject: Addendum to PCN 170501: Qualification of Texas Instruments' DMOS6 as an Additional Wafer Fab Site and Test 25 as an Additional Wafer Sort Site for 2Mb F-RAM Serial Product Family

To: PHILIP MAILLET
FUTURE
pcn.system2@future.ca

Change Type: Major

Description of Change:
The purpose of this addendum is to add parts to the parts list that were not included in the original PCN. The added part numbers can be identified in the affected parts list with PCN170501A in column D.

Cypress announced the qualification of Texas Instruments' DMOS6 as an additional wafer fab site and Test 25 as an additional wafer sort site for its 2Mb F-RAM Serial Product Family. This qualification is part of the flexible manufacturing initiative which allows Cypress to meet its delivery commitments in dynamic, changing market conditions.

Benefit of Change:
Qualification of alternate manufacturing sites is part of the ongoing flexible manufacturing initiative announced by Cypress. The goal of the flexible manufacturing initiative is to provide the means for Cypress to continue to meet delivery commitments through dynamic, changing market conditions.

Part Numbers Affected: 13
See the attached 'Affected Parts List' file for a list of all part numbers affected by this change. Note that any new parts that are introduced after the publication of this PCN will include all changes outlined in this PCN. This addendum adds parts with PCN170501A in column D.

Qualification Status:
This wafer fab site has been qualified through a series of tests documented in the Qualification Test Plan (QTP) Report #143905. The new wafer sort site has been qualified through a series of tests documented in the Qualification Test Plan (QTP) Report # 170503. This qualification report can be found as an attachment to this PCN or by visiting www.cypress.com and typing the QTP number in the keyword search window.

Sample Status:
Qualification samples may not be built ahead of time for all part numbers affected by this change. Please review the attached 'Affected Parts List' file for a list of affected part numbers with their associated DMOS6 sample ordering part numbers. Samples are available now unless there is an indication that the sample ordering part numbers are subject to lead times. If you require qualification samples, please contact your local Cypress sales representative as soon as possible, preferably within 30 days of the date of this PCN, to place any sample orders.

Approximate Implementation Date:
Note that the original part numbers in PCN170501 may already be fabricated at DMOS6 and sorted at Test 25. Effective 90 days from the date of this notification or upon customer approval, whichever comes first, all shipments of the added part numbers in the attached file may be supplied from any of the qualified manufacturing sites.

Anticipated Impact:
Products fabricated at DMOS6 and sorted at Test 25 are completely compatible with existing product from a form, fit, functional, parametric and quality performance perspective.

Cypress also recommends that customers take this opportunity to review these changes against current application notes, system design considerations and customer environment conditions to assess impact (if any) to their application.

Method of Identification:
Cypress maintains traceability of product to wafer level, including wafer fabrication location, through the lot number marked on the package.

Response Required:
No response is required.

For additional information regarding this change, contact your local sales representative or contact the PCN Administrator at pcn_adm@cypress.com.

Sincerely,

Cypress PCN Administration

Cypress Semiconductor
Sort Site Qualification Report

QTP#170503 VERSION *D
June 2017

Cypress Test 25, Austin, Texas Sort Site Qualification for F-RAM Devices
F-RAM Devices

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com or via a CYLINK CRM CASE

Prepared By:
Su Zheng
Reliability Engineer

Reviewed By:
Yusaku Ohta
Reliability Manager

Approved By:
David Hoffman
Reliability Director

PACKAGE/PRODUCT QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date
170503	Cypress Test 25, Austin, Texas Sort Site Qualification for F-RAM Device	February 2017

QUALIFICATION COVERAGE RANGE

MARKETING PART NUMBER	PACKAGE
FM16*	8L-SOIC
FM18*	8L-SOIC / 8L-PDIP
FM21*	44L-TSOP
FM22*	44L-TSOP / 48L-BGA
FM24*	8L-SOIC / 8L-DFN
FM25*	8L-SOIC / 8L-DFN / 8L-PDIP
FM28*	8L-SOIC / 28L-TSOP/ 32L-TSOP
FM31*	14L-SOIC
FM33*	14L-SOIC
CY15*	8L-SOIC / 8L-DFN / 8L-PDIP

Reliability Test Data

QTP #: 170503

Device	Fab Lot#	Assy Lot#	Test- Loc	Yield
SORT TEST: CORRELATION				
Sort 1 Yield				
TR20011ACY	2539013 W5, W9, W12	N/A	KYEC-TEST25	Correlated
Sort 2 Yield				
TR20011ACY	2539013 W5, W9, W12	N/A	KYEC-TEST25	Correlated
Sort 1 Bin Movement				
TR20011ACY	2603007 W9	N/A	KYEC-TEST25	0.47% Passed
TR20011ACY	2539013 W9	N/A	KYEC-TEST25	0.35% Passed
Sort 2 Bin Movement				
TR20011ACY	2603007 W9	N/A	KYEC-TEST25	0.92% Passed
TR20011ACY	2539013 W9	N/A	KYEC-TEST25	0.52% Passed
Fishers Exact				
TR20011ACY	2539013 W5, W9, W12	N/A	KYEC-TEST25	> 0.05
Bin Split Yield				
TR20011ACY	3646046 W5, W9, W12	N/A	KYEC-TEST25	Passed
Site to Site Verification				
TR20011ACY	3646046	N/A	KYEC-TEST25	Passed

See below for an explanation of the terms used above.

Sort is the process of electrically testing the die on a wafer after fabrication is complete. Sort test flows vary by product and technology. Sort can be a single test step, or include multiple test steps at different temperatures, data bake, UV erase or other steps.

Sort 1 is the first sort test insertion, Sort 2 is the second sort test insertion, etc. Sort 1 and Sort 2 will typically be done at different temperatures and possibly with different test parameters. Both sort steps use the same reference wafer-map and the rejected die from Sort 1 are not subject to Sort 2. The quantity-out of Sort 1 is the quantity-in for Sort 2.

Yield is the ratio of good/working die on a wafer to the total number of die on a wafer.

Sort 1 Yield and **Sort 2 Yield** refer to the percent of die on a processed wafer that pass all functional and technical requirements necessary for customer shipment during Sort 1 and Sort 2.
Sort yield comparison between repeated sort insertions for the same wafer are considered correlated if die get binned into the same bins consistently.

Binning allows die to be put into different groups depending on their test results. Each die is assigned a bin based on its performance or failure mode.

Bin Movement measures the percentage of die which are put into different bins between repeated sort insertions (i.e. Sort 1 to a repeated Sort 1). Bin movement <2% is required for passing qualification to ensure consistency in sort results.

Fishers Exact test is a statistical test used to compare proportions of two nominal variables, to check if they are statistically significant. Sort Yield Comparison using Fisher Exact Test should meet F value >=0.05.

Site to Site Verification insures consistent results across all test sites for products which include multiple die tested simultaneously. In this context, “test site” refers to one of the die which are tested simultaneously during a single touch down.

Document History Page

Document Title: QTP#170503: CYPRESS TEST 25, AUSTIN, TEXAS SORT SITE QUALIFICATION F-RAM DEVICES
Document Number: 002-18687

Rev.	ECN No.	Orig. of Change	Description of Change
**	5624001	SUZH	Initial Release.
*A	5633500	SUZH	Updated the parts list.
*B	5723685	HSTO	Updated Cypress logo Updated the parts list
*C	5747295	EKNG	Updated additional Qualification data
*D	5767156	EKNG SANC	Updated Sort 1 and 2 Bin Movement Value Added definition of technical terms

Cypress Semiconductor Corporation
2-Mbit/1-Mbit Parallel (PAR)/Serial (SPI) F-RAM Characterization Report

Design Engineering Director or Manager
David Still
dstl@cypress.com

Product Engineering Director
Jesse Siman
zsj@cypress.com

Product Engineer
Justin Beavers
jbev@cypress.com

Applications Engineer
Shivendra Singh
zsk@cypress.com

Marketing Engineer
Pramodh Prakash
tup@cypress.com

www.cypress.com

198 Champion Ct.
San Jose, CA 95134 USA

Tel: (408) 943 2600
Fax: (408) 943 4730

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2.0 Introduction

2.1 General Description

2-Mbit Serial (SPI) F-RAM

The 2-Mbit Serial (SPI) F-RAM is a nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead and system-level reliability problems caused by serial flash, EEPROM, and other nonvolatile memories.

Unlike serial flash and EEPROM, the 2-Mbit Serial (SPI) F-RAM performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. The 2-Mbit Serial (SPI) F-RAM is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

These capabilities make the 2-Mbit Serial (SPI) F-RAM ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of serial flash or EEPROM can cause data loss. The 2-Mbit Serial (SPI) F-RAM provides substantial benefits to users of serial EEPROM or flash as a hardware drop-in replacement. The 2-Mbit Serial (SPI) F-RAM uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The device incorporates a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision.

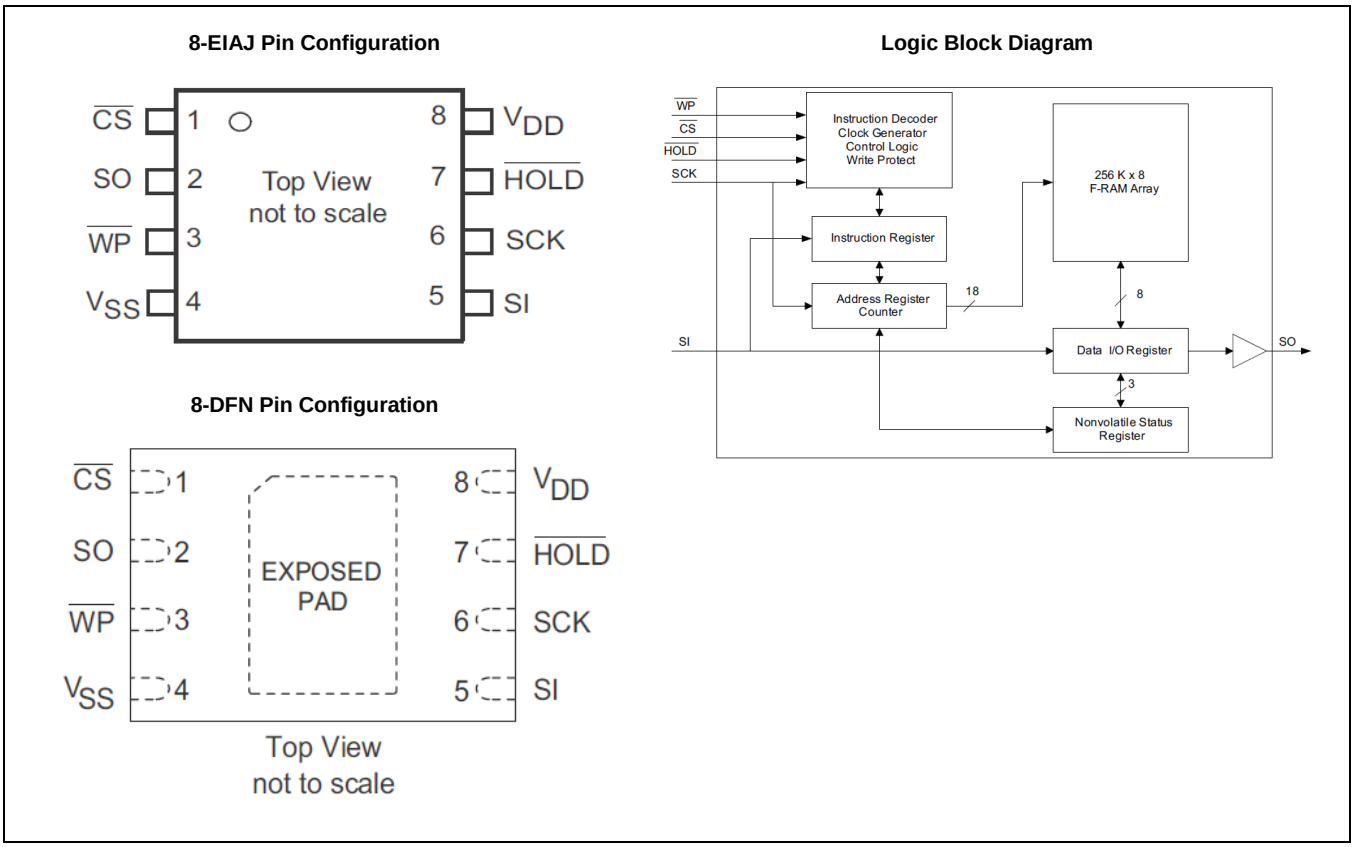

Figure 1. 2-Mbit Serial (SPI) F-RAM Pin Configuration and Logic Block Diagram

2-Mbit/1-Mbit Parallel (PAR) F-RAM

The 2-Mbit/1-Mbit Parallel (Par) F-RAM is a nonvolatile memory that reads and writes similar to a standard SRAM. A ferroelectric random access memory or F-RAM is nonvolatile, which means that data is retained after power is removed. It provides data retention for over 151 years while eliminating the reliability concerns, functional disadvantages, and system design complexities of battery-backed SRAM (BBSRAM). Fast write timing and high write endurance make the F-RAM superior to other types of memory.

The 2-Mbit/1-Mbit Parallel (PAR) F-RAM operation is similar to that of other RAM devices and therefore, it can be used as a drop-in replacement for a standard SRAM in a system. Read cycles may be triggered by CE or simply by changing the address and write cycles may be triggered by CE or WE. The F-RAM memory is nonvolatile due to its unique ferroelectric memory process. These features make the 2-Mbit/1-Mbit Parallel (PAR) F-RAM ideal for nonvolatile memory applications requiring frequent or rapid writes.

The device is available in a 400-mil, 44-pin TSOP-II surface mount package.

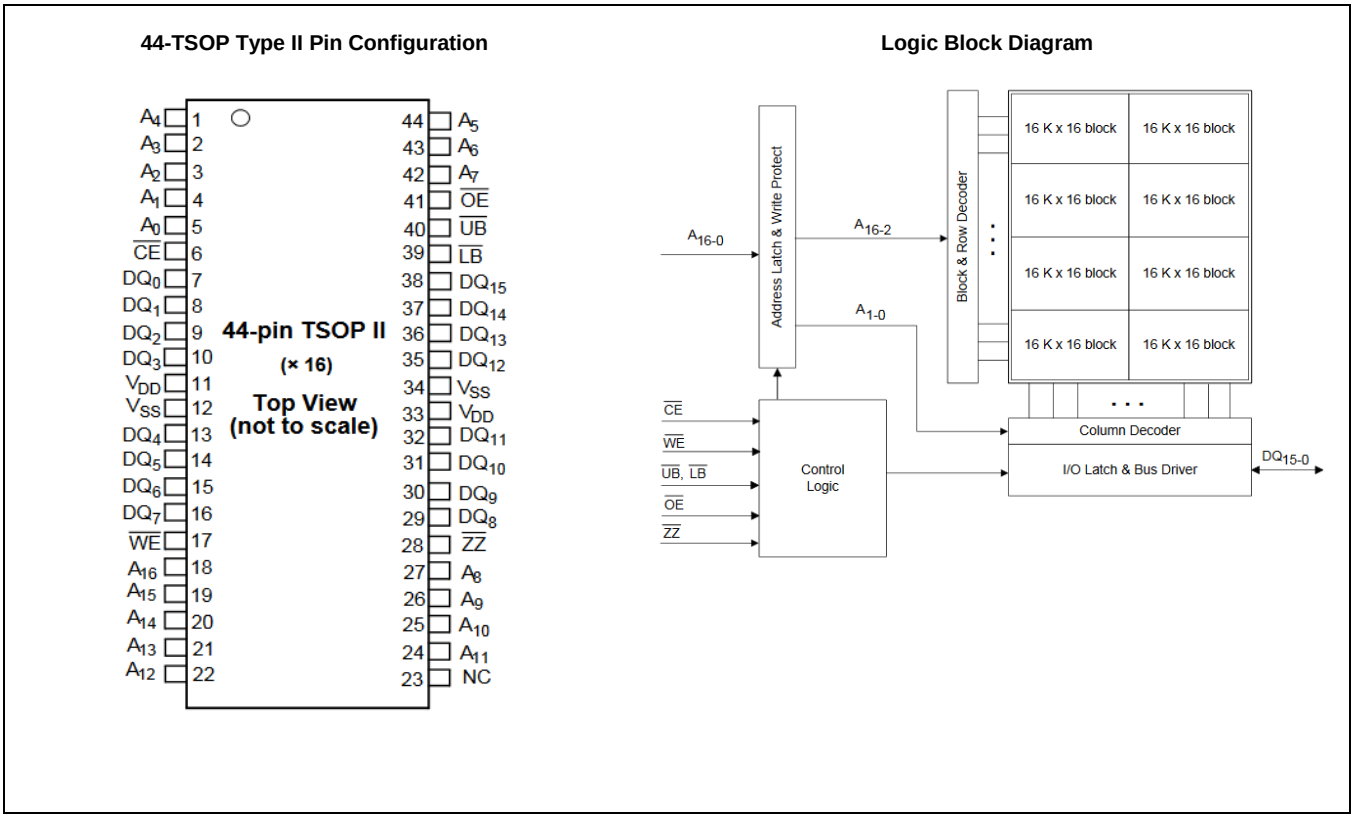

Figure 2. 2-Mbit/1-Mbit Parallel (PAR) Pin Configuration and Logic Block Diagram

2.2 Datasheet

The 2-Mbit/1-Mbit Parallel (PAR)/Serial (SPI) F-RAM meets all datasheet specifications.

Industrial datasheets are available from the Cypress Website at:

Option	Device	Datasheet
Industrial (-40°C to 85°C)	FM25V20A	http://www.cypress.com/file/141396/download
	FM28V102A	http://www.cypress.com/file/140901/download
	FM28V202A	http://www.cypress.com/file/136441/download

Automotive datasheets are available from the Cypress Website at:

Option	Device	Datasheet
Automotive-A (-40°C to 85°C)	CY15B102Q-SXA	http://www.cypress.com (Specific webpage URL is TBD)
	CY15B101N-SXA	http://www.cypress.com/file/175761/download
	CY15B102N-SXA	http://www.cypress.com/file/175756/download
Automotive-E (-40°C to 125°C)	CY15B102Q-SXE	http://www.cypress.com/file/175731/download
	CY15B101N-SXE	http://www.cypress.com (Specific webpage URL is TBD)
	CY15B102N-SXE	http://www.cypress.com (Specific webpage URL is TBD)

2.3 Application Notes

Please refer to the following Application Notes on the Cypress Website.

SPI Guide for F-RAM – http://www.cypress.com/?rID=82691

2.4 White Papers

The following F-RAM specific White Papers are available on the Cypress Website:

F-RAM™, nvSRAM, and MRAM Magnetic Field Immunity - http://www.cypress.com/file/46731/download

Energy Comparison of Cypress F-RAM and EEPROM - http://www.cypress.com/file/46746/download

Enhanced Endurance Performance of 0.13 um Nonvolatile F-RAM Products - http://www.cypress.com/file/46181/download

F-RAM Technology Brief - http://www.cypress.com/file/46186/download

2.5 Qualification Report

The 2-Mbit/1-Mbit Parallel (PAR)/Serial (SPI) F-RAM Industrial and automotive devices were qualified under QTP 143905 and 154910, respectively. The qualification reports are available from the Cypress Website at:

http://www.cypress.com (Specific webpage URL is TBD).

3.0 Characterization Hardware and Setup

AC and DC parameters were characterized on Nextest Magnum 1 tester. Characterization was performed using 8-pin EIAJ and 44-pin TSOP-II hand test boards along with the general purpose Nextest load board. The capacitance and inductance introduced by the package and the char board have an insignificant impact on these DC and AC parameters. All units were tested across datasheet V_{DD} values of 2.0V to 3.6V in addition to a +/-100 mV guardband. The data recorded in the tables below are for datasheet V_{DD} values only.

A Thermonics Precision Temperature Forcing System was used to force the temperature ranges of -40°C to 85°C for Industrial and Automotive-A grade parts and -40°C to 125°C for Automotive-E grade parts. A temperature guard band of +/-5°C was used. Characterization was performed across datasheet temperature and voltage range plus guardbands to ensure that all parameters have enough margin to spec and meet the required yield criteria for mass production. Char samples were assembled in an 8-pin EIAJ package for Serial (SPI) and in a 44-pin TSOP-II package for Parallel (PAR).

4.0 SPI Characterization

4.1 SPI Industrial / Automotive-A Characterization Summary over V_{DD} and Temperature

4.1.1 DC Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage	2	3.6	-	-	-	-	V
I_{DD}	V_{DD} Supply Current (f_{SCK} = 1 MHz)	-	300	160	228	98.75	196.3	µA
	V_{DD} Supply Current (f_{SCK} = 40 MHz)	-	3000	1153	1384	1323	1519	µA
I_{SB}	V_{DD} standby current (T_A = 25°C)	-	150	65.57	92.32	62.12	97.25	µA
I_{SB}	V_{DD} standby current (T_A = 85°C)	-	250	123.5	171.938	83.13	145.9	µA
I_{ZZ}	Sleep mode current (T_A = 25°C)	-	5	2.432	3.21	1.17	3.07	µA
I_{ZZ}	Sleep mode current (T_A = 85°C)	-	8	3.176	3.619	1.65	4.6	µA
I_{LI}	Input leakage current	-1	1	0.003	0.003	-0.04	0.44	µA
I_{LO}	Output leakage current (SO)	-1	1	0.023	0.016	-0.04	0.42	µA
V_{IH}	Input HIGH Voltage (V_{DD} = 2.0V)	1.4	-	1.15	1.18	1.04	1.26	V
V_{IH}	Input HIGH Voltage (V_{DD} = 3.0V)	2.1	-	1.46	1.74	1.52	1.78	V
V_{IH}	Input HIGH Voltage (V_{DD} = 3.6V)	2.52	-	1.7	2.02	1.54	1.9	V
V_{IL}	Input HIGH Voltage (V_{DD} = 2.0V)	-	0.6	0.7	0.92	0.72	0.96	V
V_{IL}	Input HIGH Voltage (V_{DD} = 3.0V)	-	0.9	1	1.24	1.08	1.3	V
V_{IL}	Input HIGH Voltage (V_{DD} = 3.6V)	-	1.08	1.35	1.42	1.16	1.38	V
V_{OH1}	Output HIGH Voltage (I_{OH} = -1 mA, V_{DD} = 2.7V)	2.4	-	2.921	2.945	2.6	2.63	V
V_{OH2}	Output HIGH Voltage (I_{OH} = -100 µA, V_{DD} = 2.0V)	V_{DD} - 0.2	-	1.99	1.993	1.88	1.92	V
V_{OL1}	Output LOW Voltage (I_{OL} = 2 mA, V_{DD} = 2.7V)	-	0.4	0.086	0.131	0.11	0.17	V
V_{OL2}	Output LOW Voltage (I_{OL} = 150 µA)	-	0.2	0.007	0.011	0.100	0.180	V

Table 1. DC Characterization Results

4.1.2 AC Characterization

Parameter	Description	Datasheet V_{DD} = 2.0 to 2.7V		Datasheet V_{DD} = 2.7 to 3.6V		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{SCK}	SCK clock frequency	0	25	0	40	43.68	47.67	43.27	47.67	MHz
t_{CH}	Clock HIGH time	18	-	11	-	4.70	6.10	4.60	6.60	ns
t_{CL}	Clock LOW time	18	-	11	-	4.90	60	5.50	6.30	ns
t_{CSU}	Chip select setup	12	-	10	-	-0.20	0.90	0.50	1.30	ns
t_{CSH}	Chip select hold	12	-	10	-	-20.40	-19.60	-20.30	-20.10	ns
t_{ODV}	Output data valid time	-	16	-	9	2.40	6.10	3.50	7.90	ns
t_{OH}	Output hold time	0	-	0	-	1.60	3.20	2.10	4.50	ns
t_D	Deselect time	60	-	40	-	2.10	3.10	2.10	2.10	ns
t_{SU}	Data setup time	8	-	5	-	0.40	1.60	1.00	1.70	ns
t_H	Data hold time	8	-	5	-	-0.30	0.60	0.10	0.40	ns
t_{HS}	/HOLD setup time	12	-	10	-	-20.60	-19.20	-20.00	-19.60	ns
t_{HH}	/HOLD hold time	12	-	10	-	0.20	1.20	0.40	1.10	ns

Table 2. AC Characterization Results

4.1.3 Power Cycle Timing Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
t_{PU}	Power-up V_{DD}(min) to first access (/CS LOW)	1	-	0.23	0.34	0.22	0.35	ms
t_{REC}	Recovery time from sleep mode	-	450	315.86	401.43	299.00	389.00	µs

Table 3. Power Cycle Timing Characterization Results

4.2 SPI Automotive-E Characterization Summary over V_{DD} and Temperature

4.2.1 DC Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage	2.0	3.6	-	-	-	-	V
I_{DD}	V_{DD} Supply Current (f_{SCK} = 25 MHz)	-	5000	840.0	1150	912.5	1226	µA
I_{SB}	V_{DD} standby current (T_A = 25°C)	-	150	65.25	113.00	62.12	97.25	µA
	V_{DD} standby current (T_A = 125°C)	-	750	120.1	268.0	110.7	275.1	µA
I_{ZZ}	Sleep mode current (T_A = 25°C)	-	5	1.50	3.73	1.17	3.07	µA
	Sleep mode current (T_A = 125°C)	-	20	1.9	5.85	1.76	10.75	µA
I_{LI}	Input leakage current	-1	1	-0.151	0.143	-0.040	0.044	µA
I_{LO}	Output leakage current SO	-1	1	-0.002	0.002	-0.040	0.042	µA
V_{IH}	Input HIGH Voltage (V_{DD} = 2.0V)	1.4	-	1.08	1.30	1.02	1.28	V
V_{IH}	Input HIGH Voltage (V_{DD} = 3.0V)	2.1	-	1.46	1.74	1.52	1.78	V
V_{IH}	Input HIGH Voltage (V_{DD} = 3.6V)	2.52	-	1.70	2.02	1.64	1.90	V
V_{IL}	Input LOW Voltage (V_{DD} = 2.0V)	-	0.6	0.70	0.92	0.66	0.96	V

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
V_{IL}	Input LOW Voltage (V_{DD} = 3.0V)	-	0.9	1.00	1.24	1.06	1.30	V
V_{IL}	Input LOW Voltage (V_{DD} = 3.6V)	-	1.08	1.16	1.40	1.14	1.38	V
V_{OH1}	Output HIGH Voltage (I_{OH} = -1 mA, V_{DD} = 2.7V)	2.4	-	2.60	2.63	2.58	2.63	V
V_{OH2}	Output HIGH Voltage (I_{OH}= -100 µA, V_{DD} = 2.0V)	1.8	-	1.99	1.99	1.98	1.99	V
V_{OL1}	Output LOW Voltage (I_{OL} = 2 mA, V_{DD} = 2.7V)	-	0.4	0.113	0.174	0.110	0.180	V
V_{OL2}	Output LOW Voltage (I_{OL} = 150 µA)	-	0.2	0.008	0.015	0.007	0.015	V

Table 4. DC Characterization Results

4.2.2 AC Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
t_{CH}	Clock HIGH time	18	-	4.30	6.00	4.30	6.90	ns
t_{CL}	Clock LOW time	18	-	5.10	6.30	5.50	6.40	ns
t_{CSU}	Chip select setup	12	-	0.00	1.10	0.50	1.30	ns
t_{CSH}	Chip select hold	12	-	-20.30	-19.80	-20.30	-20.10	ns
t_{ODV}	Output data valid time	-	16	2.80	6.90	3.00	8.40	ns
t_{OH}	Output hold time	0	-	1.90	4.00	2.00	4.70	ns
t_D	Deselect time	60	-	2.10	3.10	2.10	2.10	ns
t_{SU}	Data setup time	8	-	0.3	1.70	1.00	1.80	ns
t_H	Data hold time	8	-	0.1	0.60	0.10	0.50	ns
t_{HS}	/HOLD setup time	12	-	-20	-19.50	-20.00	-19.60	ns
t_{HH}	/HOLD hold time	12	-	0.1	1.30	0.40	1.20	ns

Table 5. AC Characterization Results

4.2.3 Power Cycle Timing Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
t_{PU}	Power-up V_{DD}(min) to first access (/CS LOW)	1	-	0.22	0.41	0.22	0.43	ms
t_{REC}	Recovery time from sleep mode	-	450	299	419	299	439	µs

Table 6. Power Cycle Timing Characterization Results

5.0 Parallel Characterization

5.1 PAR Industrial / Automotive-A Characterization Summary over V_{DD} and Temperature

5.1.1 DC Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage	2	3.6	-	-	-	-	V
I_{DD}	V_{DD} Supply Current	-	12	6.36	7.38	6.30	7.11	mA
I_{SB}	V_{DD} standby current (T_A = 25°C)	-	150	70.31	99.44	59.31	101.38	µA
	V_{DD} standby current (T_A = 85°C)	-	250	73.19	127.94	106.44	140.94	µA
I_{ZZ}	Sleep mode current (T_A = 25°C)	-	5	1.34	3.91	0.06	3.38	µA
	Sleep mode current (T_A = 85°C)	-	8	1.14	4.10	0.44	5.90	µA
I_{LI}	Input leakage current	-1	1	-0.002	0.176	-0.10	0.039	µA
I_{LO}	Output leakage current (SO)	-1	1	-0.001	0.143	-0.12	0.15	µA
V_{IH1}	Input HIGH Voltage (V_{DD} = 2.7 V to 3.6 V)	2.2	V_{DD} + 0.3	2.10	2.16	2.08	2.14	V
V_{IH2}	Input HIGH Voltage (V_{DD} = 2.0 V to 2.7 V)	0.7 x V_{DD}	-	1.14	1.46	1.13	1.22	V
V_{IL1}	Input LOW Voltage (V_{DD} = 2.7 V to 3.6 V)	-0.3	0.8	1.38	1.44	1.27	1.34	V
V_{IL2}	Input LOW Voltage (V_{DD} = 2.0 V to 2.7 V)	-0.3	0.3 x V_{DD}	0.83	1.05	0.80	0.89	V
V_{OH1}	Output HIGH Voltage (I_{OH} = -1 mA, V_{DD} > 2.7V)	2.4	-	2.64	3.65	2.93	3.56	V
V_{OH2}	Output HIGH Voltage (I_{OH} = -100 µA)	V_{DD} - 0.2	-	1.98	1.99	1.98	1.99	V
V_{OL1}	Output LOW Voltage (I_{OL} = 2 mA, V_{DD} > 2.7V)	-	0.4	0.01	0.10	0.05	0.09	V
V_{OL2}	Output LOW Voltage (I_{OL} = 150 µA)	-	0.2	0.01	0.06	0.01	0.02	V

Table 7. DC Characterization Results

5.1.2 AC Read Cycle Characterization

Parameter	Description	Datasheet V_{DD} = 2.0 to 2.7V		Datasheet V_{DD} = 2.7 to 3.6V		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CE}	Chip enable access time	-	70	-	60	39.45	54.10	35.55	54.10	ns
t_{RC}	Read cycle time	105	-	90	-	71.52	60.23	68.20	77.50	ns
t_{AA}	Address access time, A_{16-2}	-	105	-	90	56.90	74.12	51.27	77.46	ns
t_{OH}	Output hold time, A_{16-2}	20	-	20	-	35.00	63.60	48.13	71.25	ns
t_{AAP}	Page mode access time, A_{1-0}	-	40	-	30	16.41	29.53	16.16	25.70	ns
t_{OHP}	Page mode output hold time, A_{1-0}	3	-	3	-	5.43	16.95	5.82	9.53	ns
t_{CA}	Chip enable active time	70	-	60	-	39.10	52.09	36.17	57.34	ns
t_{PC}	Pre-charge time	35	-	30	-	27.83	16.68	15.66	22.89	ns
t_{BA}	/UB, /LB access time	-	25	-	15	3.05	9.84	3.75	7.73	ns
t_{AS}	Address setup time (to /CE LOW)	0	-	0	-	-4.75	-3.37	-5.47	-3.83	ns
t_{AH}	Address hold time (/CE Controlled)	70	-	60	-	39.10	52.43	35.73	54.63	ns
t_{OE}	Output enable access time	-	25	-	15	2.41	14.66	3.06	7.00	ns

Table 8. AC Read Cycle Characterization Results

5.1.3 AC Write Cycle Characterization

Parameter	Description	Datasheet V_{DD} = 2.0 to 2.7V		Datasheet V_{DD} = 2.7 to 3.6V		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	105	-	90	-	62.00	73.71	56.13	81.33	ns
t_{CA}	Chip enable active time	70	-	60	-	42.03	51.33	38.2	57.50	ns
t_{CW}	Chip enable to write enable HIGH	70	-	60	-	42.81	52.97	39.53	57.81	ns
t_{PC}	Precharge time	35	-	30	-	18.87	27.81	17.42	25.08	ns
t_{PWC}	Page mode write enable cycle time	40	-	30	-	20.63	26.25	20.00	28.75	ns
t_{WP}	Write enable pulse width	22	-	18	-	4.00	4.20	4.00	4.00	ns
t_{WP2}	/UB, /LB pulse width	22	-	18	-	4.00	4.18	4.00	4.00	ns
t_{WP3}	/WE LOW to /UB, /LB HIGH	22	-	18	-	0.20	2.15	0.78	0.98	ns
t_{AS}	Address setup time (to /CE LOW)	0	-	0	-	-5.16	-3.13	-5.47	-4.22	ns
t_{AH}	Address hold time (/CE Controlled)	70	-	60	-	41.13	50.16	38.13	55.1	ns
t_{ASP}	Page mode address setup time (to /WE LOW)	8	-	5	-	-2.00	2.11	-0.43	0.16	ns
t_{AHP}	Page mode address hold time (to /WE LOW)	20	-	15	-	0.90	1.97	0.61	1.02	ns
t_{WLC}	Write enable LOW to chip disabled	30	-	25	-	0.00	1.72	0.94	1.41	ns
t_{BLC}	/UB, /LB LOW to chip disabled	30	-	25	-	-0.25	1.33	-0.08	0.27	ns
t_{WLA}	Write enable LOW to address change, A_{16-2}	30	-	25	-	4.00	4.14	4.00	4.00	ns
t_{AWH}	Address change to write enable HIGH, A_{16-2}	105	-	90	-	60.66	72.83	54.79	80.22	ns
t_{DS}	Data input setup time	20	-	15	-	4.98	7.31	4.08	7.52	ns
t_{DH}	Data input hold time	0	-	0	-	-3.75	-2.97	-5.16	-2.50	ns
t_{WX}	Write enable HIGH to output driven	8	-	5	-	2.87	3.75	2.95	3.88	ns
t_{BDS}	Byte disable setup time (to /WE LOW)	8	-	5	-	-2.34	0.00	-2.19	-1.56	ns
t_{BDH}	Byte disable hold time (to /WE HIGH)	8	-	5	-	-1.95	1.094	0.16	0.16	ns

Table 9. AC Write Cycle Characterization Results

5.1.4 Power Cycle Timing Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
t_{PU}	Power-up V_{DD}(min) to first access (/CS LOW)	1	-	0.38	0.47	0.168	0.525	ms
t_{WEZZ}	Last write to sleep mode entry time	0	-	-0.39	-0.37	-0.39	-0.38	µs
t_{ZZL}	/ZZ active LOW time	1	-	0.2	0.2	0.2	0.2	µs
t_{ZZEN}	Sleep mode entry time (/ZZ LOW to /CE don't care)	-	0	-38.69	-37.94	-39.92	-37.23	µs
t_{ZZEX}	Sleep mode exit time (/ZZ HIGH to 1st access after wakeup)	-	450	301	371	301.9	404.3	µs

Table 10. Power Cycle Timing Characterization Results

5.2 PAR Automotive-E Characterization Summary over V_{DD} and Temperature

5.2.1 DC Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
V_{DD}	Power Supply Voltage	2	3.6	-	-	-	-	V
I_{DD}	V_{DD} Supply Current	-	20	6.40	7.51	6.30	7.26	mA
I_{SB}	V_{DD} standby current (T_A = 25C)	-	150	73.00	88.50	59.31	101.38	µA
	V_{DD} standby current (T_A = 125C)	-	700	236.44	275.06	206.56	274.75	µA
I_{ZZ}	Sleep mode current (T_A = 25C)	-	5	1.44	3.20	0.06	3.01	µA
	Sleep mode current (T_A = 125C)	-	20	3.80	9.53	2.36	10.24	µA
I_{LI}	Input leakage current	-1	1	-0.01	0.21	-0.10	0.39	µA
I_{LO}	Output leakage current (SO)	-1	1	-0.04	0.21	-0.12	0.15	µA
V_{IH1}	Input HIGH Voltage (V_{DD} = 2.7 V to 3.6 V)	2.2	V_{DD} + 0.3	1.58	1.89	1.82	1.85	V
V_{IH2}	Input HIGH Voltage (V_{DD} = 2.0 V to 2.7 V)	0.7 x V_{DD}	-	1.14	1.46	1.13	1.22	V
V_{IL1}	Input LOW Voltage (V_{DD} = 2.7 V to 3.6 V)	-0.3	0.8	1.14	1.34	1.09	1.19	V
V_{IL2}	Input LOW Voltage (V_{DD} = 2.0 V to 2.7 V)	-0.3	0.3 x V_{DD}	0.83	1.05	0.80	0.89	V
V_{OH1}	Output HIGH Voltage (I_{OH} = -1 mA, V_{DD} > 2.7V)	2.4	-	2.93	3.83	2.93	3.56	V
V_{OH2}	Output HIGH Voltage (I_{OH} = -100 µA)	V_{DD} - 0.2	-	1.98	1.99	1.98	1.99	V
V_{OL1}	Output LOW Voltage (I_{OL} = 2 mA, V_{DD} > 2.7V)	-	0.4	0.07	0.10	0.05	0.16	V
V_{OL2}	Output LOW Voltage (I_{OL} = 150 µA)	-	0.2	0.01	0.06	0.01	0.02	V

Table 11. DC Characterization Results

5.2.2 AC Read Cycle Characterization

Parameter	Description	Datasheet V_{DD} = 2.0 to 2.7V		Datasheet V_{DD} = 2.7 to 3.6V		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CE}	Chip enable access time	-	70	-	60	40.23	53.71	35.55	54.10	ns
t_{RC}	Read cycle time	105	-	90	-	61.56	79.49	52.27	78.16	ns
t_{AA}	Address access time, A_{16-2}	-	105	-	90	57.95	77.11	51.27	77.46	ns
t_{OH}	Output hold time, A_{16-2}	20	-	20	-	55.16	71.25	48.13	71.25	ns
t_{AAP}	Page mode access time, A_{1-0}	-	40	-	30	16.54	24.34	16.13	25.70	ns
t_{OHP}	Page mode output hold time, A_{1-0}	3	-	3	-	5.23	7.77	5.82	9.53	ns
t_{CA}	Chip enable active time	70	-	60	-	40.86	55.51	36.17	55.51	ns
t_{PC}	Precharge time	35	-	30	-	17.72	23.40	15.66	22.89	ns
t_{BA}	/UB, /LB access time	-	25	-	15	3.52	7.50	3.75	7.73	ns
t_{AS}	Address setup time (to /CE LOW)	0	-	0	-	-5.00	-4.06	-5.47	-4.08	ns
t_{AH}	Address hold time (/CE Controlled)	70	-	60	-	40.27	54.63	35.73	54.63	ns
t_{OE}	Output enable access time	-	25	-	15	2.84	6.78	3.06	7.00	ns

Table 12. AC Read Cycle Characterization Results

5.2.3 AC Write Cycle Characterization

Parameter	Description	Datasheet V_{DD} = 2.0 to 2.7V		Datasheet V_{DD} = 2.7 to 3.6V		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	90	-	105	-	64.34	81.33	56.13	80.74	ns
t_{CA}	Chip enable active time	60	-	70	-	42.22	57.66	35.00	52.58	ns
t_{CW}	Chip enable to write enable HIGH	60	-	70	-	45.47	58.13	39.53	57.66	ns
t_{PC}	Precharge time	30	-	35	-	19.69	23.98	15.22	22.73	ns
t_{PWC}	Page mode write enable cycle time	30	-	40	-	21.25	27.50	20.00	28.75	ns
t_{WP}	Write enable pulse width	18	-	22	-	4.20	4.20	4.00	4.10	ns
t_{WP2}	/UB, /LB pulse width	18	-	22	-	4.18	4.18	4.00	4.10	ns
t_{WP3}	/WE LOW to /UB, /LB HIGH	18	-	22	-	0.98	1.17	0.78	1.17	ns
t_{AS}	Address setup time (to /CE LOW)	0	-	0	-	-4.69	-4.38	-5.70	-4.06	ns
t_{AH}	Address hold time (/CE Controlled)	60	-	70	-	44.14	56.17	35.29	51.85	ns
t_{ASP}	Page mode address setup time (to /WE LOW)	5	-	8	-	0.16	0.16	0.16	0.16	ns
t_{AHP}	Page mode address hold time (to /WE LOW)	15	-	20	-	1.15	1.29	0.61	1.02	ns
t_{WLC}	Write enable LOW to chip disabled	25	-	30	-	1.25	1.41	1.09	1.41	ns
t_{BLC}	/UB, /LB LOW to chip disabled	25	-	30	-	0.27	0.63	-0.08	0.27	ns
t_{WLA}	Write enable LOW to address change, A_{16-2}	25	-	30	-	4.14	4.14	4.00	4.00	ns
t_{AWH}	Address change to write enable HIGH, A_{16-2}	90	-	105	-	62.85	80.22	54.92	80.08	ns
t_{DS}	Data input setup time	15	-	20	-	4.08	7.50	4.08	7.73	ns
t_{DH}	Data input hold time	0	-	0	-	-4.89	-2.73	-5.16	-2.27	ns
t_{WX}	Write enable HIGH to output driven	5	-	8	-	2.60	6.00	2.48	4.94	ns
t_{BDS}	Byte disable setup time (to /WE LOW)	5	-	8	-	-1.88	-1.56	-2.34	-1.56	ns
t_{BDH}	Byte disable hold time (to /WE HIGH)	5	-	8	-	-0.78	0.16	0.16	0.16	ns

Table 13. AC Write Cycle Characterization Results

5.2.4 Power Cycle Timing Characterization

Parameter	Description	Datasheet		DMOS5		DMOS6		Units
		Min	Max	Min	Max	Min	Max	
t_{PU}	Power-up V_{DD}(min) to first access (/CS LOW)	1	-	228.13	525.00	168.75	525.00	ms
t_{WEZZ}	Last write to sleep mode entry time	0	-	-39.40	-37.64	-39.04	-37.24	µs
t_{ZZL}	/ZZ active LOW time	1	-	0.20	0.20	0.20	0.20	µs
t_{ZZEN}	Sleep mode entry time (/ZZ LOW to /CE don't care)	-	0	-39.75	-37.99	-39.92	-36.57	µs
t_{ZZEX}	Sleep mode exit time (/ZZ HIGH to 1st access after wakeup)	-	450	318.16	422.48	301.90	438.75	µs

Table 14. Power Cycle Timing Characterization Results

Document History Page

Rev.	ECN No.	Orig. of Change	Description of Change
**	5546192	JBEV	New Characterization Report.

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Cypress Semiconductor
Product Qualification Report

QTP#143905 VERSION **
January, 2017

1Mb and 2Mb F-RAM Memory Product Qualification 130nm Technology, TI 300mm wafer Fab DMOS 6	
FM25V20A-G	2Mb (256Kx8bits) Serial F-RAM Memory
FM25V20A-GTR	2Mb (256Kx8bits) Serial F-RAM Memory
FM25V20A-DG	2Mb (256Kx8bits) Serial F-RAM Memory
FM25V20A-DGTR	2Mb (256Kx8bits) Serial F-RAM Memory
FM25V20A-DGQ	2Mb (256Kx8bits) Serial F-RAM Memory with Extended Temperature
FM25V20A-DGQTR	2Mb (256Kx8bits) Serial F-RAM Memory with Extended Temperature
FM25V20A-PG	2Mb (256Kx8bits) Serial F-RAM Memory
FM28V202A-TG	2Mb (128Kx16bits) Parallel F-RAM Memory
FM28V202A-TGTR	2Mb (128Kx16bits) Parallel F-RAM Memory
FM28V102A-TG	1Mb (64Kx16bits) Parallel F-RAM Memory
FM28V102A-TGTR	1Mb (64Kx16bits) Parallel F-RAM Memory

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com or via a CYLINK CRM CASE

Prepared By:
Su Zheng
Reliability Engineer

Reviewed By:
Yusaku Ohta
Reliability Manager

Approved By:
David Hoffman
Reliability Director

PACKAGE/PRODUCT QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date
143905	TI FR130 DMOS5 (200mm wafer fab) to DMOS6 (300mm wafer fab) foundry transfer using the TR20005B (2Mb industrial 2T2C F-RAM product)	January 2017

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualification of 130nm FM25V20A-G TR20005 2Mbit 2T2C FRAM foundry transfer from DMOS5(200mm wafer fab) to DMOS6(300mm wafer fab).	
Marketing Part #:	FM25V20A-G, FM25V20A-GTR, FM25V20A-DG, FM25V20A-DGTR, FM25V20A-DGQ, FM25V20A-DGQTR, FM25V20A-PG, FM28V202A-TG, FM28V202A-TGTR, FM28V102A-TG, FM28V102A-TGTR
Device Description:	1Mb and 2Mb F-RAM Serial and Parallel Memory
Cypress Division:	Cypress Semiconductor Corporation – Memory Products Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	Proprietary*	Metal Composition:	Proprietary*
Passivation Type and Thickness:			Proprietary*
Generic Process Technology/Design Rule (□-drawn):			130nm
Gate Oxide Material/Thickness (MOS):			Proprietary*
Name/Location of Die Fab (prime) Facility:			Texas Instruments / Dallas
Die Fab Line ID/Wafer Process ID:			DMOS 6 / E035.1

***Texas Instruments' proprietary information is available with signed NDA.**

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
8-pin SOIC	UTAC, Thailand (UT)
8-pin PDIP	UTAC, Thailand (UT)
8-pin TDFN	UTAC, Thailand (UT)
44-pin TSOPII	JCET, China (JT)

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	SZ820
Package Outline, Type, or Name:	SOIC 8L (208mils)
Mold Compound Name/Manufacturer:	G600 / Sumitomo
Mold Compound Flammability Rating:	UL 94 V=0 pass
Mold Compound Alpha Emission Rate:	<0.1
Oxygen Rating Index: >28%	53%
Lead Frame Designation:	FMP
Lead Frame Material:	Copper
Substrate Material:	N/A
Lead Finish, Composition / Thickness:	Matte Sn
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Henkel
Die Attach Material:	8200T
Bond Diagram Designation	001-86122
Wire Bond Method:	Thermosonic
Wire Material/Size:	CuPd / 0.8 mil
Thermal Resistance Theta JA °C/W:	114 C/W
Package Cross Section Yes/No:	Yes
Assembly Process Flow:	001-94050M
Name/Location of Assembly (prime) facility:	UTAC, Thailand (UT)
MSL LEVEL	MSL3
REFLOW PROFILE	260 C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	UTAC, Thailand / KYEC, Taiwan

Note: Please contact a Cypress Representative for other package availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Data Retention (Plastic)	125 C, non-biased JESD22-A117 and JESD22-A103	P
Endurance Test	MIL-STD-883, Method 883-1033	P
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.6V, 125 C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.6V, 125 C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.6V, 125 C JESD22-A108	P
Low Temperature Operating Life Cold Life Test	Dynamic Operating Condition, Vcc = 4.3V, -30 C, f = 4MHz JESD22-A108	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 4.3V, -30 C	P
Long Life Verification	Dynamic Operating Condition, Vcc = 3.6V, 125 C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130C, 85%RH, nnV Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30 C, 60% RH)	P
Pressure Cooker Test	JESD22-A102: 121 C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30 C, 60% RH)	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65 C to 150 C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30 C, 60% RH)	P
High Temp Storage	JESD22-A103: 150 C, no bias Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30 C, 60% RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	(1,100V, 2,200V, 3,300V) JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	(500V, 750V, 1,000V, 1,250V) JESD22-C101	P
Static Latch up	125C, ± 140mA JESD78B	P

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Neutron Emission (SER)	Vccnom, room temperature, JESD89	<1.47 FIT/Mb
Neutron Single Latch-up (SEL)	Vccmax, Data Sheet max temperature, JESD89	No event

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	14,950 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	534,000 DHRs	0	0.7	55	31 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 143905

Device	package	Fab Lot#	Assy Lot#	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	15	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	15	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	15	0	
STRESS: TEMPERATURE CYCLE CONDITION C（-65C TO 150C）, with MSL3 Preconditioning								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	500	80	0	
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	1000	80	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	500	79	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	1000	79	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	500	80	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	1000	80	0	
STRESS: PRESSURE COOKER TEST(121C,100%RH, with MSL3 Preconditioning)								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	168	80	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	168	80	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	168	80	0	
STRESS: HIGH ACCELERATED SATURATION TEST(130C, 85%RH, with MSL3 Preconditioning)								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	96	28	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	96	27	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	96	28	0	
STRESS: HIGH TEMPERATURE STORAGE,150C								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	500	80	0	
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	1000	80	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	500	80	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	1000	80	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	500	80	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	1000	80	0	
STRESS: ESD-MACHINE MODEL								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	200	5	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	200	5	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	200	5	0	
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	200	5	0	
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	200	5	0	
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	200	5	0	
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	200	5	0	
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	200	5	0	
STRESS: ESD-CHARGE DEVICE MODEL(500V)								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	9	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	9	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	9	0	
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	9	0	
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	9	0	
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	9	0	
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	9	0	
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL(750V)								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0	
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0	
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0	
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0	
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0	
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL(1000V)								
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0	
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0	

FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: ESD-CHARGE DEVICE MODEL(1250V)

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: ESD-CHARGE DEVICE MODEL(1500V)

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: ESD-CHARGE DEVICE MODEL(1750V)

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: ESD-CHARGE DEVICE MODEL(2000V)

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0

STRESS: ESD-HUMAN BODY CIRCUIT（1100V）

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: ESD-HUMAN BODY CIRCUIT（2200V）

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	8	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	8	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	8	0
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	8	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	8	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	8	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	8	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	8	0

STRESS: ESD-HUMAN BODY CIRCUIT（3300V）

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0

CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: STATIC LATCH-UP (+/-140mA 125C)

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2443004	611444239	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611600876	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2602005	611602793	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617892	UT	COMP	3	0
CY15B102Q7-SXE	SZ820AAZAR	2538007	611617893	UT	COMP	3	0

STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	96	1500	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	96	941	0
FM25V20A-G	SZ820ABASC	2444010	611513111	UT	96	784	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	96	1442	0
CY15B102Q7-SXE	SZ820AAZAR	2553000	611627196	UT	96	3500	0
CY15B102Q7-SXE	SZ820AAZAR	2629051	611627197	UT	96	3283	0
FM25V20A-G	SZ820ABASC	2629051	611627197	UT	96	3500	0

STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C

FM25V20A-G	SZ820ABASC	2445005	611503699	UT	116	178	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	1000	178	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	116	178	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	1000	178	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	116	178	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	1000	178	0

STRESS: EFR-REGULATOR ON

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	96	45	0

STRESS: AGED BOND STRENGTH

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	COMP	3	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	COMP	3	0

STRESS: DATA RETENTION,125C

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	500	77	0
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	1000	75	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	500	77	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	1000	77	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	500	77	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	1000	77	0

STRESS: ENDURANCE and DATA RETENTION

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	168	77	0
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	500	77	0
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	1000	77	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	168	77	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	500	77	0
FM25V20A-G	SZ820ABASC	2444010	611503700	UT	1000	76	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	168	77	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	500	77	0
FM25V20A-G	SZ820ABASC	2445005	611503699	UT	1000	77	0

STRESS: LTOL READ & RECRORD,-30C

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	32	0

STRESS: LOW TEMPERATURE OPERATING LIFE,-30C

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	500	32	0
FM25V20A-G	SZ820ABASC	2443004	611503131	UT	1000	32	0

STRESS: SOFT ERROR TEST-NEUTRON/PROTON/SEL

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0

STRESS: SOFT ERROR TEST-ALPHA-PATICLE/SEL

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0

STRESS: PRE/POST LFR CRITICAL PARAMETER

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	12	0

STRESS: CONSTRUCTIONAL ANALYIS

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	5	0

STRESS: DYNAMIC/LATCH-UP

FM25V20A-G	SZ820ABASC	2443004	611503131	UT	COMP	3	0

Document History Page

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Document Number: 002-18390

Rev.	ECN No.	Orig. of Change	Description of Change
**	5580521	SUZH	Initial Release

Item	Marketing Part Number	Sample Order Part Number	Included In
1	FM25V20A-G	FM25V20A7-G	PCN170501
2	FM25V20A-DG	FM25V20A7-DG	PCN170501
3	FM25V20A-DGQ	FM25V20A7-DGQ	PCN170501
4	FM25V20A-PG	FM25V20A7-PG	PCN170501
5	FM28V102A-TG	FM28V102A7-TG	PCN170501
6	FM28V202A-TG	FM28V202A7-TG	PCN170501
7	FM25V20A-DGQTR	FM25V20A7-DGQ; Subject to lead time	PCN170501A
8	FM25V20A-DGTR	FM25V20A7-DG	PCN170501A
9	FM25V20A-GTR	FM25V20A7-G	PCN170501A
10	FM28V102A-TGTR	FM28V102A7-TG	PCN170501A
11	FM28V202A-TGTR	FM28V202A7-TG	PCN170501A
12	CG8668AM	FM25V20A7-G	PCN170501A
13	CG8668AMT	FM25V20A7-G	PCN170501A